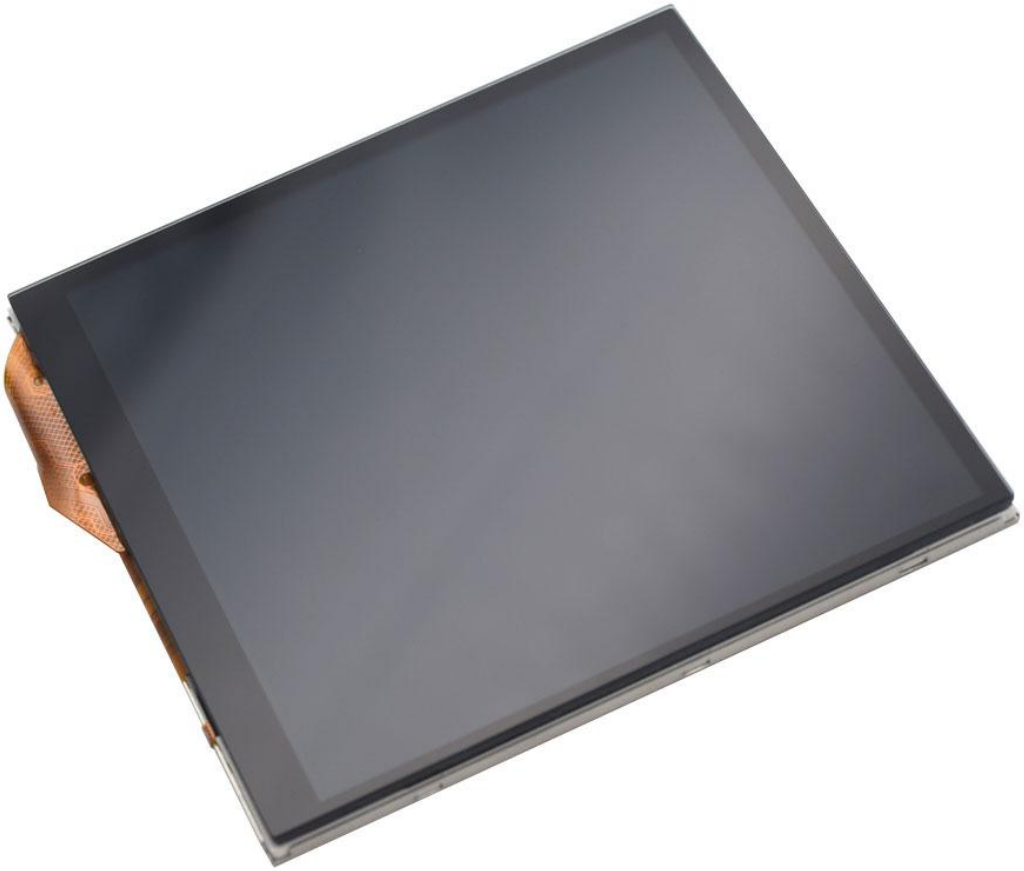
DisplayModule



DM-TFT40-416

4.0" IPS 480 × 480 High Brightness TFT Display Panel With Capacitive Touch –MIPI

Contents

1 Revision History

2 Main Features

3 Pin Description

3.1 Panel Pin Description

3.2 CTP Pin Description

4 Mechanical Drawing

4.1 Panel Mechanical Drawing

5 Function Block Diagram

6 Optics & Electrical Characteristics

6.1 Optical Characteristics

6.2 Absolute Maximum Ratings

6.3 DC Characteristics

6.3.1 MIPI DC Characteristics

6.4 LED Backlight Characteristics

6.5 AC Characteristics

6.5.1 MIPI Interface Characteristics

6.5.2 Display RESET Timing Characteristics

7 CTP Specification

7.1 Electrical Characteristics

7.1.1 Absolute Maximum Rating

7.1.2 DC Electrical Characteristics(Ta=25 °C)

7.1.3 AC Characteristics

7.2 I2C Timing

8 Reliability

9 Warranty and Conditions

1 Revision History

Date	Changes
2020-04-20	First release

2 Main Features

Item	Specification	Unit
Diagonal Size	4.0	inch
Driver element	TFT active matrix	-
Pixel arrangement	RGB vertical stripe	-
Display mode	Transmissive /Normally Black	-
Display Colors	16.7M	Colors
Resolution	480 x 480	pixel
Controller IC	ST7701S	-
LCD Interface	2-lane MIPI	-
CTP IC	GT911	-
CTP Interface	I2C	-
Touch mode	Five points and Gestures	-
Active Area	71.86 x 70.18	mm
Panel Dimension	77 x 80 x 4.35	mm
Pixel Pitch	0.1497 x 0.1462	mm
Weight	TBD	g

3 Pin Description

3.1 Panel Pin Description

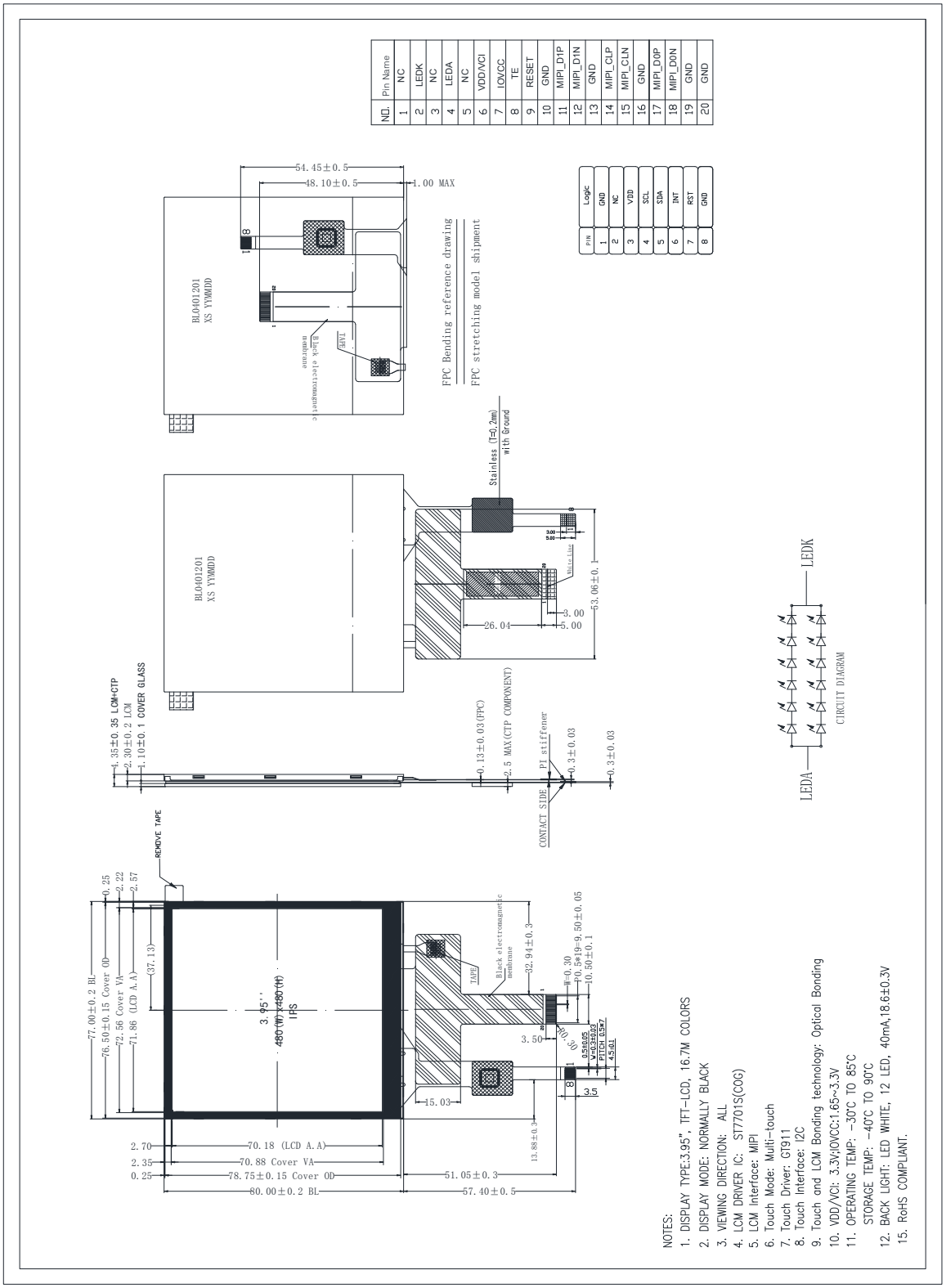
Pin No.	Symbol	Function Description
1	NC	-
2	LEDK	Cathode pin of backlight.
3	NC	-
4	LEDA	Anode pin of backlight.
5	NC	-
6	VDD/VCI	Supply Voltage (3.3V).
7	IOVCC	I/O power supply voltage.
8	TE	-Tearing effect output Leave the pin to open when not in use.
9	RESET	- The external reset input. Initializes the chip with a low input. Be sure to execute a power-on reset after supplying power.
10	GND	Ground.
11	MIPI_D1P	MIPI DSI differential data pair (DSI-Dn+/-).
12	MIPI_D1N	
13	GND	Ground.
14	MIPI_CLP	MIPI DSI differential clock pair (DSI-CLK+/-).
15	MIPI_CLN	
16	GND	Ground.
17	MIPI_D0P	MIPI DSI differential data pair (DSI-Dn+/-).
18	MIPI_D0N	
19	GND	Ground.
20	GND	Ground.

3.2 CTP Pin Description

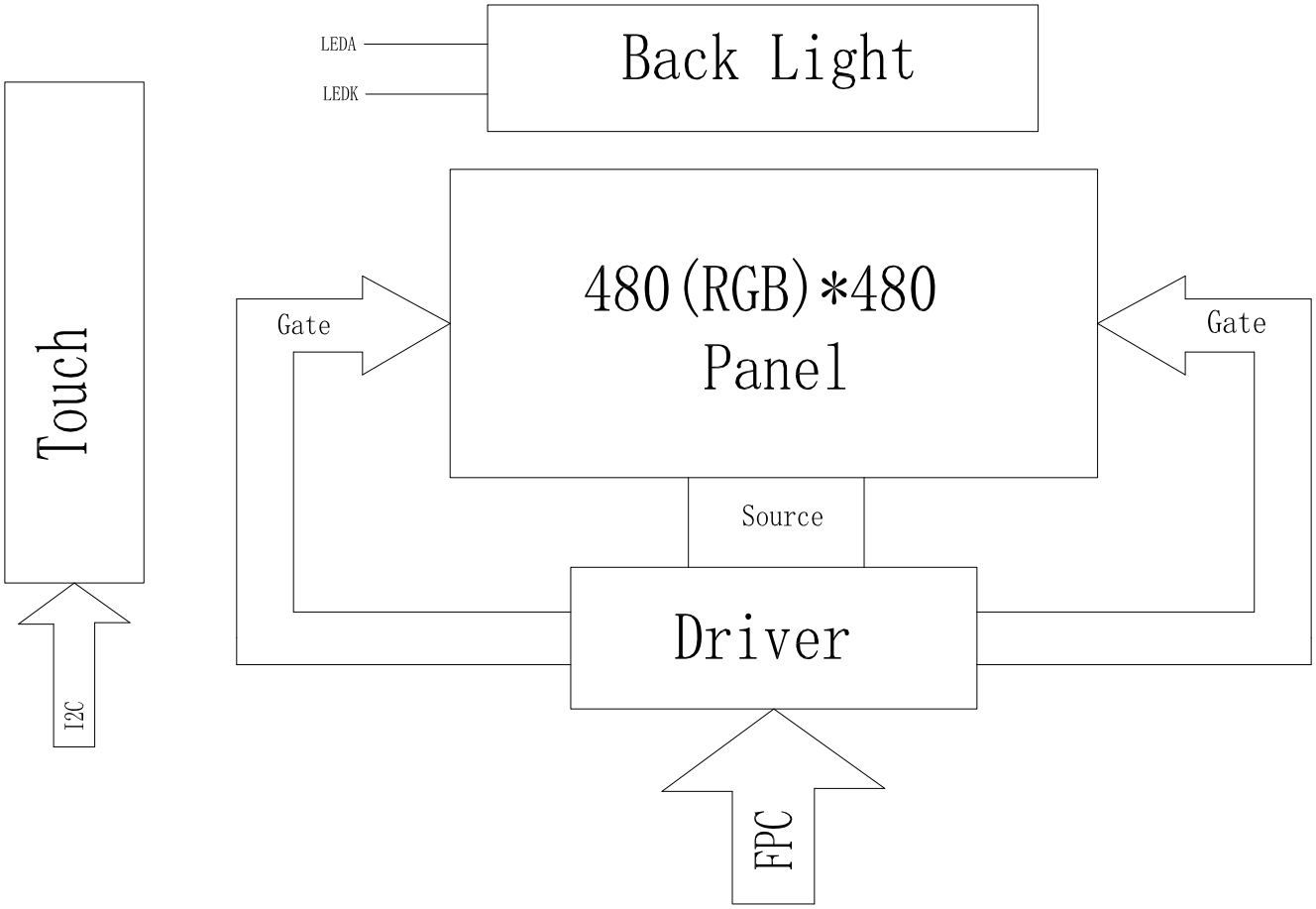
Pin No.	Symbol	Function Description
1	GND	Ground
2	NC	No Connection
3	VDD	Supply voltage
4	SCL	I2C clock input
5	SDA	I2C data input and output
6	INT	External interrupt to the host
7	RST	External Reset, Low is active
8	GND	Ground

4 Mechanical Drawing

4.1 Panel Mechanical Drawing



5 Function Block Diagram



6 Optics & Electrical Characteristics

6.1 Optical Characteristics

Item		Symbol	Min	Typ	Max	Unit	Remark
View Angles			70	80	-	°	CR>10
C.I.E. (White)		(x) (y)	0.269 0.310	0.309 0.350	0.349 0.390	-	Θ=0 Normal viewing angle
C.I.E(Red)		(x) (y)	0.571 0.323	0.611 0.363	0.651 0.403	-	
C.I.E(Green)		(x) (y)	0.277 0.530	0.317 0.570	0.357 0.610	-	
C.I.E(Blue)		(x) (y)	0.110 0.060	0.150 0.100	0.190 0.140	-	
Response time	Rising Falling	T_R+T_F	-	25	35	msec	-
Contrast Ratio		CR	640	800	-	-	-
Uniformity		S(%)	55	60	-	%	C-light
Option View Direction		ALL					

Note: Measuring Condition

- Measuring surrounding：dark room
- Ambient temperature：25±2°C
- 15min. warm-up time.

6.2 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Remark
Digital Supply Voltage	V_{CI}	-0.3	4.6	V	Note
Digital interface Supply Voltage	I_{OVCC}	-0.3	4.6	V	Note
Operating Temperature	T_{OP}	-30	85	℃	-
Storage Temperature	T_{STG}	-40	90	℃	-

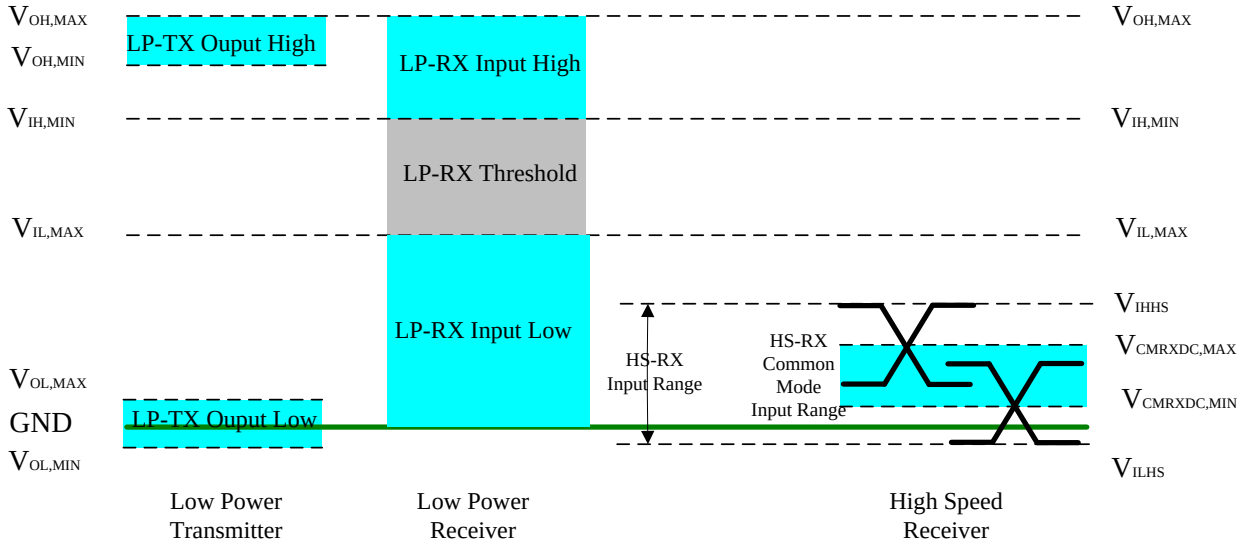
Note: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

6.3 DC Characteristics

Item	Symbol	Min	Typ.	Max	Unit	Remark
Digital Supply Voltage	V_{CI}	2.5	3.3	3.6	V	-
Digital interface supply Voltage	I_{OVCC}	1.65	1.8	3.3	V	-
Normal mode Current	I_{DD}	-	30	-	mA	-
Differential Input High Threshold Voltage	VIT+	-	0	50	mV	MIPI_CLK MIPI_Data
Differential Input Low Threshold Voltage	VIT-	-50	0	-	mV	
Sigle-ended Receiver Input Operation Voltage Range	VIR	0.5	-	1.2	V	

Note : The VCC input must be kept in a stable value; ripple and noise are not allowed.

6.3.1 MIPI DC Characteristics



Parameter	Symbol	Min	Typ.	Max	Unit
Operation Voltage for MIPI Receiver					
Low power mode operating voltage	VLPH	1.1	1.2	1.3	V
MIPI Characteristics for High Speed Receiver					
Single-ended input low voltage	V_{ILHS}	-40	-	-	mV
Single-ended input high voltage	V_{IHHS}	-	-	460	mV
Common-mode voltage	V_{CMRXDC}	70	-	330	mV
Differential input impedance	Z_{ID}	80	100	125	ohm
MIPI Characteristics for Low Power Mode					
Pad signal voltage range	VI	-50	-	1350	mV
Logic 0 input threshold	VIL	0	-	550	mV
Logic 1 input threshold	VIH	880	-	1350	mV
Output low level	VOL	-50	-	50	mV
Output high level	VOH	1.1	1.2	1.3	V

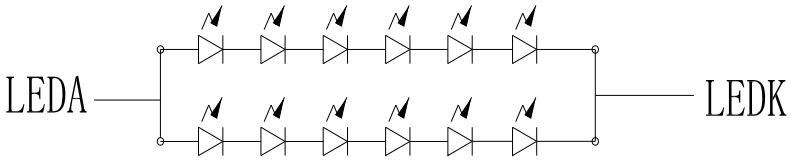
6.4 LED Backlight Characteristics

The back-light system is edge-lighting type with 12 chips White LED

Parameter	Symbol	Min	Typ	Max	Unit	Remark
Forward voltage	V_F	-	18.6	-	V	
Forward current	I_F	35	40	-	mA	
LCM Luminance (IF =40mA)	L_V	900	950	-	cd/m^2	
LED life time	Hr	-	50000	-	Hour	Note1,2
Uniformity	AVg	80	-	-	%	

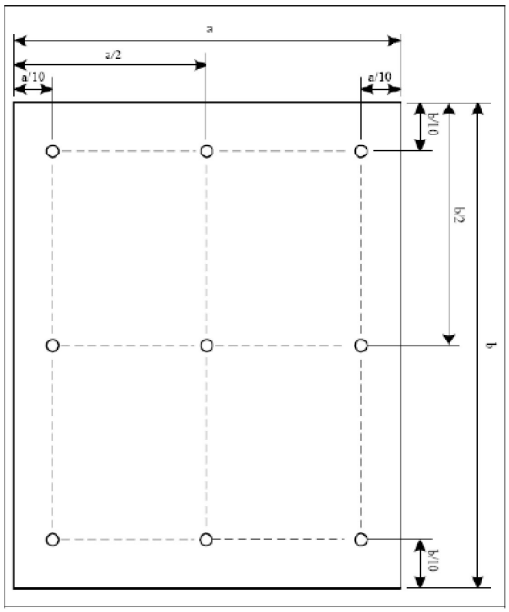
Note1: LED life time (Hr) can be defined as the time in which it continues to operate under the condition: Ta=25±3 ℃, typical IL value indicated in the above table until the brightness becomes less than 50%.

Note2: The "LED life time" is defined as the module brightness decrease to 50% original brightness at Ta=25℃ and IL=40mA. The LED lifetime could be decreased if operating IL is larger than 4 0 mA. The constant current driving method is suggested.



CIRCUIT DIAGRAM

NOTE 3：Luminance Uniformity of these 9 points is defined as below:



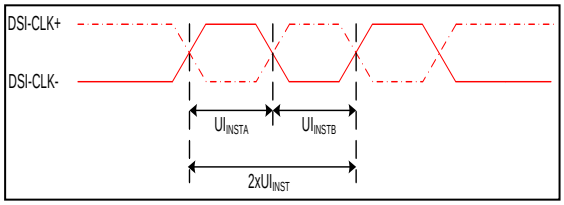
$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points}(1-9)}{\text{maximum luminance in 9 points}(1-9)}$$

$$\text{Lumiance} = \frac{\text{Total lumincace of 9 points}}{9}$$

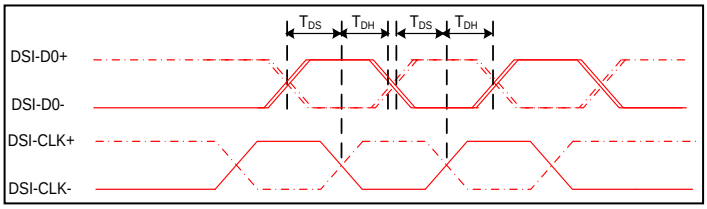
6.5 AC Characteristics

6.5.1 MIPI Interface Characteristics

High Speed Mode



DSI clock channel timing

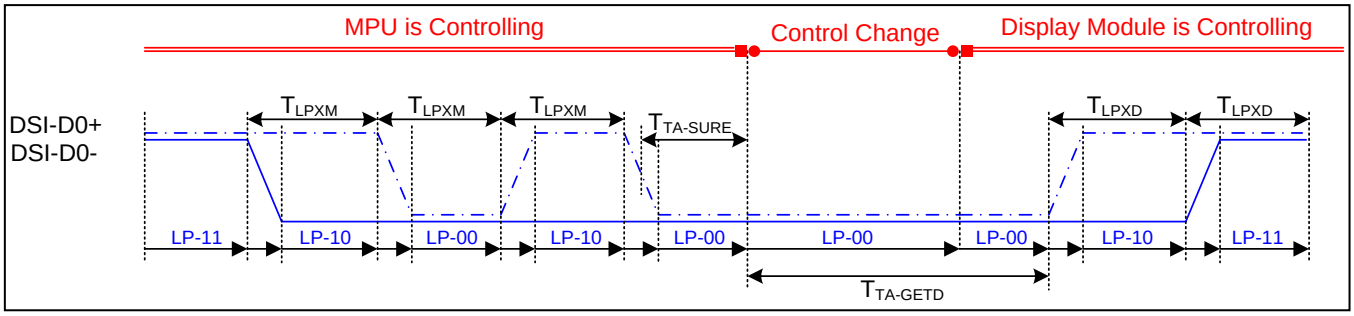


Rising and falling time on clock and data channel

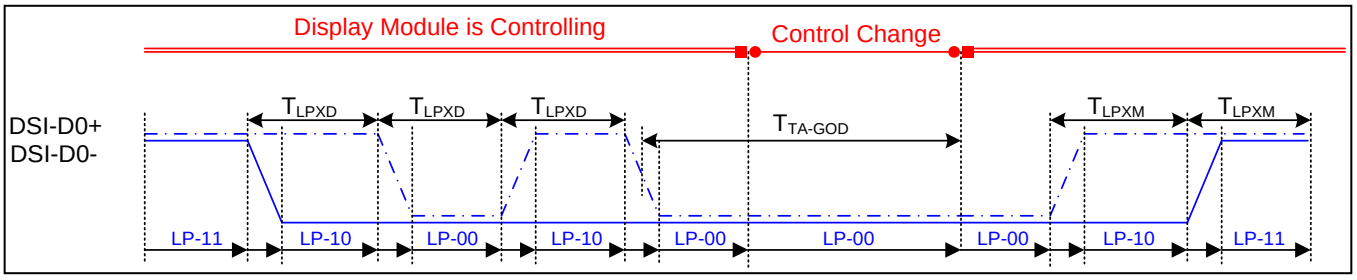
Mipi Interface- High Speed Mode Timing Characteristics

Signal	Symbol	Parameter	Min	Max	Unit	Description
DSI-CLK+/-	$2xUI_{INSTA}$	Double UI instantaneous	4	25	ns	
DSI-CLK+/-	UI_{INSTA} UI_{INSTB}	UI instantaneous halfs	2	12.5	ns	UI = UI_{INSTA} = UI_{INSTB}
DSI-Dn+/-	tDS	Data to clock setup time	0.15	-	UI	
DSI-Dn+/-	tDH	Data to clock hold time	0.15	-	UI	

Lowe Power Mode



Bus Turnaround (BTA) from display module to MPU Timing

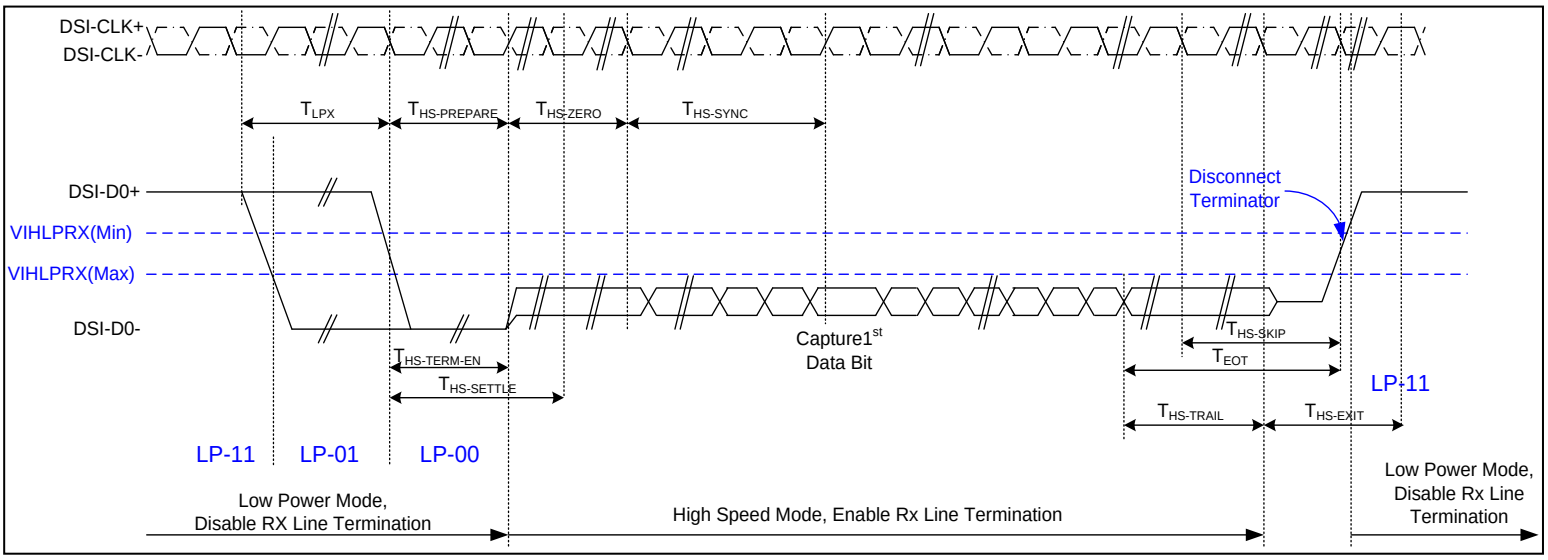


Bus Turnaround (BTA) from MPU to display module Timing

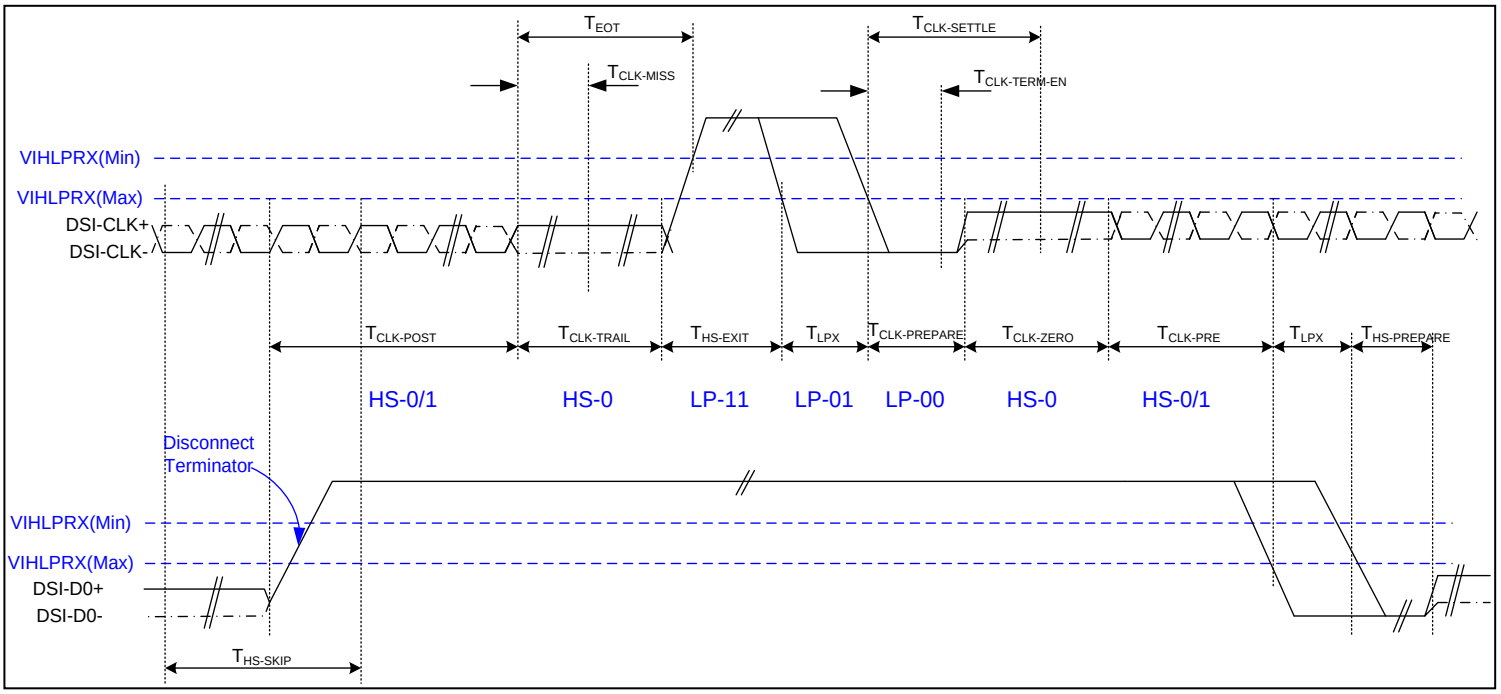
Mipi Interface Low Power Mode Timing Characteristics

Signal	Symbol	Parameter	Min	Max	Unit	Description
DSI-D0+/-	TLPXM	Length of LP-00,LP-01, LP-10 or LP-11 periods MPU Display Module	50	75	ns	Input
DSI-D0+/-	TLPXD	Length of LP-00,LP-01, LP-10 or LP-11 periods MPU Display Modul	50	75	ns	Output
DSI-D0+/-	TTA-SURED	Time-out before the MPU start driving	T_{LPXD}	$2xT_{LPXD}$	ns	Output
DSI-D0+/-	TTA-GETD	Time to drive LP-00 by display module	$5xT_{LPXD}$		ns	Input
DSI-D0+/-	TTA-GOD	Time to drive LP-00 after turnaround request-MPU	$4xT_{LPXD}$		ns	Output

DSI Bursts Mode



Data lanes-Low Power Mode to/from High Speed Mode Timing

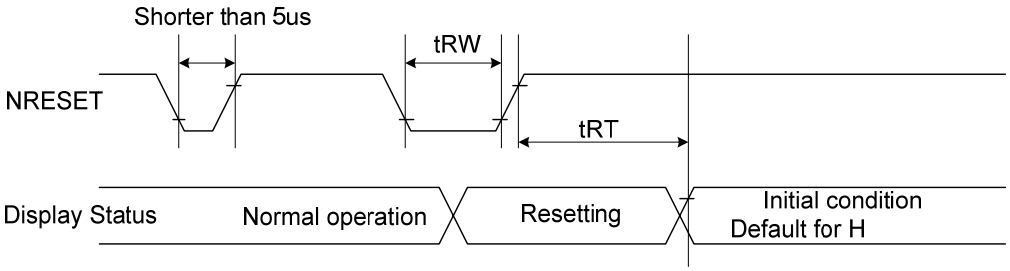


Clock lanes- High Speed Mode to/from Low Power Mode Timing

Signal	Symbol	Parameter	Min	Max	Unit	Description
Low Power Mode to High Speed Mode Timing						
DSI-Dn+/-	TLPX	Length of any low power state period	50	-	ns	Input
DSI-Dn+/-	THS-PREPARE	Time to drive LP-00 to prepare for HS transmission	40+4 UI	85+6 UI	ns	Input
DSI-Dn+/-	THS-TERM-EN	Time to enable data receiver line termination measured from when Dn crosses VILMAX	-	35+4 UI	ns	Input
DSI-Dn+/-	THS-PREPARE + THS-ZERO	THS-PREPARE + time to drive HS-0 before the sync sequence	140+ 10UI	-	ns	Input
High Speed Mode to Low Power Mode Timing						
DSI-Dn+/-	THS-SKIP	Time-out at display module to ignore transition period of EoT	40	55+4 UI	ns	Input
DSI-Dn+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	-	ns	Input
DSI-Dn+/-	THS-TRAIL	Time to drive flipped differential state after last payload data bit of a HS transmission burst	60+4 UI	-	ns	Input
High Speed Mode to/from Low Power Mode Timing						
DSI-CLK+/-	TCLK-POS	Time that the MPU shall continue sending HS clock after the last associated data lane has transition to LP mode	60+5 2UI	-	ns	Input
DSI-CLK+/-	TCLK-TRAIL	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns	Input
DSI-CLK+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	-	ns	Input
DSI-CLK+/-	TCLK-PREPARE	Time to drive LP-00 to prepare for HS transmission	38	95	ns	Input
DSI-CLK+/-	TCLK-TERM-EN	Time-out at clock lan display module to enable HS transmission	-	38	ns	Input
DSI-CLK+/-	TCLK-PREPARE + TCLK-ZERO	Minimum lead HS-0 drive period before starting clock	300	-	ns	Input
DSI-CLK+/-	TCLK-PRE	Time that the HS clock shall be driven prior to any associated data lane beginning the transition from LP to HS mode	8UI	-	ns	Input
DSI-CLK+/-	TEOT	Time form start of TCLK-TRAIL period to start of LP-11 state	-	105n s+12 UI	ns	Input

6.5.2 Display RESET Timing Characteristics

Reset input timing



Timing Parameters

Siganl	Symbol	Parameter	Min	Max	Unit
RESX	TRW	Reset pulse duration	10	-	µs
	TRT	Reset cancel	-	5 (Note 1, 5)	ms
				120 (Note 1, 6, 7)	ms

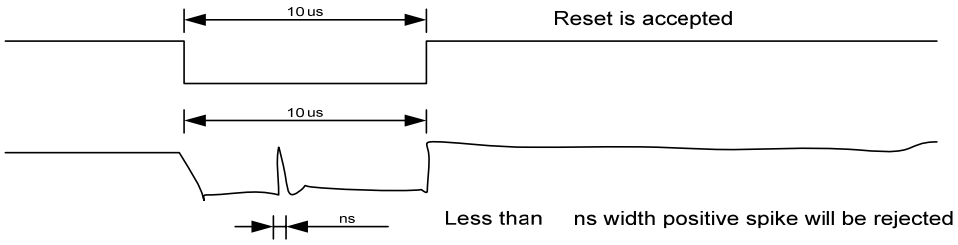
Note 1:The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from OTP to registers. This loading is done every time when there is H/W reset cancel time (tRT) within 5 ms after a rising edge of RESX.

Note 2: Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5µs	Reset Rejected
Longer than 9µs	Reset
Between 5µs and 9µs	Reset starts

Note 3: During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out mode. The display remains the blank state in Sleep In mode.) and then return to Default condition for Hardware Reset.

Note 4: Spike Rejection also applies during a valid reset pulse as shown below:



Note 5: When Reset applied during Sleep In Mode.

Note 6: When Reset applied during Sleep Out Mode.

Note 7: It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

7 CTP Specification

7.1 Electrical Characteristics

7.1.1 Absolute Maximum Rating

Item	Symbol	Min	Max	Unit	Note
Digital Supply Voltage	VDD	2.66	3.47	V	
Operating Temperature	T_{OP}	-30	+85	℃	
Storage Temperature	T_{ST}	-30	+85	℃	

7.1.2 DC Electrical Characteristics(Ta=25 ℃)

(Ambient temperature:25℃, VDD=2.8V, VDDIO=1.8V or VDDIO=VDD)

Item	Min	Type	Max	Unit	Note
Power Supply Voltage/VDD	2.66	3.3	3.47	V	
Normal mode operating current	-	8	14.5	mA	
Green mode operating current	-	3.3	-	mA	
Sleep mode operating current	70	-	120	uA	
Doze mode operating current	-	0.78	-	mA	
Digital Input low voltage/VIL	-0.3	-	0.25*VDD	V	
Digital Input high voltage/VIH	0.75*VDD	-	VDD+0.3	V	
Digital Output low voltage/VOL	-	-	0.15*VDD	V	
Digital Output high voltage/VOH	0.85*VDD	-	-	V	

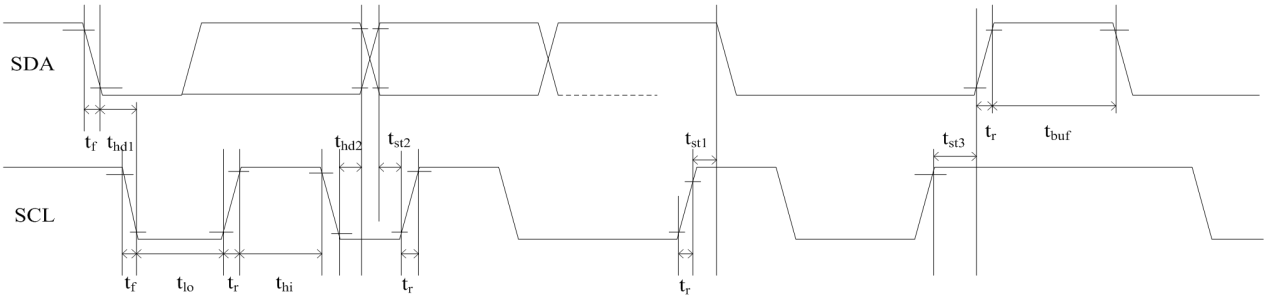
7.1.3 AC Characteristics

(Ambient temperature:25℃, VDD=2.8V, VDDIO=1.8V)

Parameter	Min	Typ	Max	Unit	Note
OSC oscillation frequency	59	60	61	MHz	
I/O output rise time,low to high	-	14	-	ns	
I/O output rfall time,high to low	-	14	-	ns	

7.2 I2C Timing

GT911 provides a standard I2C interface for SCL and SDA to communicate with the host. GT911 always serves as slave device in the system with all communication being initialized by the host. It is strongly recommended that transmission rate be kept at or below 400Kbps. The I2C timing is shown below:



Test condition 1: 1.8V host interface voltage, 400Kbps transmission rate, 2K pull-up resistor

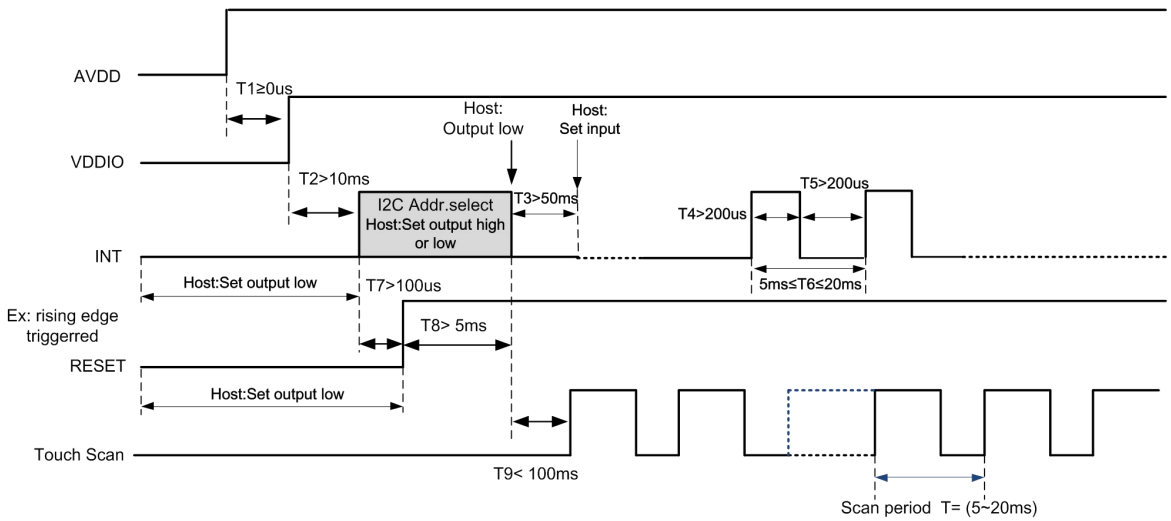
Item	Symbol	Min	Max	Unit
SCL low period	t_{lo}	1.3	-	μs
SCL high period	t_{hi}	0.6	-	μs
SCL setup time for Start condition	t_{st1}	0.6	-	μs
SCL setup time for Stop condition	t_{st3}	0.6	-	μs
SCL hold time for Start condition	t_{hd1}	0.6	-	μs
SDA setup time	t_{st2}	0.1	-	μs
SDA hold time	t_{hd2}	0	-	μs

Test condition 2: 3.3V host interface voltage, 400Kbps transmission rate, 2K pull-up resistor

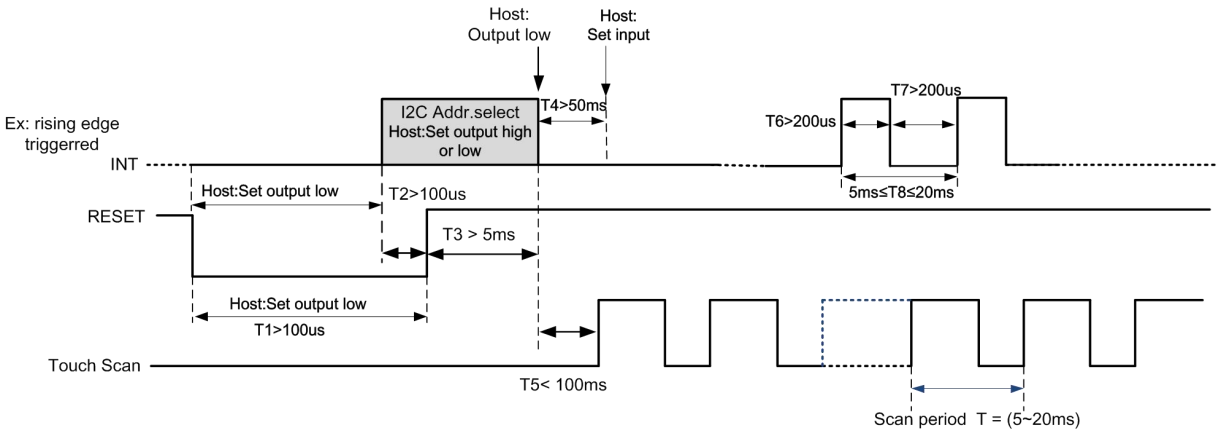
Item	Symbol	Min	Max	Unit
SCL low period	t_{lo}	1.3	-	μs
SCL high period	t_{hi}	0.6	-	μs
SCL setup time for Start condition	t_{st1}	0.6	-	μs
SCL setup time for Stop condition	t_{st3}	0.6	-	μs
SCL hold time for Start condition	t_{hd1}	0.6	-	μs
SDA setup time	t_{st2}	0.1	-	μs
SDA hold time	t_{hd2}	0	-	μs

GT911 supports two I^2C slave addresses: 0xBA/0xBB and 0x28/0x29. The host can select the address by changing the status of Reset and INT pins during the power-on initialization phase. See the diagram below for configuration methods and timings:

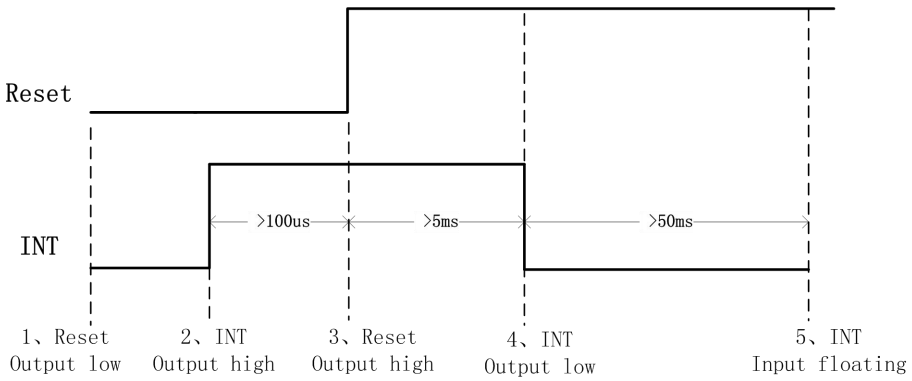
Power-on Timing:



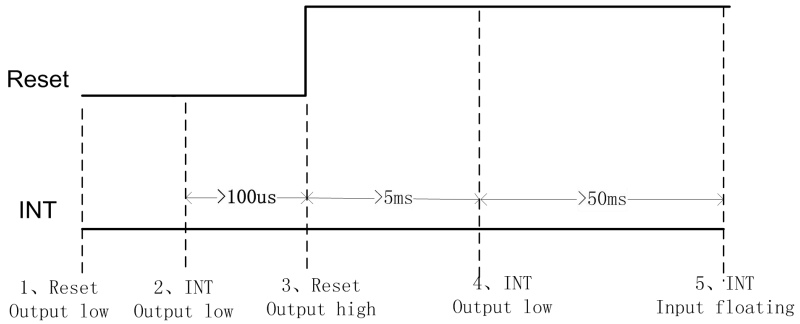
Timing for host resetting GT911:



Timing for setting slave address to 0x28/0x29:



Timing for setting slave address to 0xBA/0xBB:



a) Data Transmission

(For example：device address is 0xBA/0xBB)

Communication is always initiated by the host. Valid Start condition is signaled by pulling SDA line from “high” to “low” when SCL line is “high”. Data flow or address is transmitted after the Start condition.

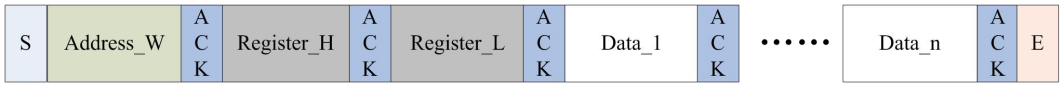
All slave devices connected to I 2 C bus should detect the 8-bit address issued after Start condition and send the correct ACK. After receiving matching address, GT911 acknowledges by configuring SDA line as output port and pulling SDA line low during the ninth SCL cycle. When receiving unmatched address, namely, not 0XBA or 0XBB, GT911 will stay in an idle state.

For data bytes on SDA, each of 9 serial bits will be sent on nine SCL cycles. Each data byte consists of 8 valid data bits and one ACK or NACK bit sent by the recipient. The data transmission is valid when SCL line is “high”.

When communication is completed, the host will issue the STOP condition. Stop condition implies the transition of SDA line from “low” to “high” when SCL line is “high”.

b) Writing Data to GT911

(For example：device address is 0xBA/0xBB)



Timing for Write Operation

The diagram above displays the timing sequence of the host writing data onto GT911. First, the host issues a Start condition. Then, the host sends 0XBA (address bits and R/W bit; R/W bit as 0 indicates Write operation) to the slave device.

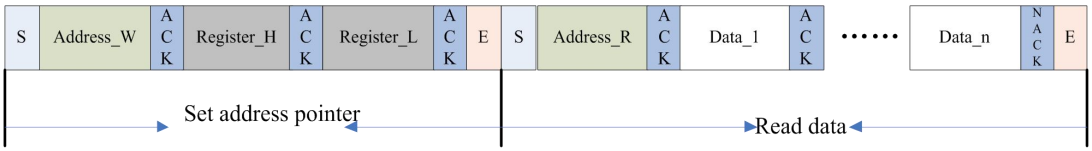
After receiving ACK, the host sends the 16-bit register address (where writing starts) and the 8-bit data bytes (to be written onto the register).

The location of the register address pointer will automatically add 1 after every Write Operation.

Therefore, when the host needs to perform Write Operations on a group of registers of continuous addresses, it is able to write continuously. The Write Operation is terminated when the host issues the Stop condition.

c) Reading Data from GT911

(For example：device address is 0xBA/0xBB)



Timing for Read Operation

The diagram above is the timing sequence of the host reading data from GT911. First, the host issues a Start condition and sends 0XBA (address bits and R/W bit; R/W bit as 0 indicates Write operation) to the slave device.

After receiving ACK, the host sends the 16-bit register address (where reading starts) to the slave device. Then the host sets register addresses which need to be read.

Also after receiving ACK, the host issues the Start condition once again and sends 0XBB (Read Operation). After receiving ACK, the host starts to read data.

GT911 also supports continuous Read Operation and, by default, reads data continuously. Whenever receiving a byte of data, the host sends an ACK signal indicating successful reception. After receiving the last byte of data, the host sends a NACK signal followed by a STOP condition which terminates communication.

8 Reliability

Test Item	Content of Test	Test Condition	Note
High Temperature Storage	Endurance test applying the high storage temperature for a long time.	90°C 96hrs	2
Low Temperature Storage	Endurance test applying the high storage temperature for a long time.	-30°C 96hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	85°C 96hrs	-
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-30 °C 96hrs	1
High Temperature/ Humidity Operation	The module should be allowed to stand at 60°C,90%RH max, for 96hrs under no-load condition excluding the polarizer. Then taking it out and drying it at normal temperature.	60°C,90%RH 96hrs	1,2
Thermal Shock Resistance	The sample should be allowed stand the following 10 cycles of operation	-30°C/85°C 20 cycles	-

Note1: No dew condensation to be observed.

Note2: The function test shall be conducted after 4 hours storage at the normal. Temperature and humidity after remove from the rest chamber.

9 Warranty and Conditions

http://www.displaymodule.com/pages/faq HYPERLINK "http://www.displaymodule.com/pages/faq"