

EEEE-520-01L1, Design of Digital Systems Tech Memo: Project 2

To: Dr. Mark Indovina

From: Isaac Witlin

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Date: Due: 11/5/2018

Re: Project 2: Hierarchical Cell Design

1 Abstract

Project 2 intends to introduce and apply the development of a hierarchical cell. This cell is a 16 bit adder attached to a 50-bit boundary scan cell for testing the 16 bit adder. More standard cells were created to implement larger cells using auto place and route tools to simplify the development of the final cell. This does not mean that significant cell layout planning didn't need to be implemented to allow the place and route tools to work effectively enough to reach a final design. The final design was also manually instantiated in the quarter pad frame cell. Timing and functional data was collected for each new cell. All cells are fully functional and the timing data matched the trends found in Project 1.

2 Theory

A total of nine new cells were created in project 2. The first cell created was a D Flip Flop (DFFX1) with a two phase non-overlapping clock. The DFFX1 was a flat cell designed via the same process as all cells created in Project 1. The second cell created as a Full Adder (FA) cell designed hierarchically, but the cell remained a standard height with I/O located within the cell (rather than on a side with a lot of spacing from the center). In addition the P&R boundary was located in the same general space as the cells in project 1 to allow proper auto placement in larger cells. A boundary scan cell (BSC) was also designed in a similar fashion. The fourth cell was a 16-bit Full Adder (ADD16) which did consist of upper and lower spacing for pin-outs and large 30λ vertical VDD and VSS rails along with multiple rows of standard cell height cells. A 50-bit Boundary Scan Cell (BSR50) was created in a similar manor. The BSR50 and the ADD16 cells were then instantiated in one main hierarchical cell (BSSUM) where the ADD16 was tied to the higher 16 bit I/O of the BSR50. The remaining BSR50 inputs where tied low or high with standard cells (TIHI, TILOW) created based off of project 1's INVX1. BSSUM was then instantiated into the BSTEST cell which placed it inside a quarter pad frame.

2.1 Simulation

The DFFX1, FA, BSC, TIHI and TILOW were all tested using methods from project one. The ADD16, BSR50, and BSSUM cells required more advanced Verilog based testing to prove they were fully operational. These testbenches were copied from handouts provided.

2.1.1 Testing The D Flip Flop

The DFFX1 cell required additional testing to determine its minimum guard time and minimum pulse width for effective operation. This was performed using a Verilog test bench. For the guard time a set period for all three input signals (D, Phi1, and Phi2) was determined and the positioning of the pulse of Phi 2 was varied by incrementing and decrementing two delay conditions that make up the pulse position. Some trial and error was required to iterate over an appropriate range of values to determine the minimum guard time. A similar process was used for determining the minimum pulse width for both Phi1 and Phi2, only delay conditions that controlled pulse width were varied.

2.2 Layout

Hierarchical cells are developed by using automatic place and route tools provided by Cadence. To start with place and route, the total cell size is defined as well as all the I/O pins metal attribute for the selected cell derived from the symbol. Then another place and route boundary is defined to limit the space where cells can actually be auto placed into an arrangement. Here the operator can enter how many VDD/VSS rails (how many rows) a cell will have. The width between each VDD and VSS rail is defined by the standard cell library (about 1.9 μm). Once the standard cell height cells are placed within the appropriate rows the operator can optimize pin placement on the cells to match and specified requirements. In Project 2 all I/O pins had to be placed on vertical metal layers, therefore I/O pins can only be placed on either the top or bottom of the cell. Once pin optimization is complete the cells can be routed using the auto route tool.

For project two the router had to interlace all metal layers such that metal 2 can only be vertical and metal 3 can only be horizontal, switching between the two up to metal 10. Metal 11 was not used in project 2 because it was too large, in general anything beyond Metal 4 was excessive for creating the cells in this project. To counter the auto routers inability to effectively route VDD and VSS, these nets were routed manually, for smaller cells all this required was a pin placement on the VDD and VSS standard cell rails. In larger cells the VDD and VSS vertical tracks were attached to each standard cell row. In larger cells adequate spacing was left on the top, bottom, left, and right to allow the cell to properly abut other larger cells and provide enough spacing for routing. In general this meant there was 8 λ tracks top and bottom of larger cells. 38 λ tracks left and right, and 16 λ tracks in between each standard cell row. Larger cells needed to have the proper amount of rows and columns to be able to fit inside the quarter pad frame cell (980x980 μm)

3 Results & Discussion

All cells were completed. To pass DRC and LVS the ADD16 cell needed some manual adjustments for Via's that the auto route tool did not place properly (used too much metal, too close to other Via's etc.). In addition the ADD16 cells needed one specific net to be routed manually because the tool would refuse to route that net. Some difficulty was countered with properly defining standard cell origin and P&R boundary so all cells would auto place correctly. In addition the width of each row was not uniform, there was spacing in between some auto placed cells, because of these issues cells were re-arranged manually. The BSR50 cell had some routing issues that caused some nets to be too close to other nets to pass DRC, nets were manually moved. There were not routing issues in the BSSUM cell and the BSTEST cell was routed manually because the auto route tool could not route to the pad frame appropriately.

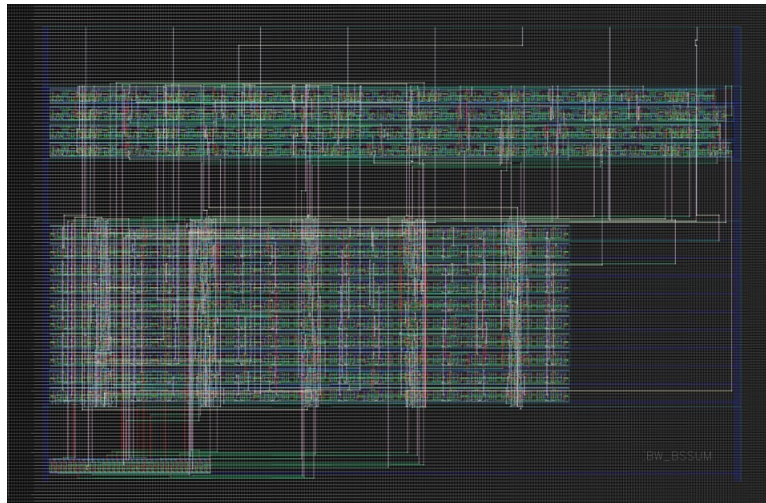


Figure 3.1: Final BSSUM Cell

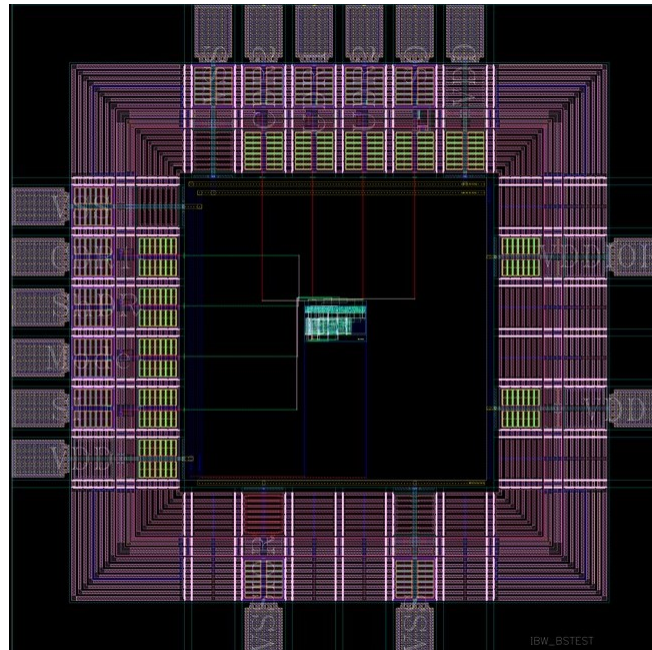


Figure 3.2: BSSUM Inside Pad Frame (BSTEST)

3.1 Timing

Rise Time (ns)	Pre Layout	Post Layout	Difference
INVX1	1.553	1.62	4.31%
INVX2	0.8448	0.8735	3.40%
NAND2X1	1.548	1.651	6.65%
NOR2X1	1.663	1.751	5.29%
TMUX2X1	1.474	1.551	5.22%
AOI22X1	0.8239	0.9225	11.97%
XOR2X1	1.645	1.817	10.46%
DFFX1	0.009135	0.01603	75.48%
FA	1.638	1.815	10.81%

Figure 3.3: Rise Time for all cells, pre & post layout, including their % difference.

Fall Time (ns)	Pre Layout	Post Layout	Difference
INVX1	1.118	1.097	-1.88%
INVX2	0.5974	0.5889	-1.42%
NAND2X1	1.166	1.111	-4.72%
NOR2X1	0.5652	0.533	-5.70%
TMUX2X1	1.055	1.01	-4.27%
AOI22X1	0.577	0.4929	-14.58%
XOR2X1	1.174	0.9997	-14.85%
DFFX1	0.007795	0.013	66.77%
FA	1.146	0.9755	-14.88%

Figure 3.4: Fall Time for all cells, pre & post layout, including their % difference.

Propagation Delay Rise Time (ns)	Input 1	Input 2	Input 3	Input 4	Input 5	Input 6
INVX1 Pre	1.14					
INVX1 Post	1.177					
INVX2 Pre	0.629					
INVX2 Post	0.6481					
NAND2X1 Pre	1.145	1.14				
NAND2X1 Post	1.206	1.201				
NOR2X1 Pre	1.257	1.244				
NOR2X1 Post	1.312	1.299				
TMUX2X1 Pre	0.8176	0.8188	0.02595			
TMUX2X1 Post	0.8355	0.8362	0.02598			
AOI22X1 Pre	0.9262	0.9175	0.9976	0.9987		
AOI22X1 Post	1.012	1.015	1.086	1.093		
XOR2X1 Pre	1.255	1.253				
XOR2X1 Post	1.388	1.39				
DFFX1 Pre	0.08508	0.05267				
DFFX1 Post	0.1253	0.06838				
FA Pre	1.151	1.29	1.157	1.294	1.151	1.26
FA Post	1.237	1.447	1.234	1.453	1.232	1.408

Figure 3.5: Propagation Delay Rise Time for all cells, pre & post layout

Propagation Delay Fall Time (ns)	Input 1	Input 2	Input 3	Input 4	Input 5	Input 6
INVX1 Pre	0.8084					
INVX1 Post	0.8011					
INVX2 Pre	0.4473					
INVX2 Post	0.4415					
NAND2X1 Pre	0.8801	0.8767				
NAND2X1 Post	0.85	0.8543				
NOR2X1 Pre	0.8156	0.8134				
NOR2X1 Post	0.774	0.7809				
TMUX2X1 Pre	0.658	0.6563	-0.02442			
TMUX2X1 Post	0.6376	0.6362	-0.02444			
AOI22X1 Pre	0.8844	0.8911	0.8871	0.8897		
AOI22X1 Post	0.7471	0.7594	0.7572	0.7638		
XOR2X1 Pre	0.9064	0.9029				
XOR2X1 Post	0.7851	0.8003				
DFFX1 Pre	0.07404	0.06222				
DFFX1 Post	0.1031	0.08835				
FA Pre	0.9473	0.9243	0.9457	0.9283	0.8979	0.8895
FA Post	0.9789	0.836	0.9946	0.8424	0.8896	0.7627

Figure 3.6: Propagation Delay Fall Time for all cells, pre & post layout

Propagation Delay Rise Time	Difference (Input 1)	Difference (Input 2)	Difference (Input 3)	Difference (Input 4)	Difference (Input 5)	Difference (Input 6)
INVX1 Pre	3.25%					
INVX1 Post						
INVX2 Pre	3.04%					
INVX2 Post						
NAND2X1 Pre	5.33%	5.35%				
NAND2X1 Post						
NOR2X1 Pre	4.38%	4.42%				
NOR2X1 Post						
TMUX2X1 Pre	2.19%	2.13%	0.12%			
TMUX2X1 Post						
AOI22X1 Pre	9.26%	10.63%	8.86%	9.44%		
AOI22X1 Post						
XOR2X1 Pre	10.60%	10.93%				
XOR2X1 Post						
	47.27%	29.83%				
	7.47%	12.17%	6.66%	12.29%	7.04%	11.75%

Figure 3.7: Propagation Delay Rise Time % Difference, pre & post layout

Propagation Delay Fall Time	Difference (Input 1)	Difference (Input 2)	Difference (Input 3)	Difference (Input 4)	Difference (Input 5)	Difference (Input 6)
INVX1 Pre	-0.90%					
INVX1 Post						
INVX2 Pre	-1.30%					
INVX2 Post						
NAND2X1 Pre	-3.42%	-2.56%				
NAND2X1 Post						
NOR2X1 Pre	-5.10%	-4.00%				
NOR2X1 Post						
TMUX2X1 Pre	-3.10%	-3.06%	0.08%			
TMUX2X1 Post						
AOI22X1 Pre	-15.52%	-14.78%	-14.64%	-14.15%		
AOI22X1 Post						
XOR2X1 Pre	-13.38%	-11.36%				
XOR2X1 Post						
	39.25%	42.00%				
	3.34%	-9.55%	5.17%	-9.25%	-0.92%	-14.26%

Figure 3.8: Propagation Delay Fall Time % Difference, pre & post layout

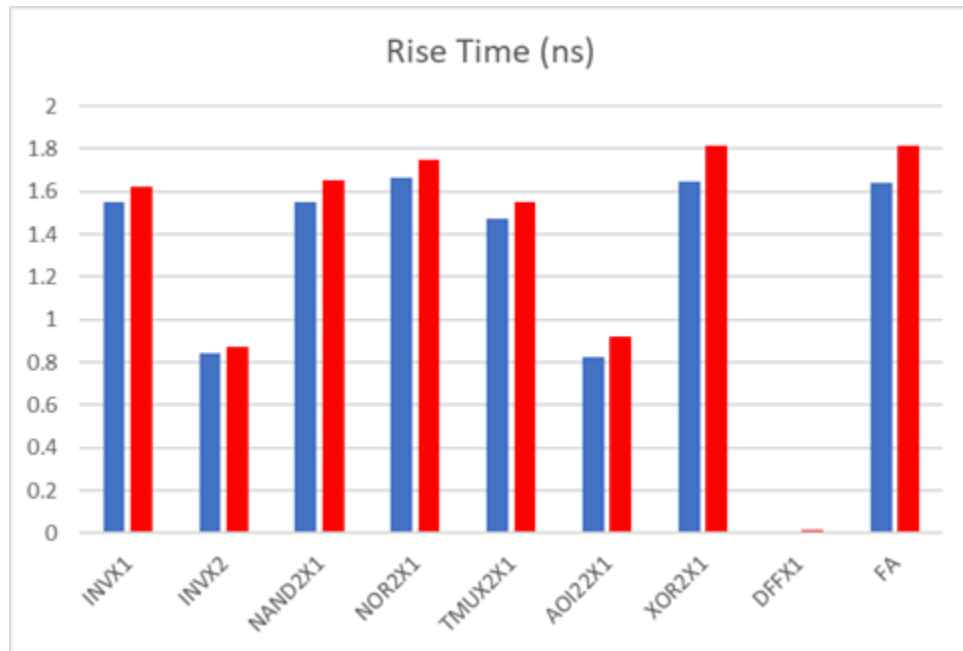


Figure 3.8: Rise Time for all cells, pre & post layout bar graph. (pre is marked blue and post is marked red)

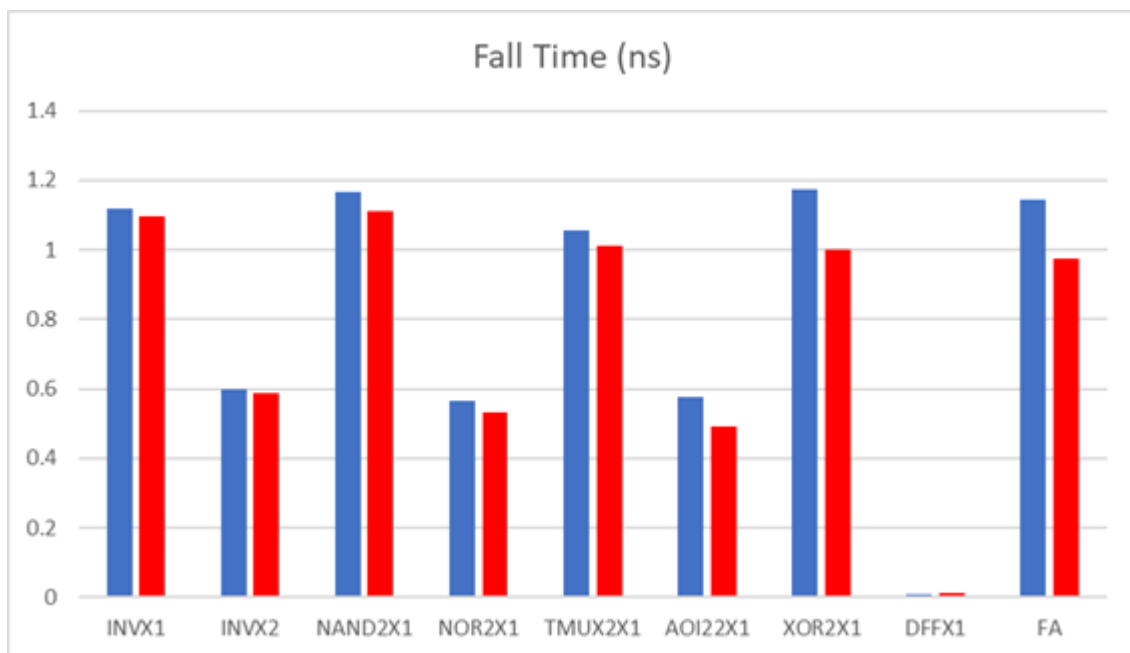


Figure 3.10: Fall Time for all cells, pre & post layout bar graph. (pre is marked blue and post is marked red)

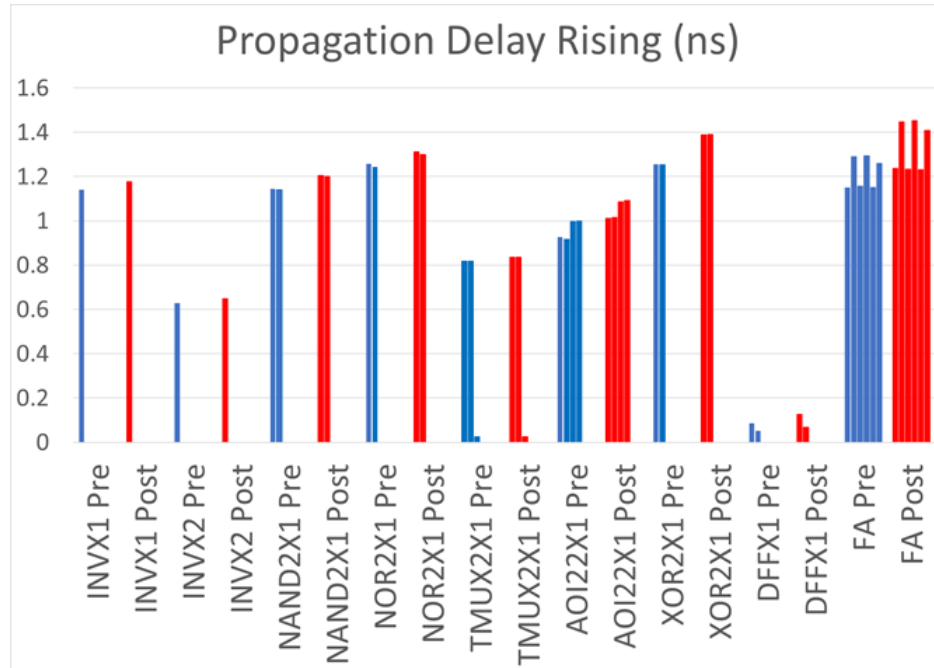


Figure 3.11: Propagation Delay Rise Time, pre & post layout bar graph. (output 1-4 from left to right, pre is marked blue and post is marked red)

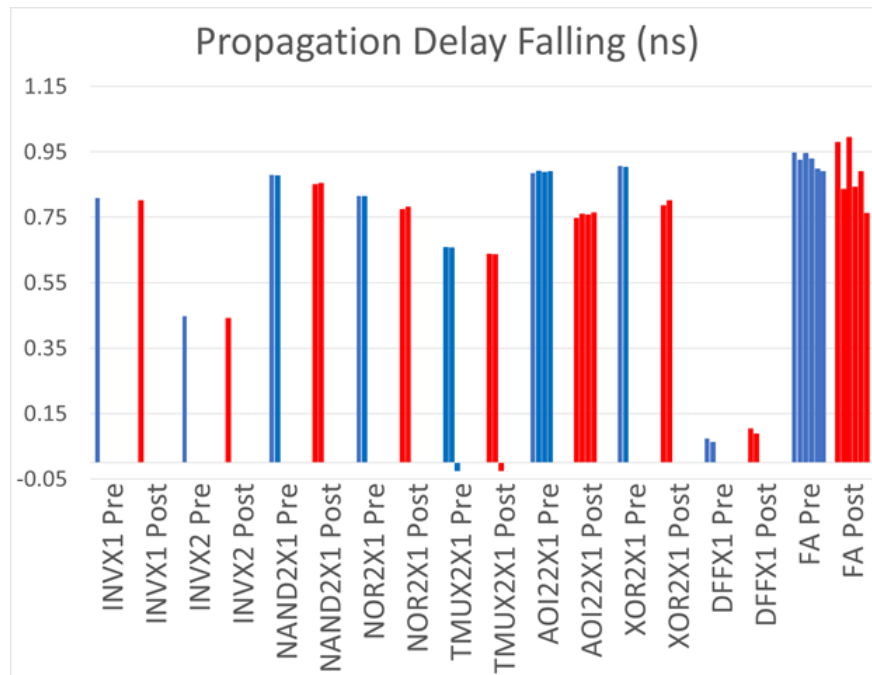


Figure 3.11: Propagation Delay Fall Time, pre & post layout bar graph. (output 1-4 from left to right, pre is marked blue and post is marked red)

3.1.1 DFFX1 Guard Time and Minimum Pulse Width

Through trial and error three Verilog testbench tests were performed to determine the Guard Time, and Minimum Pulse width for Phi1 and Phi2 by measuring results from the output waveforms. The Guard Time for the DFFX1 was determined to be -532ps, at which point the input of the data coming in is fully transparent to the output. The minimum pulse width for Phi1 and Phi2 was 15ps and 17ps respectively, at which point the Flip Flop no longer operates.



Figure 3.12: Phi1 Minimum Pulse Width Waveform

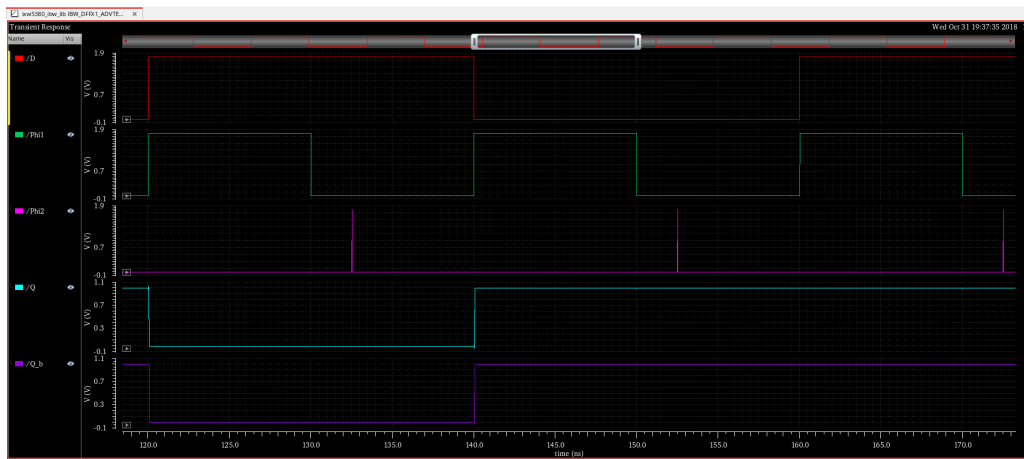


Figure 3.13: Phi2 Minimum Pulse Width Waveform

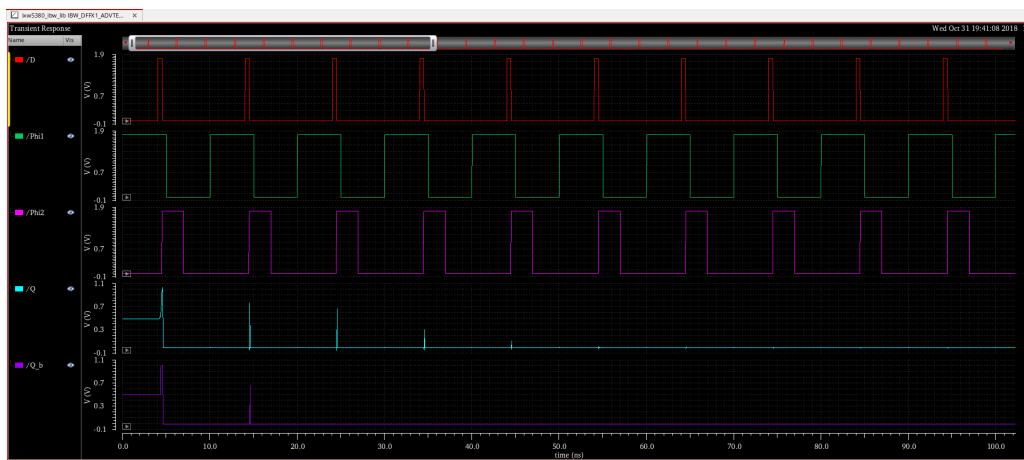


Figure 3.13: Minimum Guard Time Waveform

4 Conclusion

With more time, a smaller, faster cell that uses less metal layers could be developed by further optimizing in the planning stage of each cell design. The auto route tool, even when things are optimized will sometimes make mistakes that will need to be manually adjusted. To mitigate this its possible to increase the area that the auto route tool is given to route on. If the spacing of each

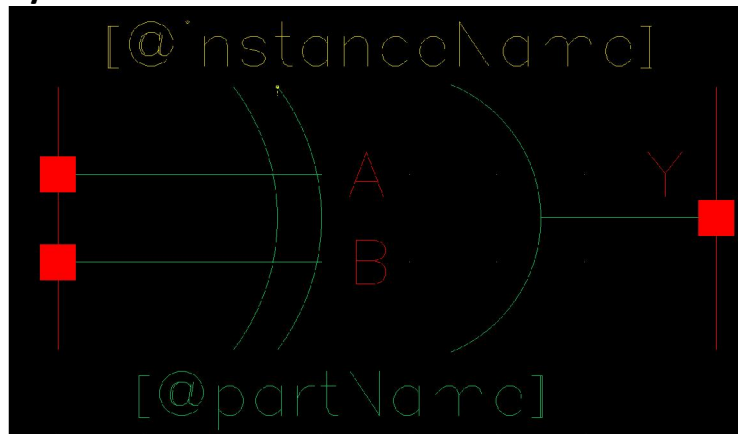
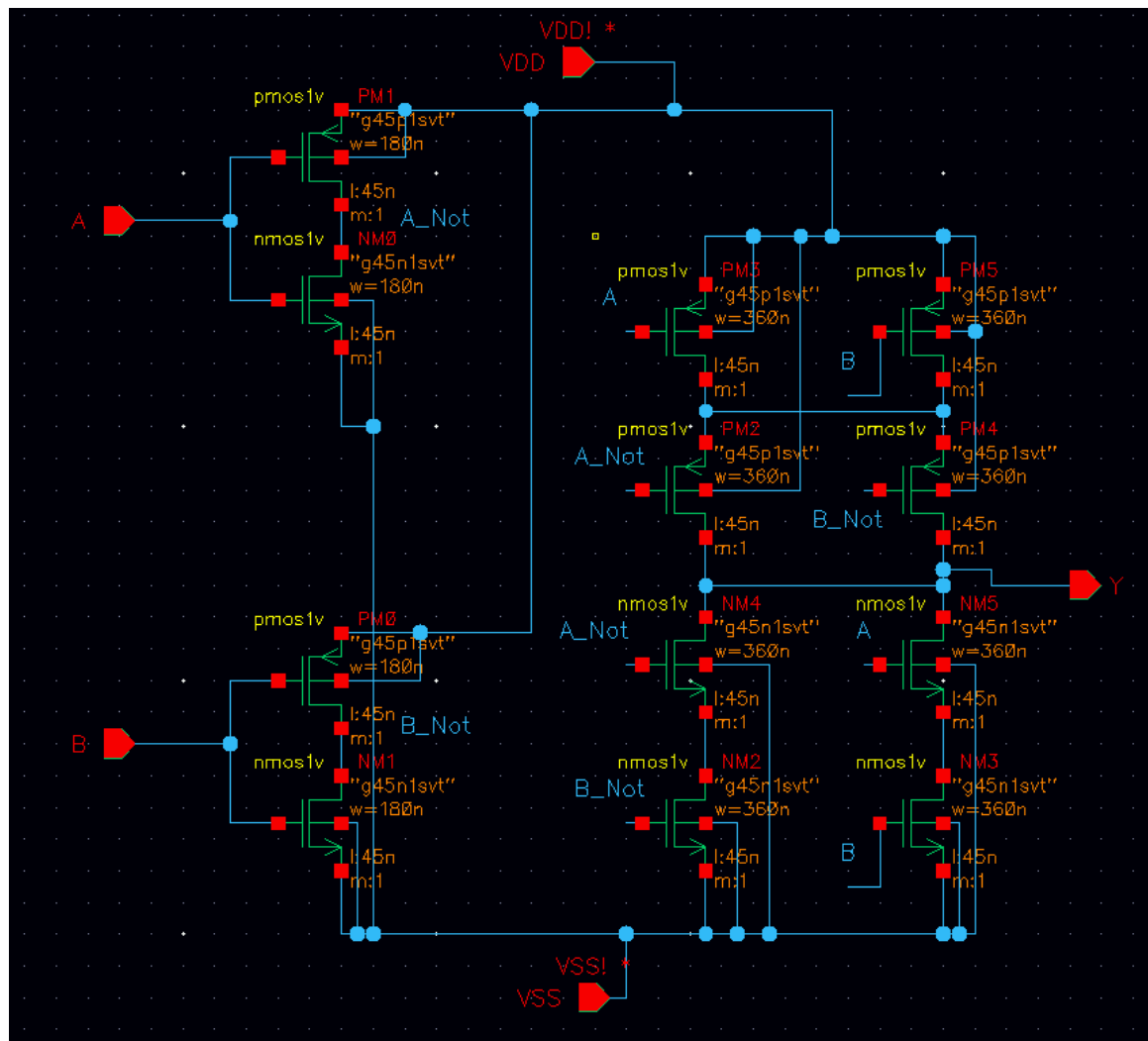
standard cell row in the BSR50 was greater than 16 λ tracks then the auto route tool probably would not have spacing issues with its nets. To reduce routing compute time and complexity it was also necessary to ensure all standard cell VDD and VSS rails were inside proper 8 λ tracks. The timing data produced expected results that conform with the trend in the cells in project 1, because each cell is skewed low the falling is always faster than the rising delay. The DFFX1 Guard Time, and Minimum Pulse Width measurements could have been more robust and automated to allow easier data collection. The DFFX1 minimum pulse width calculation was measured at the first DFFX1 failure, not when the propagation delay from normalized to measured of the clock and output is greater than 10%. The DFFX1 did not have properly aligned 8 λ track I/O pins, this would impact auto routing for the creation of larger cells, because I did not encounter any issues, the cell was not re-worked, because doing so would require a redesign of the BSC and BSR50 cells.

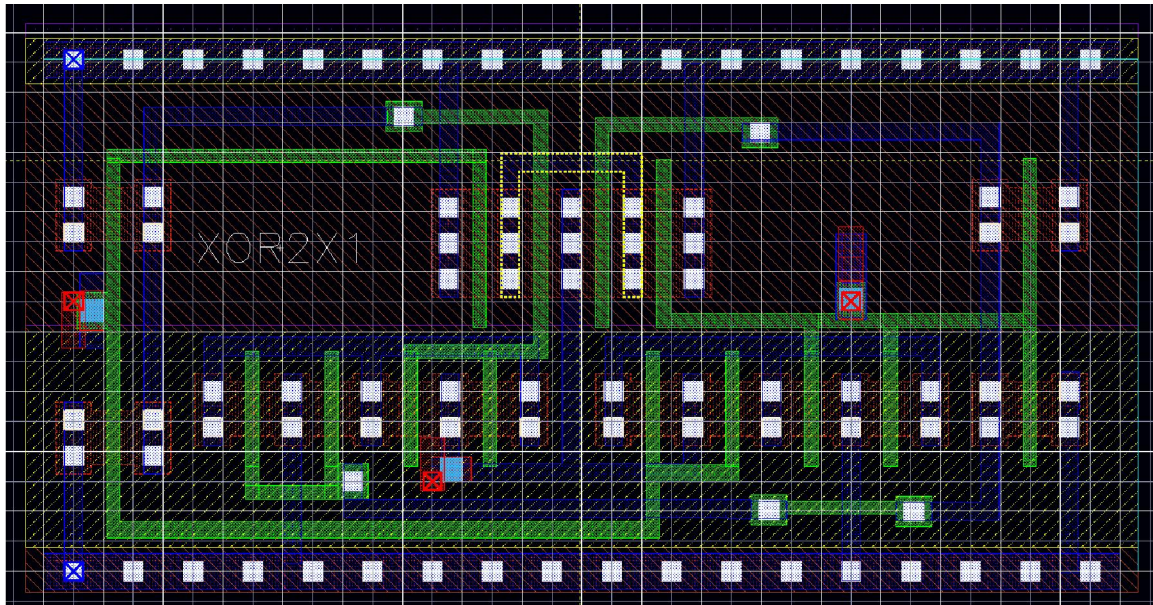
5 Appendices

5.1 Cell Datasheets

Attached on the next page are all cell data sheets. The final page of this document is after all included data sheets.

Library Name:		ixw5380_ibw_lib
Cell Name:		IBW_XOR2X1
Function/Truth Table:		
A1	B0	Y
0	0	0
0	1	1
1	0	1
1	1	0
Delay Calculations: (ns)		
B/Y pdr		1.388
B/Y pdf		0.7851
A/Y pdr		1.39
A/Y pdf		0.8003
Output Rise Time		1.817
Output Fall Time		0.9997
Layout Area: 7.1um²		

Symbol with Port Names:**Schematic:**

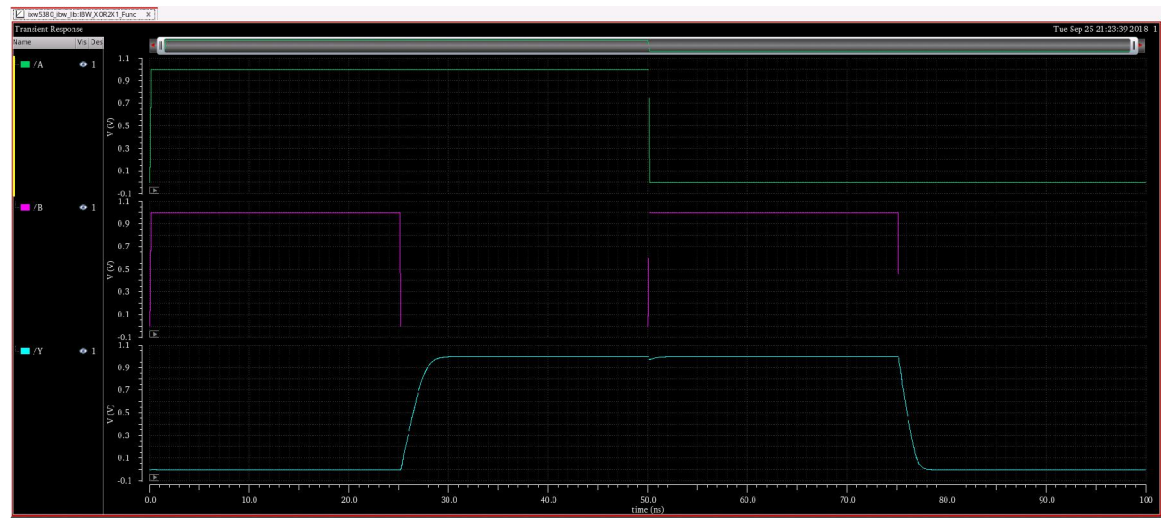
Layout:**Verilog Model:**

```
//Verilog HDL for "ixw5380_ibw_lib", "IBW_XOR2X1" "functional"

module IBW_XOR2X1 ( Y, A, B, .VDD(\VDD! ), .VSS(\VSS! ) );

    input A;
    output Y;
    input
`ifdef INCA
        (* integer inh_conn_prop_name = "VDD";
        integer inh_conn_def_value = "cds_globals.\VDD! "; *)
        \VDD! ;
    input
`ifdef INCA
        (* integer inh_conn_prop_name = "VSS";
        integer inh_conn_def_value = "cds_globals.\VSS! "; *)
        \VSS! ;
    input B;

    xor(Y, A, B);
endmodule
```

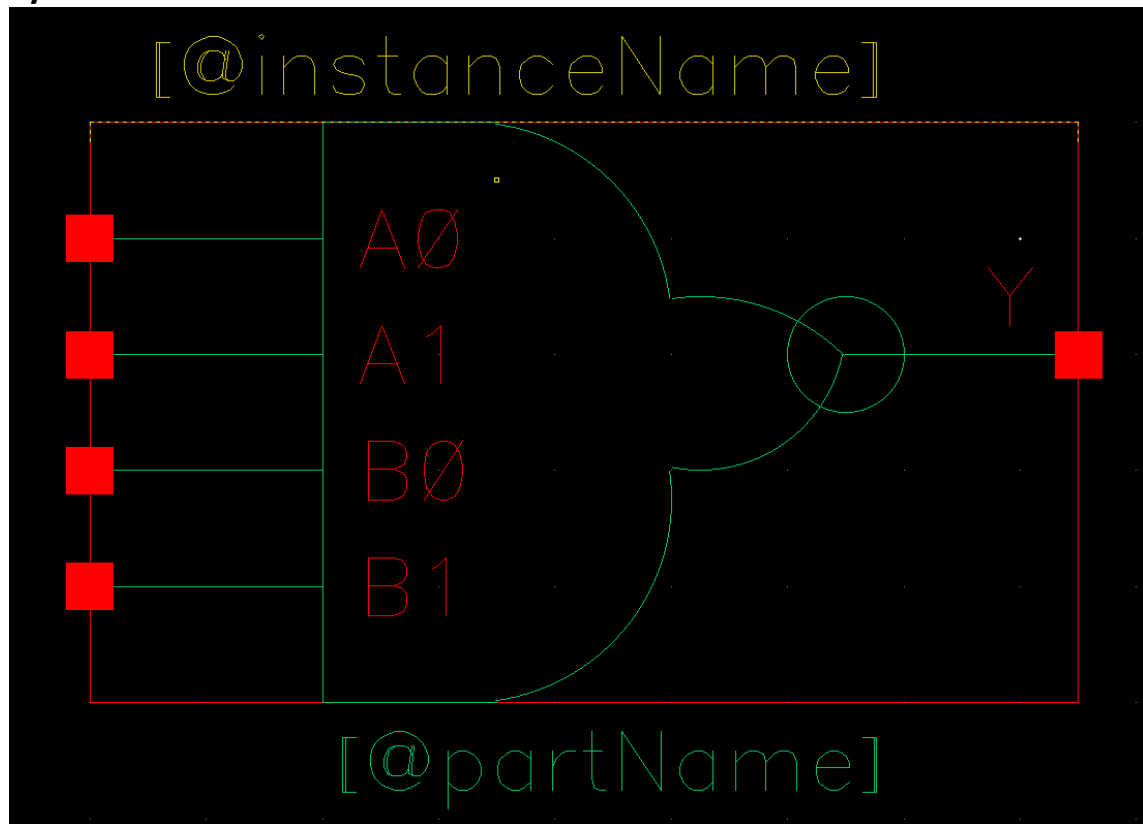
Functional Simulation Waveforms:**Comments/Notes:**

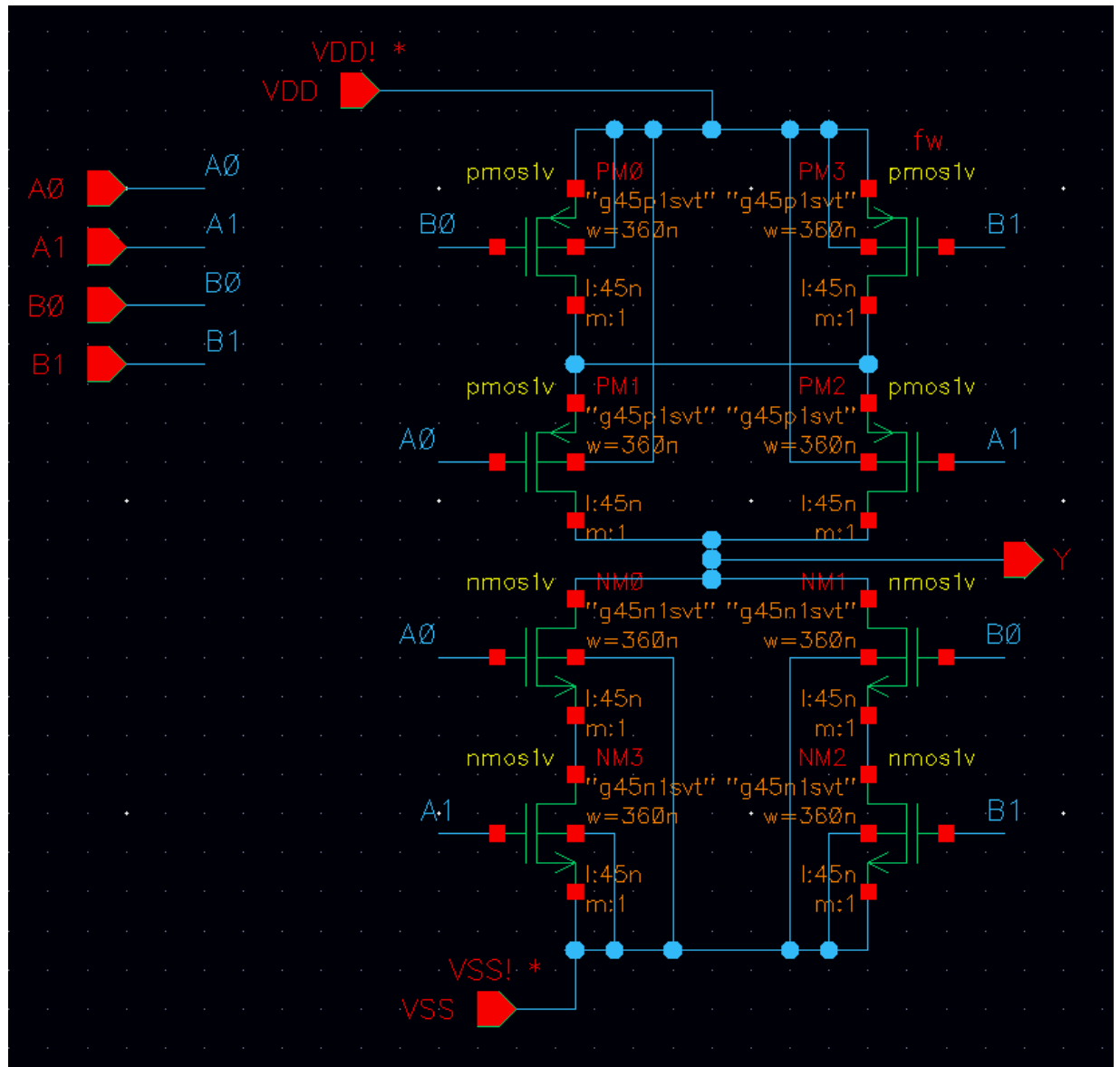
Library Name:		ixw5380_ibw_lib		
Cell Name:		IBW_AOI22X1		
Function/Truth Table:				
A0	A1	B0	B1	Y
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0
Delay Calculations: (ns)				
A0/Y pdf			0.7471	
A0/Y pdr			1.012	

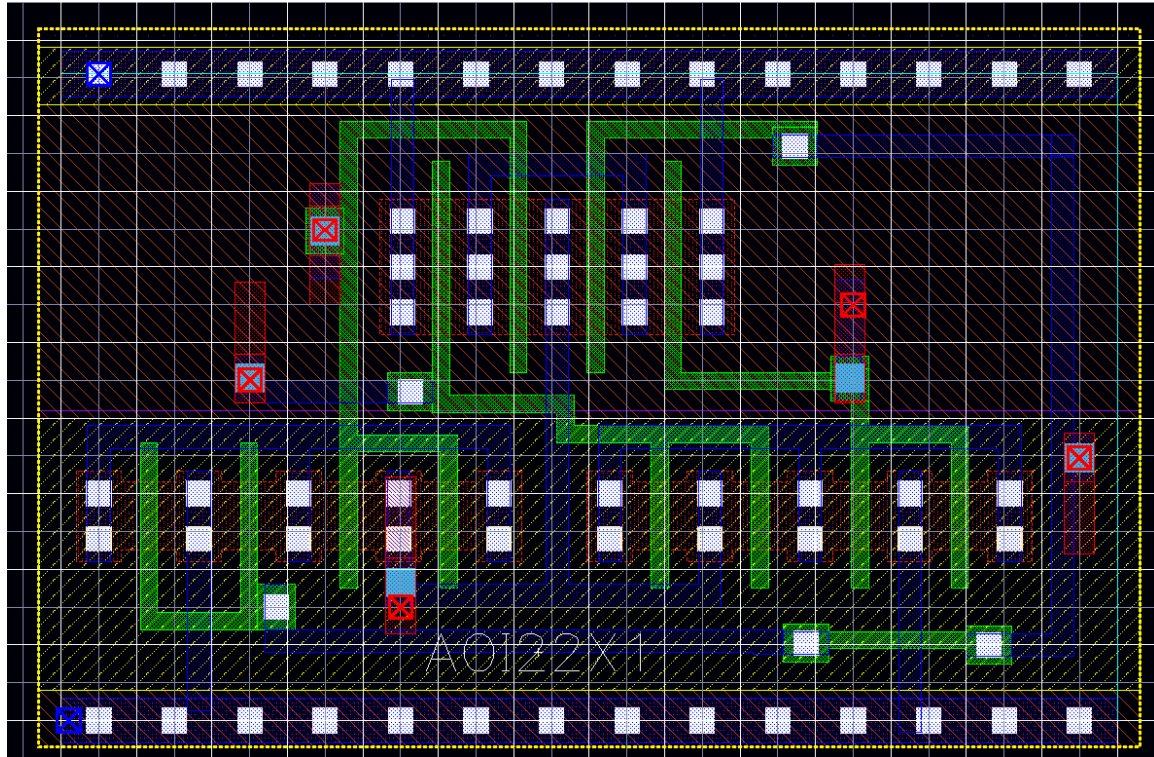
A1/Y pdf	0.7594
A1/Y pdr	1.015
B0/Y pdf	0.7572
B0/Y pdr	1.086
B1/Y pdf	0.7638
B1/Y pdr	1.093
Output Rise Time	0.9225
Output Fall Time	1.817

Layout Area: 5.6um²

Symbol with Port Names:



Schematic:

Layout:**Verilog Model:**

```
//Verilog HDL for "ixw5380_ibw_lib", "IBW_A0I22X1" "functional"

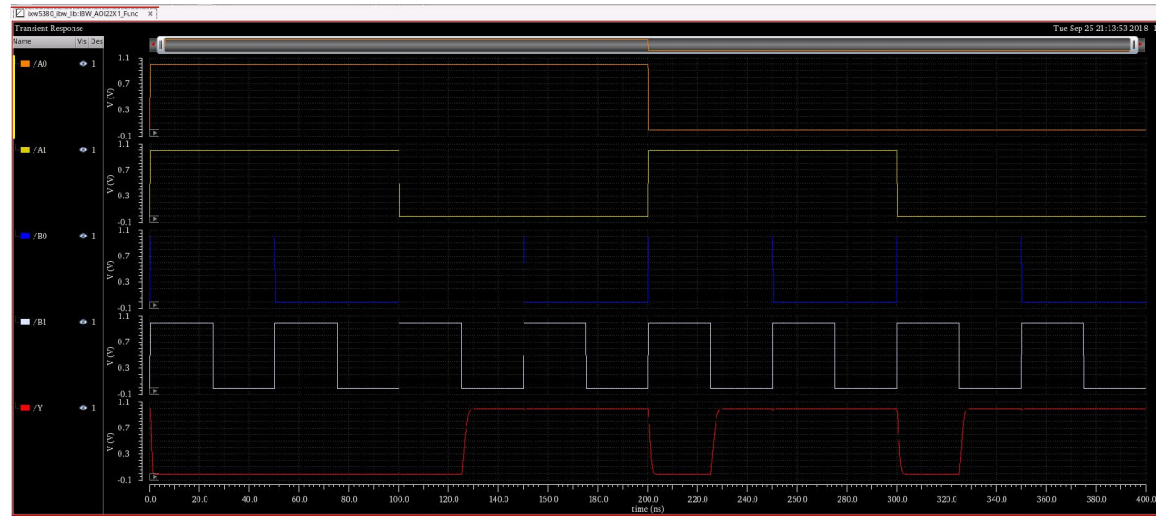
module IBW_A0I22X1 ( Y, A0, A1, B0, B1, .VDD(\VDD! ), .VSS(\VSS! ) );

    input A0;
    output Y;
    input
`ifdef INCA
    (* integer inh_conn_prop_name = "VDD";
    integer inh_conn_def_value = "cds_globals.\VDD! "; *)
`endif
    \VDD! ;
    input B0;
    input B1;
    input A1;
    input
`ifdef INCA
    (* integer inh_conn_prop_name = "VSS";
    integer inh_conn_def_value = "cds_globals.\VSS! "; *)
`endif
    \VSS! ;

    wire N0;
    wire N1;

    and(N0,A0,A1);
    and(N1,B0,B1);
    nor(Y,N0,N1);

endmodule
```

Functional Simulation Waveforms:**Comments/Notes:**

Library Name:		ixw5380_ibw_lib		
Cell Name:		IBW_DFFX1		
Function/Truth Table:				
Phi1	Phi2	D	Q	Q_Not
1	0	1	X	X
0	1	1	X	X
1	0	X	1	0
0	1	X	1	0
1	0	0	X	X
0	1	0	X	X
1	0	X	0	1
0	1	X	0	1
Delay Calculations: (ns)				
Phi1/Q pdf			.103	
Phi1/Q pdr			.125	
Phi1/Q_Not pdf			.068	
Phi1/Q_Not pdr			.088	
Guard Time			0.532	
Phi1 Minimum Pulse Width			0.15	
Phi2 Minimum Pulse Width			.017	
Output Rise Time			.016	
Output Fall Time			.013	
Layout Area: 10.1 um²				

Verilog Model:

```
//Verilog HDL for "ixw5380_ibw_1ib", "IBW_DFFX1" "functional"

module IBW_DFFX1 ( Q, Q_Not, D, Phi1, Phi2, .VDD(\VDD! ), .VSS(\VSS! ) );

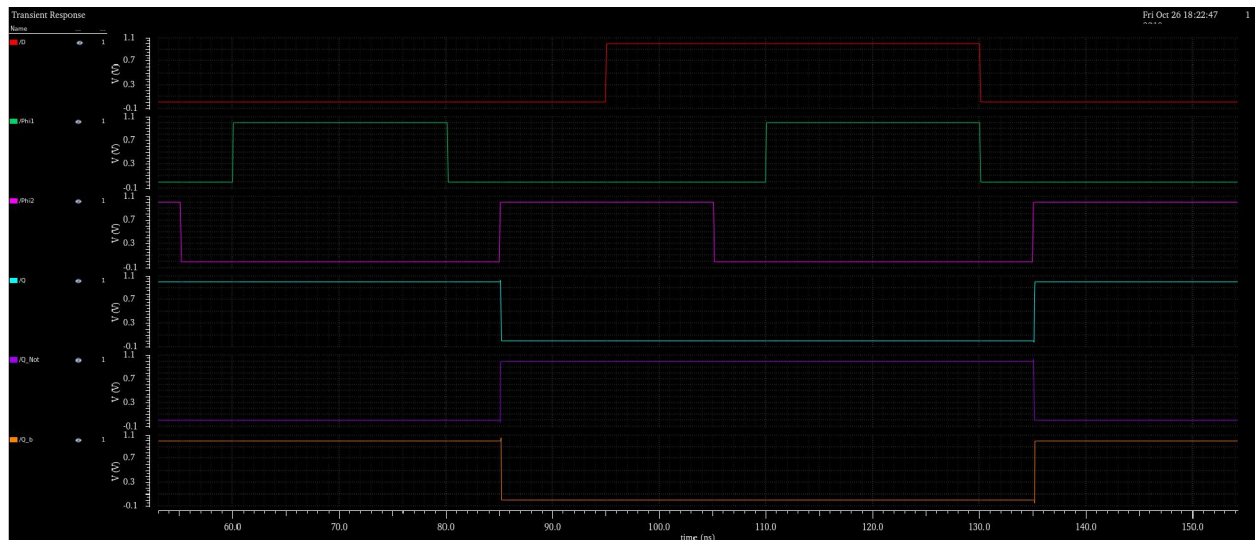
    input
    `ifdef INCA
        (* integer inh_conn_prop_name = "VDD";
         integer inh_conn_def_value = "cds_globals.\VDD! "; *)
        \VDD! ;
    input Phi2;
    output Q;
    input

    `ifdef INCA
        (* integer inh_conn_prop_name = "VSS";
         integer inh_conn_def_value = "cds_globals.\VSS! "; *)
        \VSS! ;
    input Phi1;
    input D;
    output Q_Not;

    wire A1, A2, B1, B2, Y1, Y2, nS1, S1, nS2, S2, R;

    not U1(A1, D);
    and U2(f1, A1, nS1),
        U3(f2, A2, S1);
    or U4(Y1, f1, f2);
    not U5(nS1,S1);
    not U6(B1, Y1);
    not U7(A2, B1);
    and U8(f3, B1, nS2),
        U9(f4, B2, S2);
    or U10(Y2, f3, f4);
    not U11(nS2,S2);
    not U12(B2,R);
    not U13(R,Y2);
    not U14(Q_Not, Y2);
    not U15(Q,R);

endmodule
```

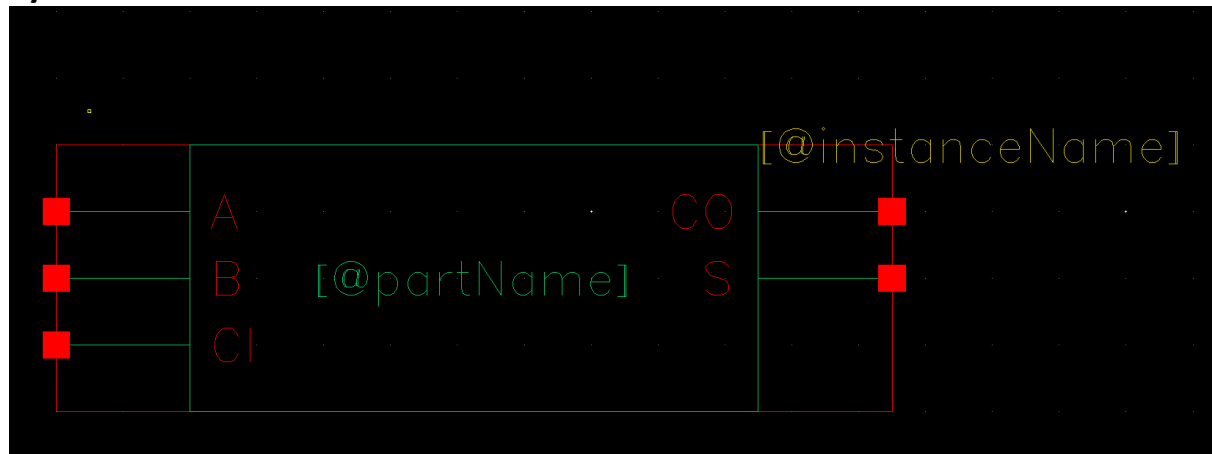
Functional Simulation Waveforms:

Library Name:		ixw5380_ibw_lib		
Cell Name:		IBW_FA		
Function/Truth Table:				
A	B	Cin	Cout	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1
Delay Calculations: (ns)				
A/S pdf			.836	
A/S pdr			1.45	
B/S pdf			.842	
B/S pdr			1.45	
CI/S pdf			.763	
CI/S pdr			1.41	
A/CO pdf			.978	
A/CO pdr			1.24	
B/CO pdf			.995	
B/CO pdr			1.23	

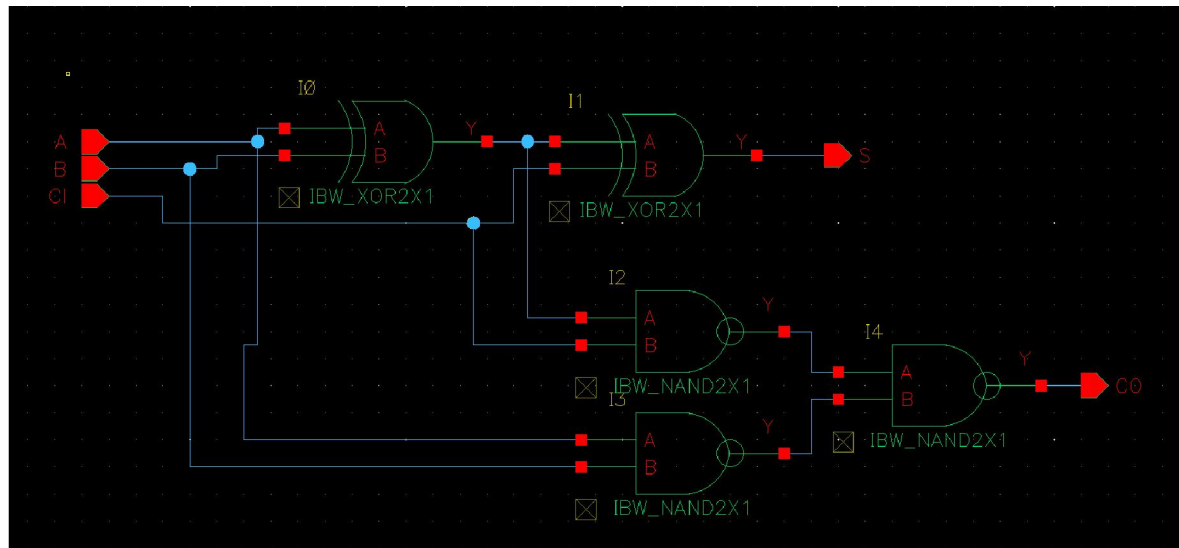
CI/CO pdf	.890
CI/CO pdr	1.41
Output Rise Time	1.82
Output Fall Time	.976

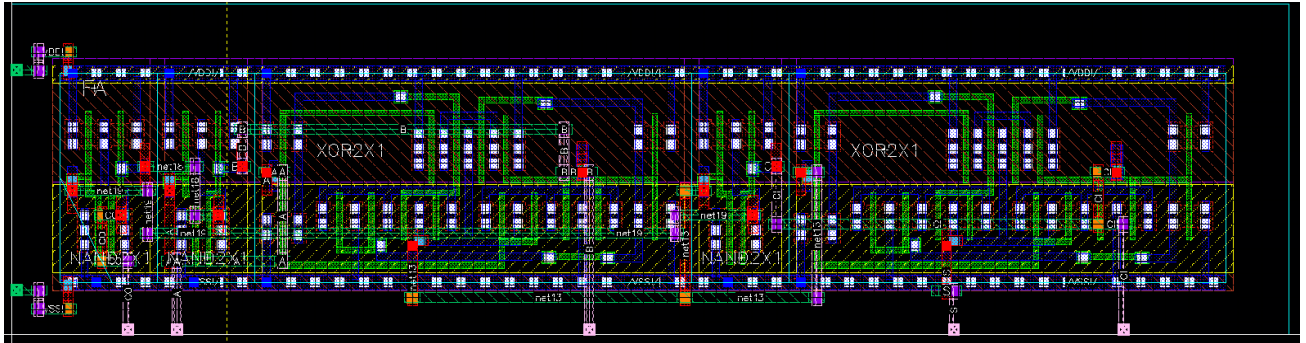
Layout Area: 18.5 μm^2

Symbol with Port Names:



Schematic:



Layout:**Verilog Model:**

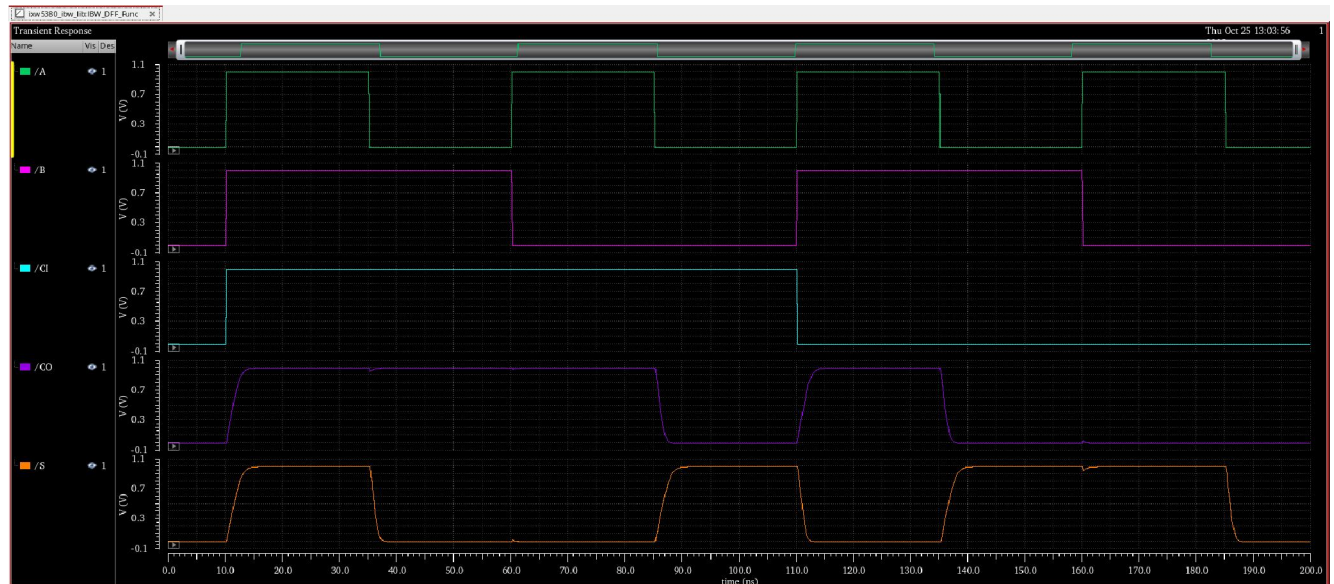
```
//Verilog HDL for "ixw5380_ibw.lib", "IBW_FA" "functional"

module IBW_FA ( CO, S, A, B, C1 );

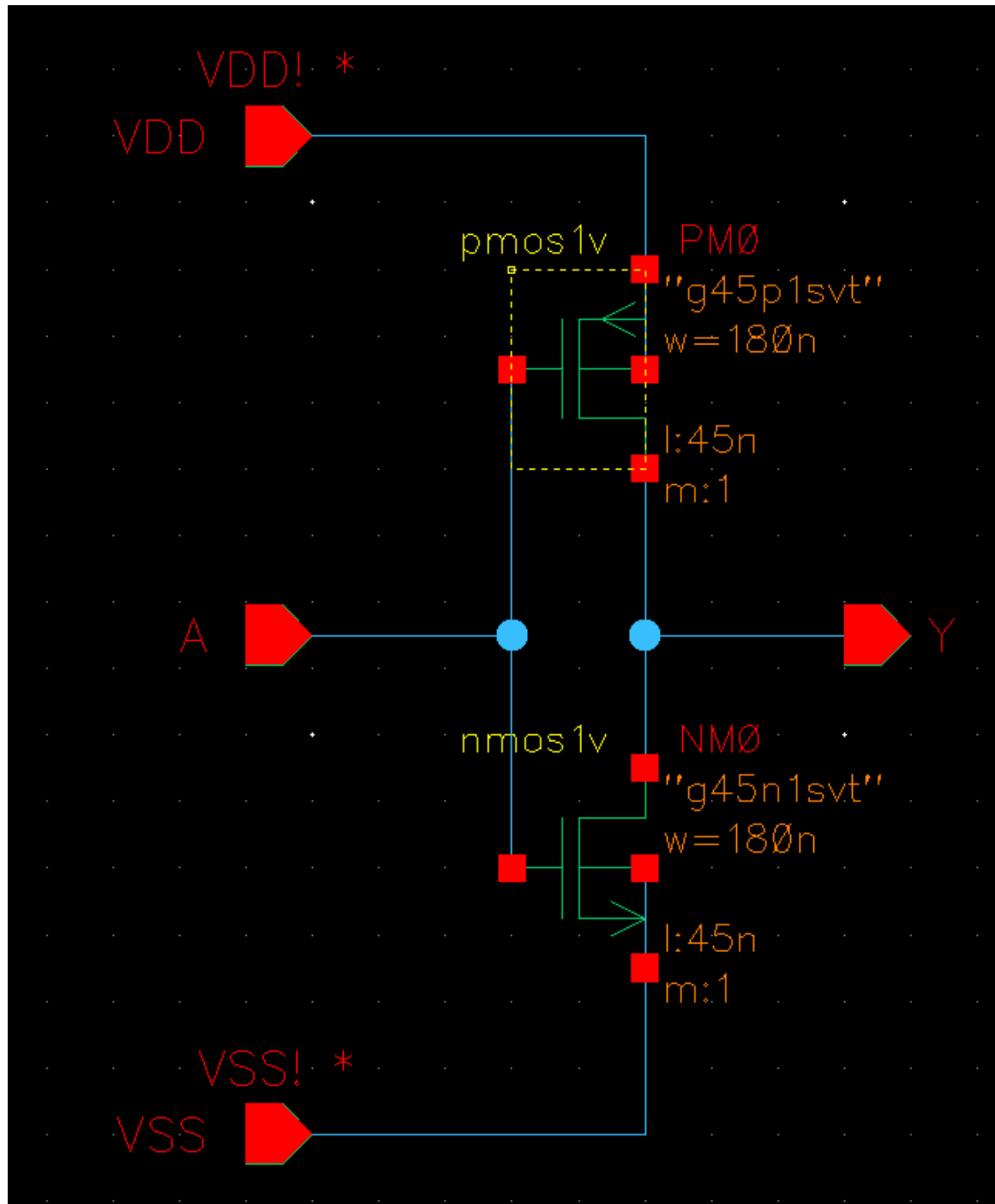
    input A;
    output CO;
    input C1;
    output S;
    input B;

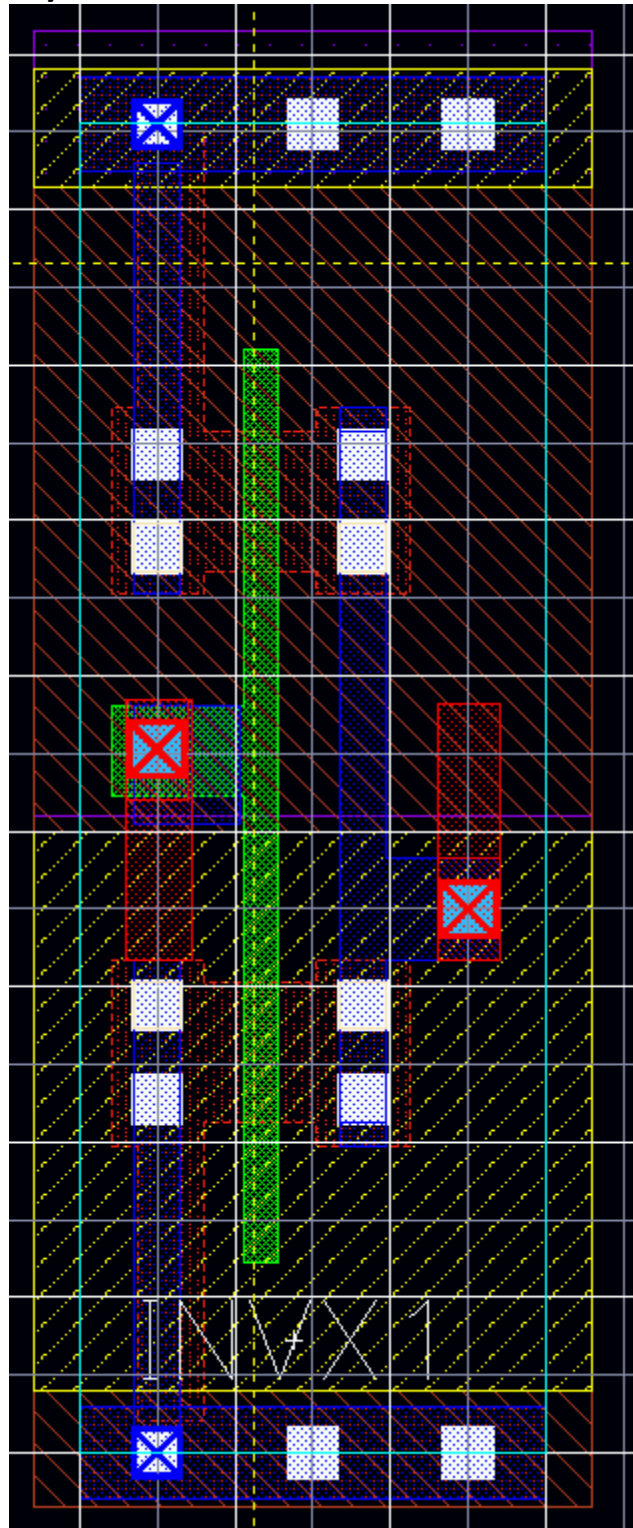
    wire x1, n1, n2;

    xor U1(x1,A,B);
    xor U2(S,x1,C1);
    nand U3(n1,x1,c1);
    nand U4(n2,A,B);
    nand U5(CO,n1,n2);
endmodule
```

Functional Simulation Waveforms:

Library Name:	ixw5380_ibw_lib	
Cell Name:	IBW_INVX1	
Function/Truth Table:		
A	Y	
1	0	
0	1	
Delay Calculations: (ns)		
Propagation Delay Falling	0.8084	
Propagation Delay Rising	1.14	
Output Rise Time	1.62	
Output Fall Time	1.097	
Layout Area: 1.4 um ²		
Symbol with Port Names:		
<		

Schematic:

Layout:

Verilog Model:

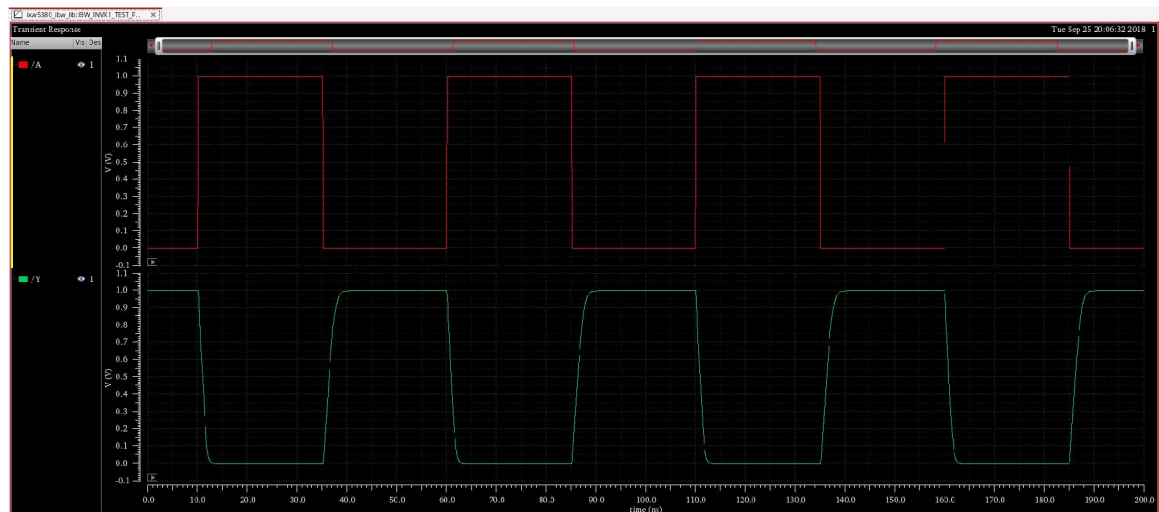
```
//Verilog HDL for "ixw5380_ibw_lib", "IBW_INVX1" "functional"

module IBW_INVX1 ( Y, A, .VDD(\VDD! ), .VSS(\VSS! ) );

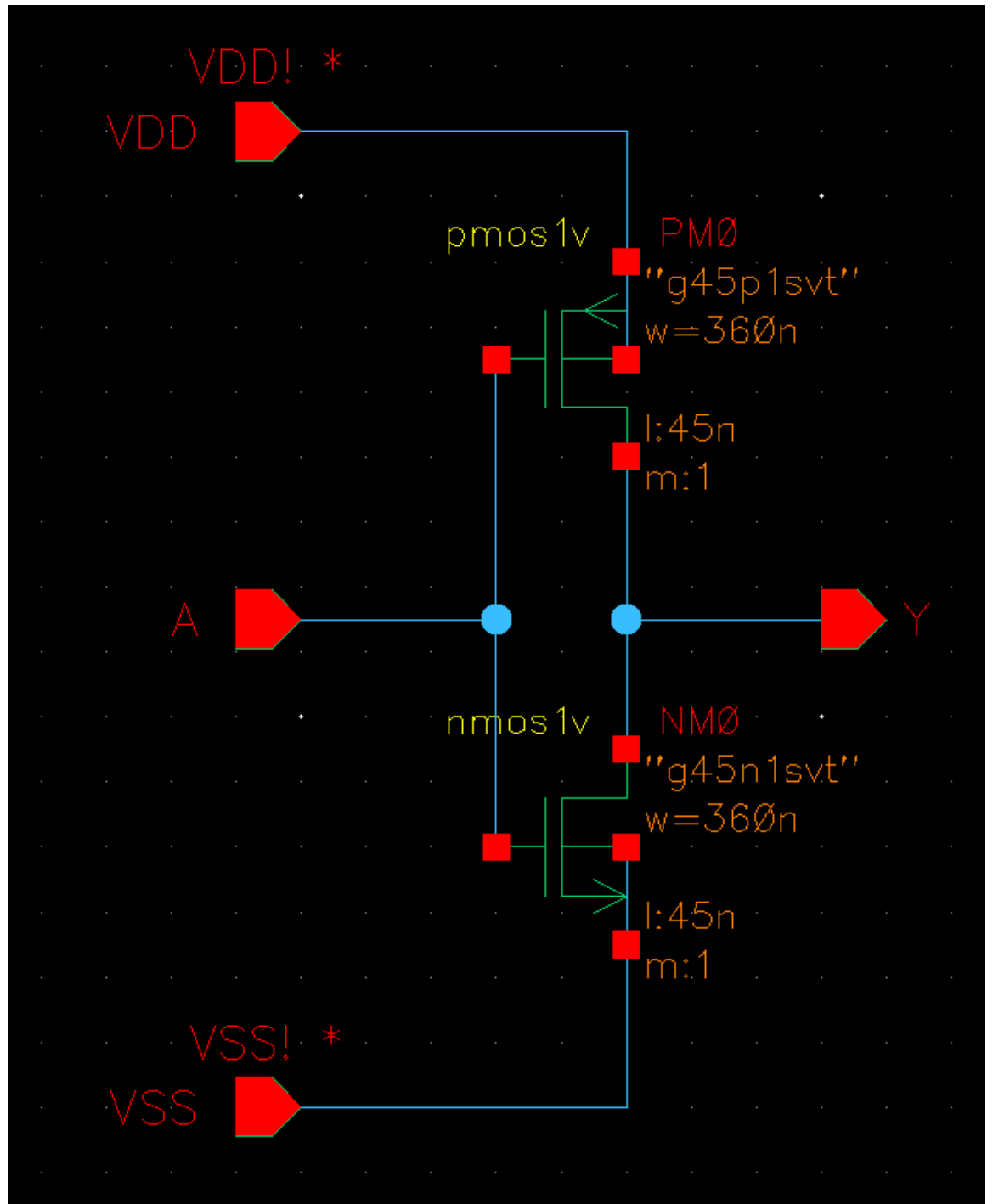
    input A;
    output Y;
    input
`ifdef INCA
        (* integer inh_conn_prop_name = "VDD";
        integer inh_conn_def_value = "cds_globals.\VDD! "; *)
        \VDD! ;
    input
`ifdef INCA
        (* integer inh_conn_prop_name = "VSS";
        integer inh_conn_def_value = "cds_globals.\VSS! "; *)
        \VSS! ;

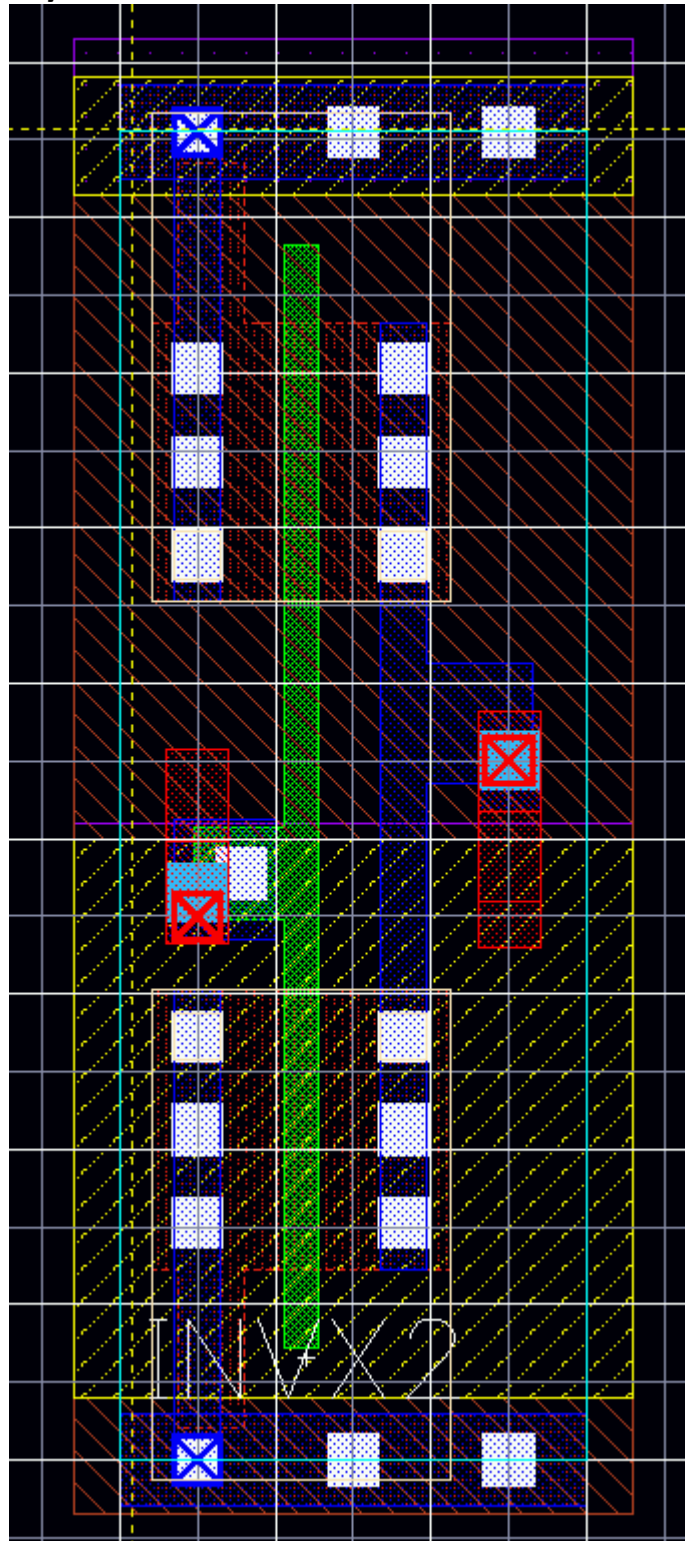
    not U1 (Y, A);

endmodule
```

Functional Simulation Waveforms:

Library Name:	ixw5380_ibw_lib		
Cell Name:	IBW_INVX2		
Function/Truth Table:			
A		Y	
1		0	
0		1	
Delay Calculations: (ns)			
Propagation Delay Falling		0.8011	
Propagation Delay Rising		1.177	
Output Rise Time		0.8735	
Output Fall Time		0.5889	
Layout Area: 1.4 um ²			
Symbol with Port Names:			

Schematic:

Layout:

Verilog Model:

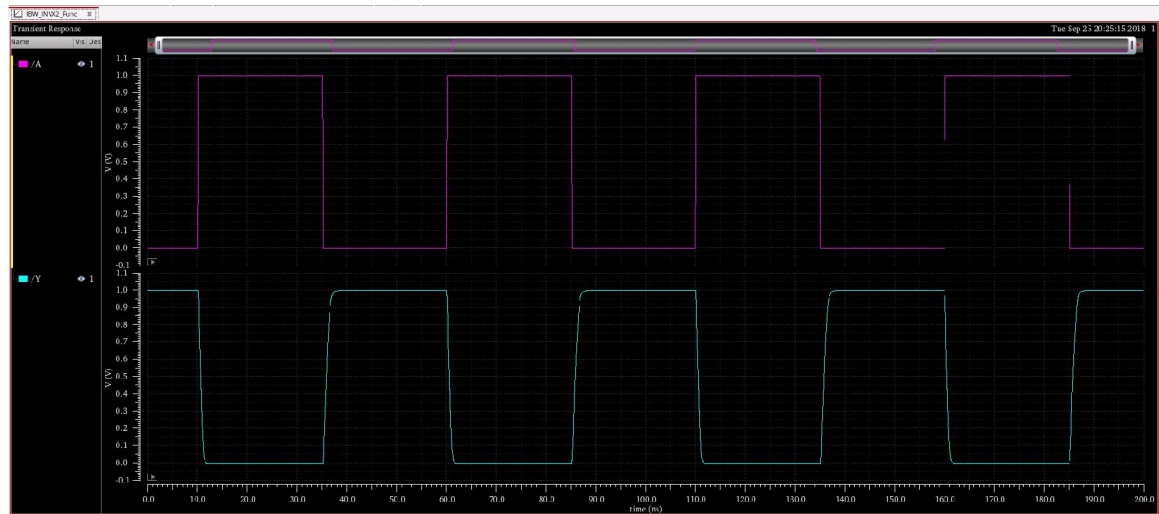
```
//Verilog HDL for "ixw5380_ibw_lib", "IBW_INVX1" "functional"

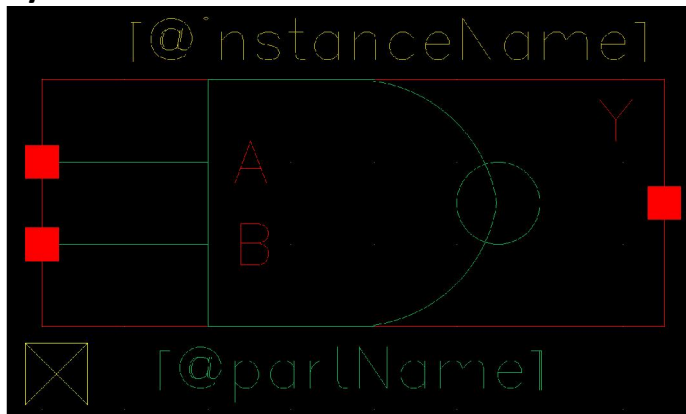
module IBW_INVX2 ( Y, A, .VDD(\VDD! ), .VSS(\VSS! ) );

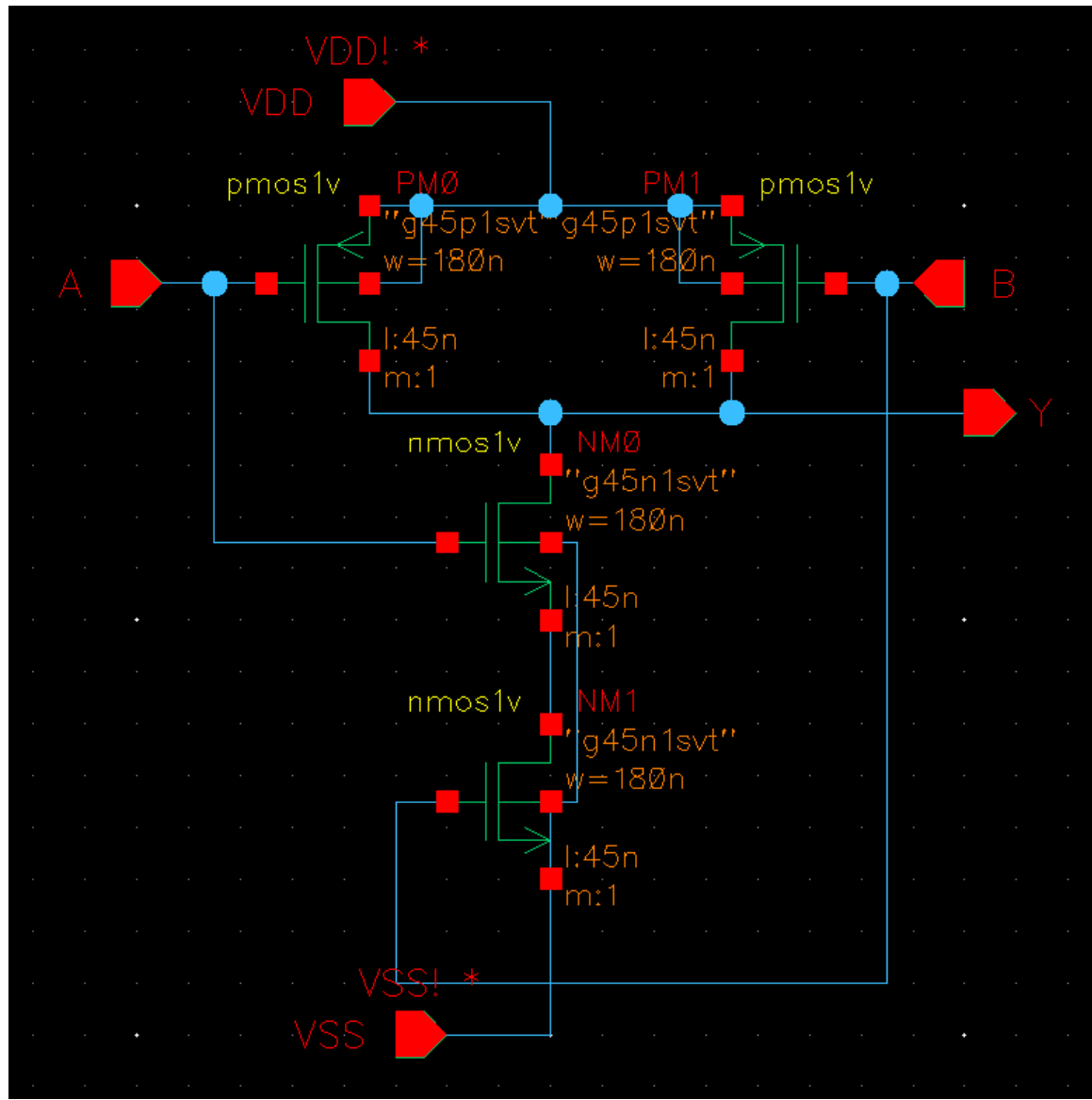
    input A;
    output Y;
    input
`ifdef INCA
    (* integer inh_conn_prop_name = "VDD";
    integer inh_conn_def_value = "cds_globals.\VDD! "; *)
    \VDD! ;
    input
`ifdef INCA
    (* integer inh_conn_prop_name = "VSS";
    integer inh_conn_def_value = "cds_globals.\VSS! "; *)
    \VSS! ;

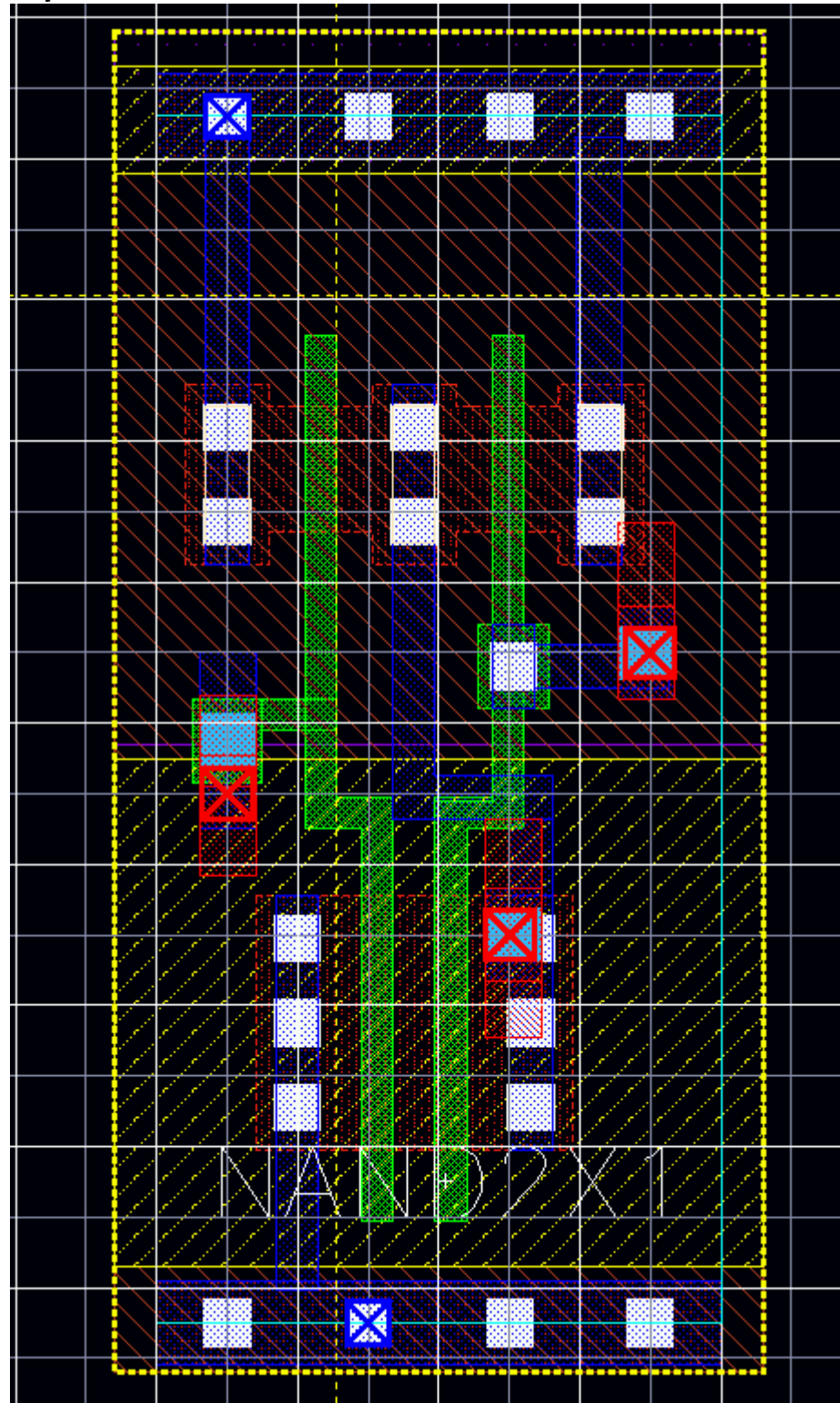
    not U1 (Y, A);

endmodule
```

Functional Simulation Waveforms:

Library Name:		ixw5380_ibw_lib	
Cell Name:		IBW_NAND2X1	
Function/Truth Table:			
A	B	Y	
0	0	1	
0	1	1	
1	0	1	
1	1	0	
Delay Calculations: (ns)			
A/Y pdr		1.206	
A/Y pdf		0.85	
B/Y pdr		1.201	
B/Y pdf		0.8543	
Output Rise Time		1.651	
Output Fall Time		1.111	
Layout Area: 1.7 um ²			
Symbol with Port Names:			
			

Schematic:

Layout:

Verilog Model:

```
//Verilog HDL for "ixw5380_ibw_lib", "IBW_INVX1" "functional"
```

```
module IBW_INVX2 ( Y, A, .VDD(\VDD! ), .VSS(\VSS! ) );
```

```
    input A;
```

```
    output Y;
```

```
    input
```

```
`ifdef INCA
```

```
    (* integer inh_conn_prop_name = "VDD";
```

```
    integer inh_conn_def_value = "cds_globals.\VDD! "; *)
```

```
`endif
```

```
    \VDD! ;
```

```
    input
```

```
`ifdef INCA
```

```
    (* integer inh_conn_prop_name = "VSS";
```

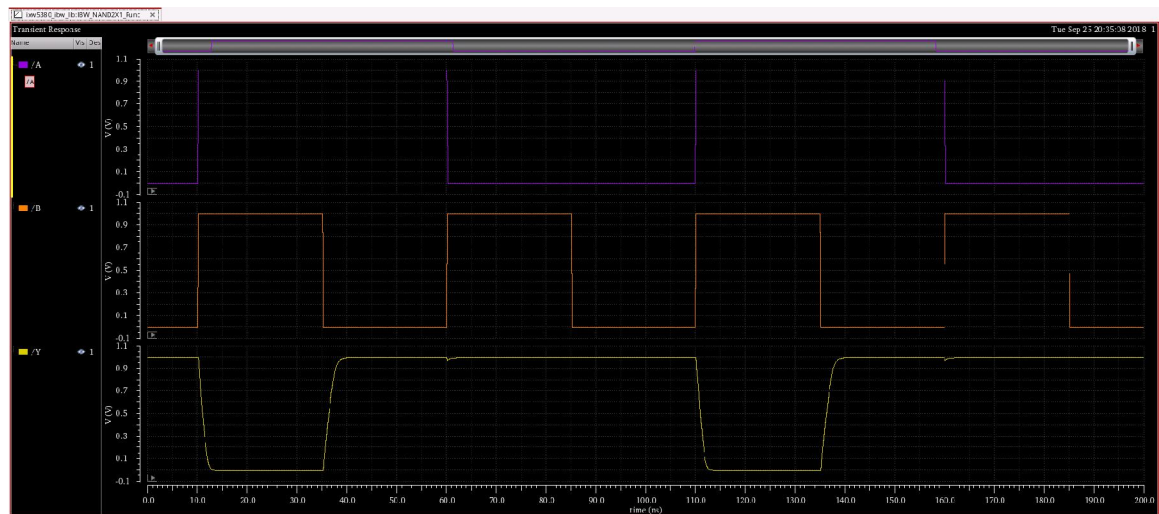
```
    integer inh_conn_def_value = "cds_globals.\VSS! "; *)
```

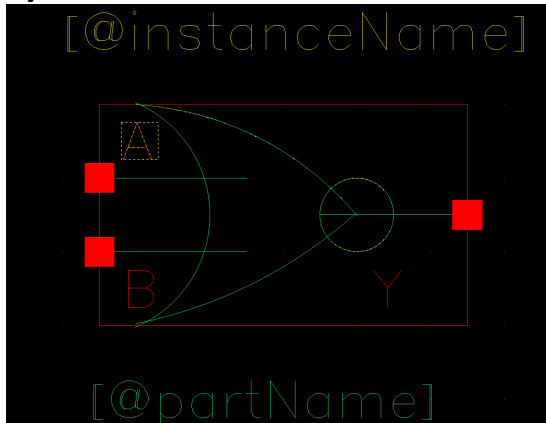
```
`endif
```

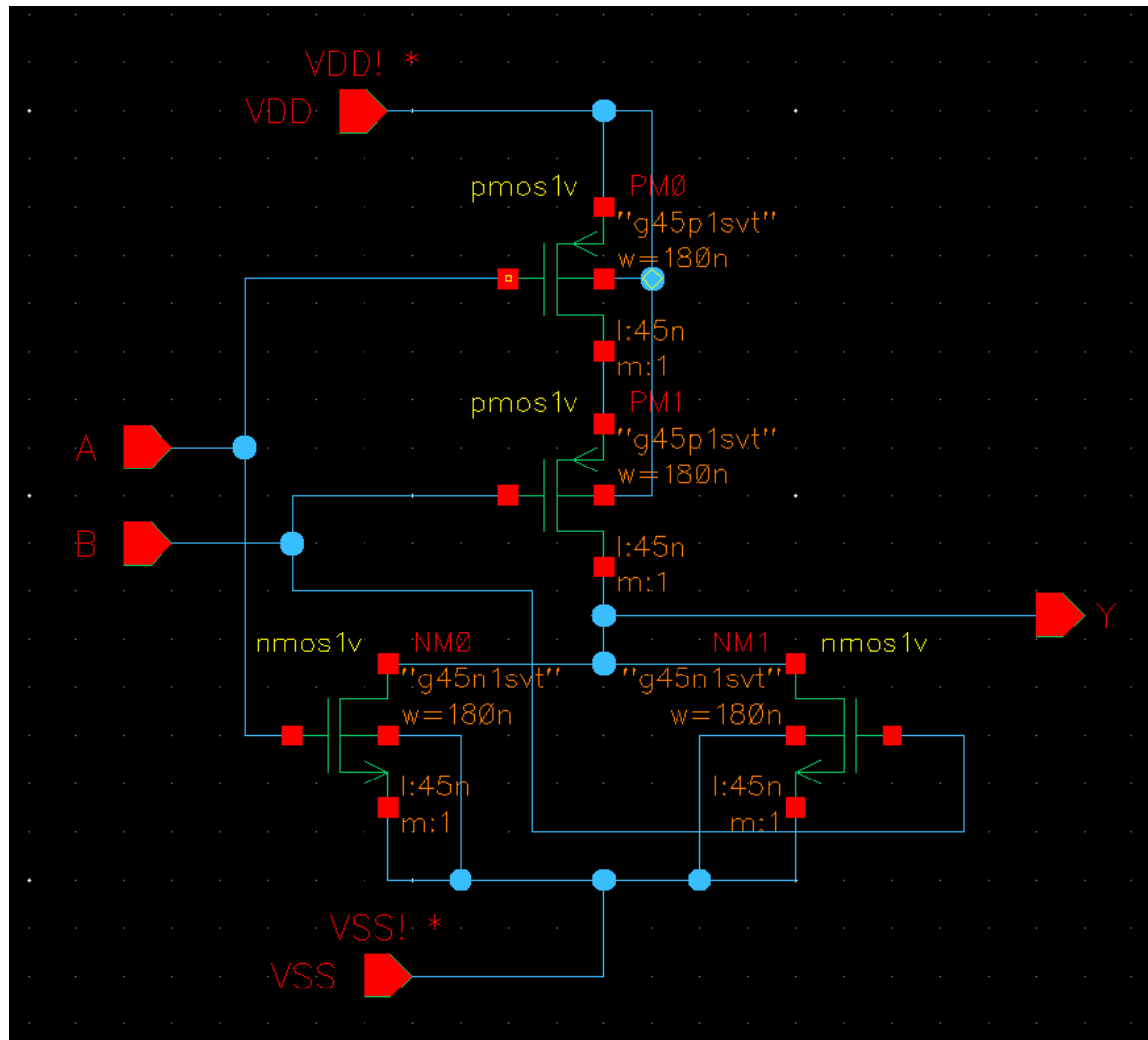
```
    \VSS! ;
```

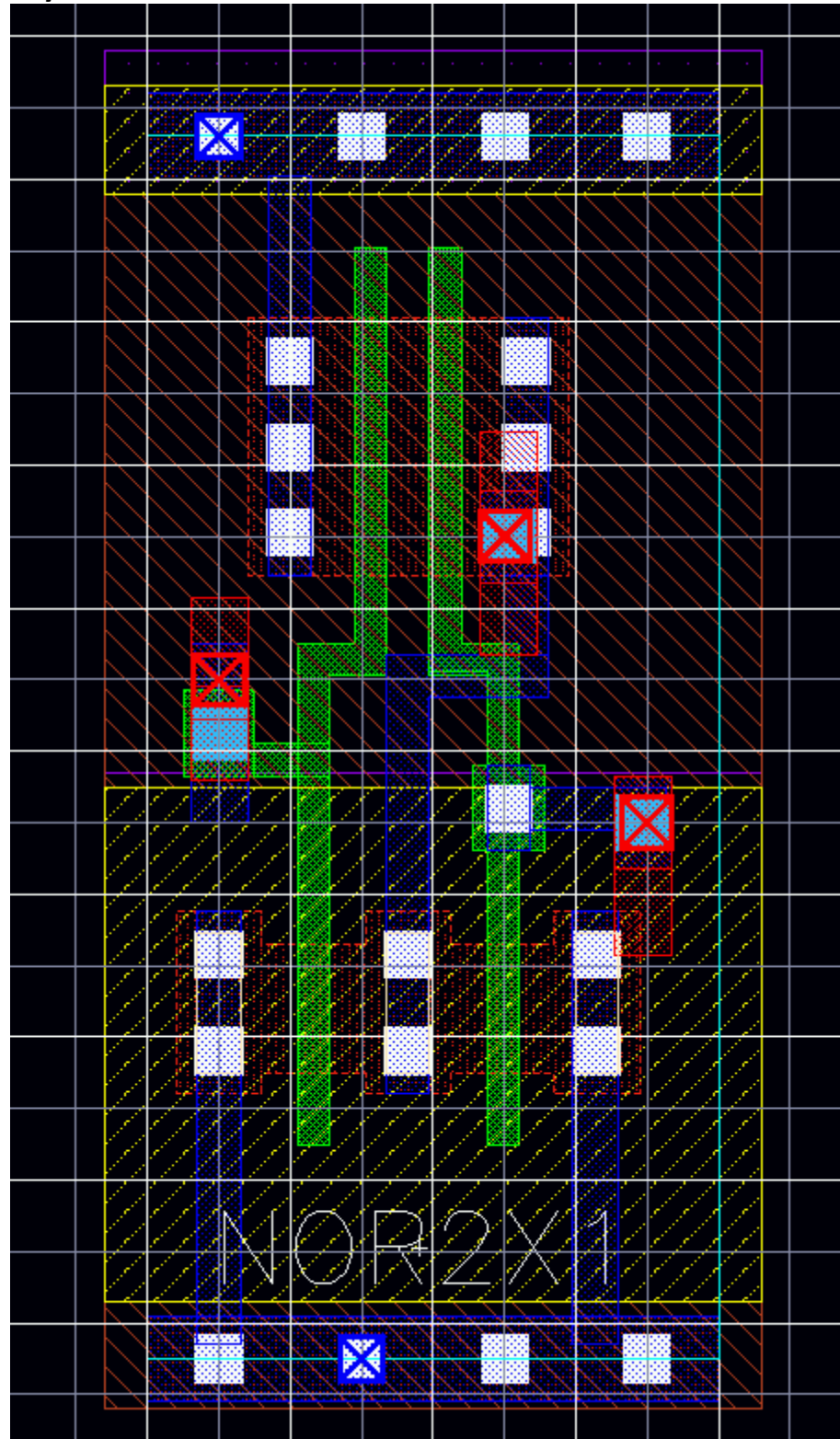
```
not U1 (Y, A);
```

```
endmodule
```

Functional Simulation Waveforms:**Comments/Notes:**

Library Name:		ixw5380_ibw_lib	
Cell Name:		IBW_NOR2X1	
Function/Truth Table:			
A	B	Y	
0	0	1	
0	1	0	
1	0	0	
1	1	0	
Delay Calculations: (ns)			
A/Y pdr		1.312	
A/Y pdf		0.774	
B/Y pdr		1.299	
B/Y pdf		0.7809	
Output Rise Time		1.751	
Output Fall Time		0.533	
Layout Area: 1.7 um ²			
Symbol with Port Names:			
@instanceName  @partName			

Schematic:

Layout:

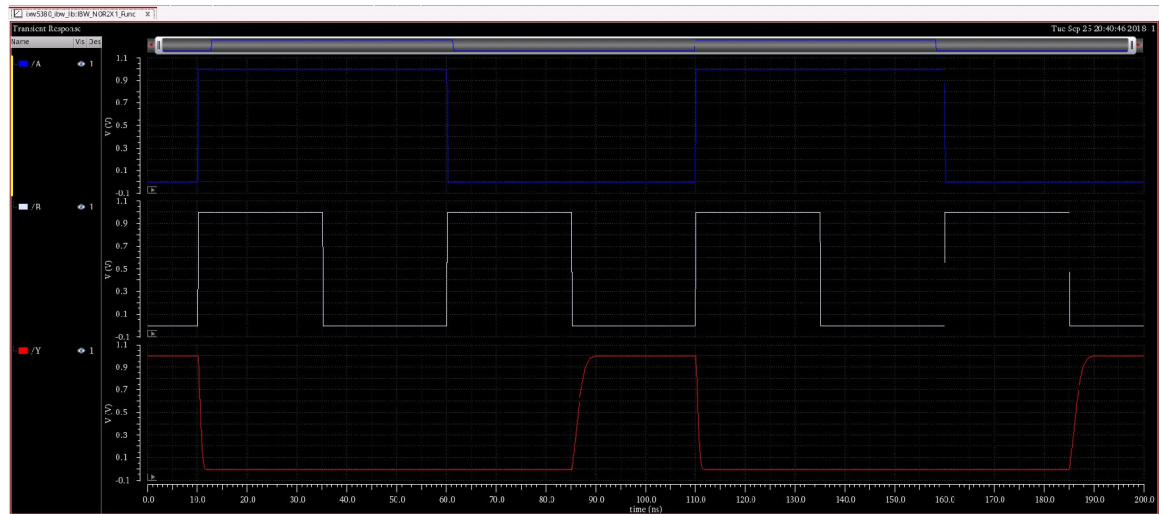
Verilog Model:

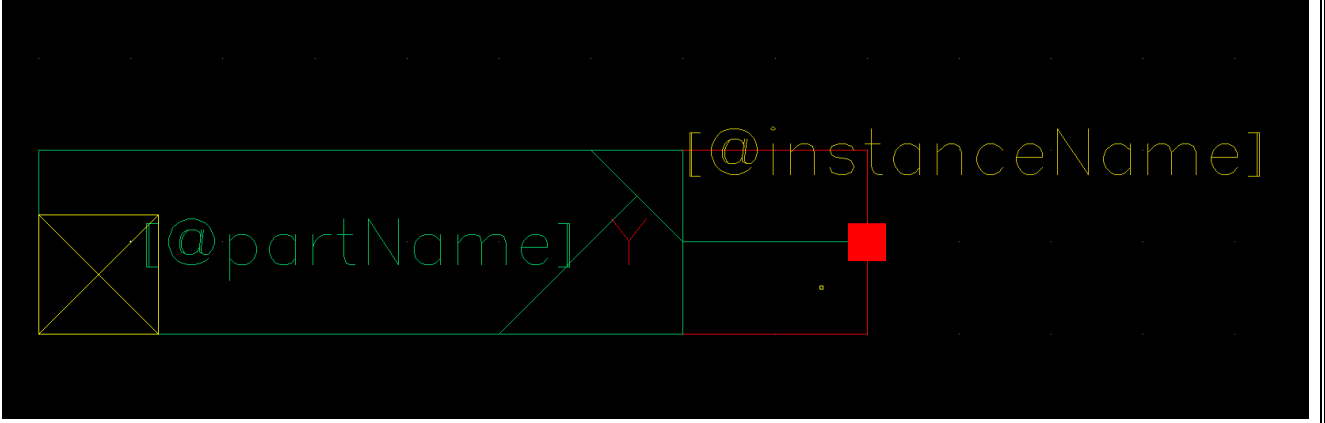
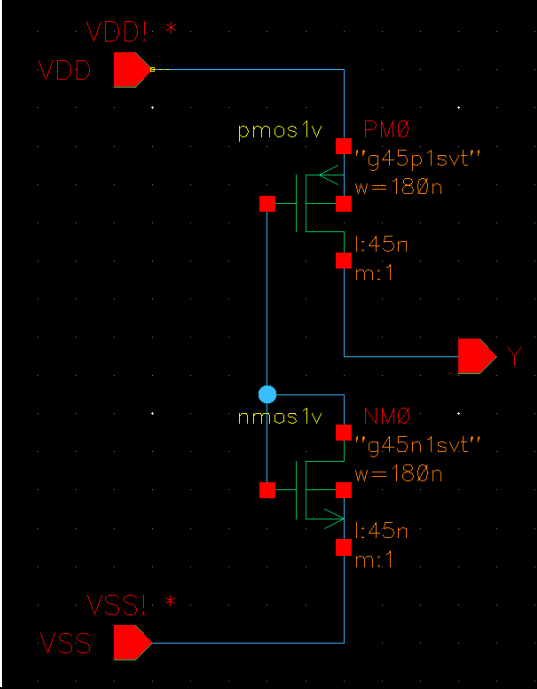
```
//Verilog HDL for "ixw5380_ibw_lib", "IBW_NOR2X1" "functional"

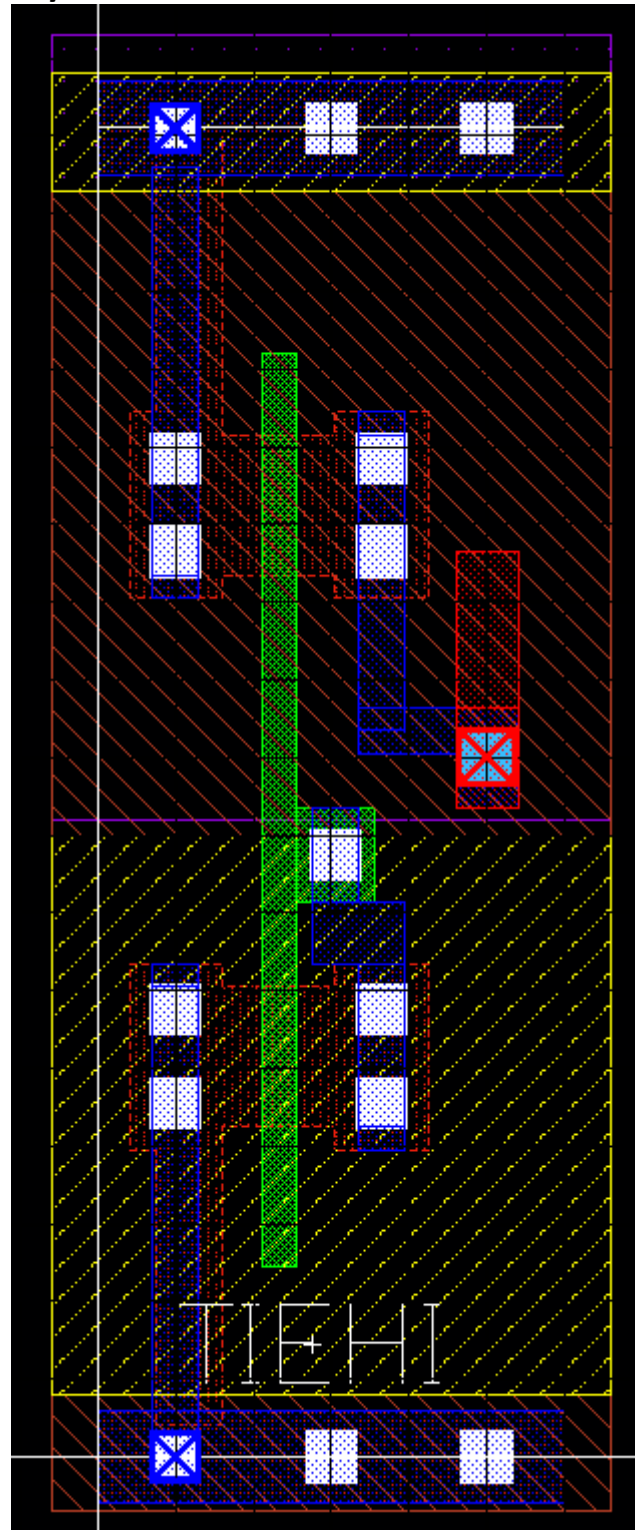
module IBW_NOR2X1 ( Y, A, B, .VDD(\VDD! ), .VSS(\VSS! ) );

    input A;
    output Y;
    input
`ifdef INCA
    (* integer inh_conn_prop_name = "VDD";
       integer inh_conn_def_value = "cds_globals.\VDD! "; *)
    \VDD! ;
    input
`ifdef INCA
    (* integer inh_conn_prop_name = "VSS";
       integer inh_conn_def_value = "cds_globals.\VSS! "; *)
    \VSS! ;
    input B;

    nor (Y, A, B);
endmodule
```

Functional Simulation Waveforms:**Comments/Notes:**

Library Name:	ixw5380_ibw_lib
Cell Name:	IBW_TIHI
Layout Area: 1.4 μm^2	
Symbol with Port Names:	
	
Schematic:	
	

Layout:

Verilog Model:

```
//Verilog HDL for "ixw5380_ibw_lib", "IBW_TIELO" "functional"

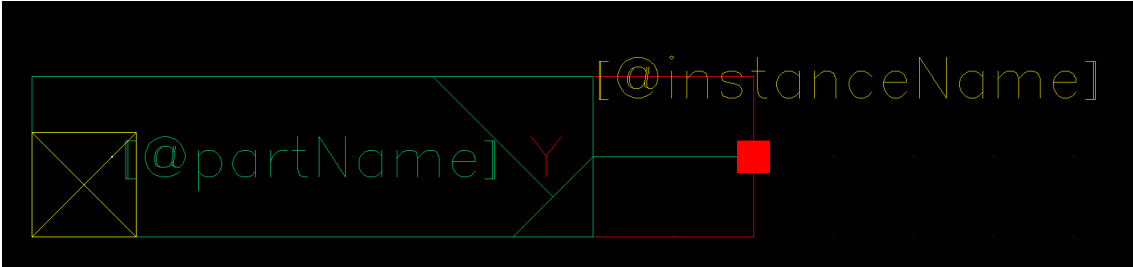
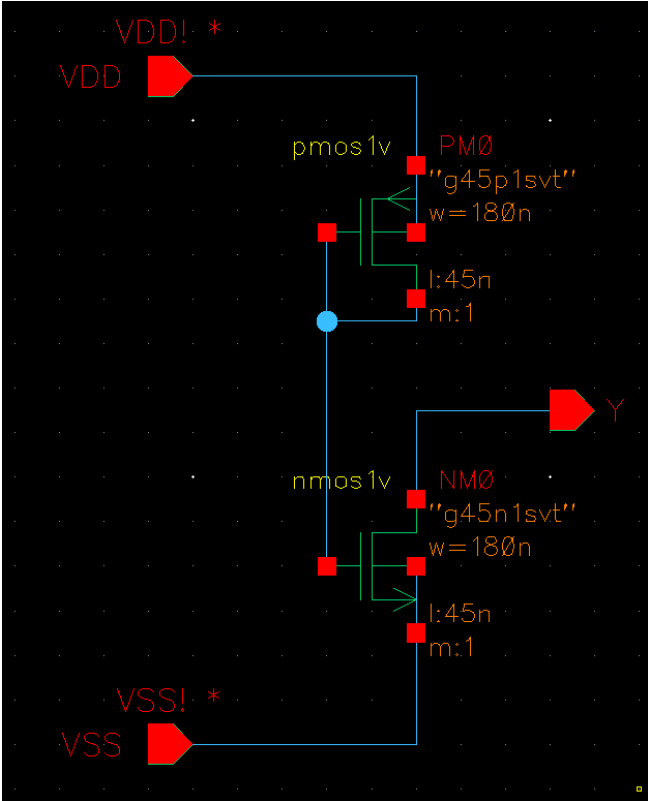
module IBW_TIWHI ( Y, .VDD(\VDD! ), .VSS(\VSS! ) );

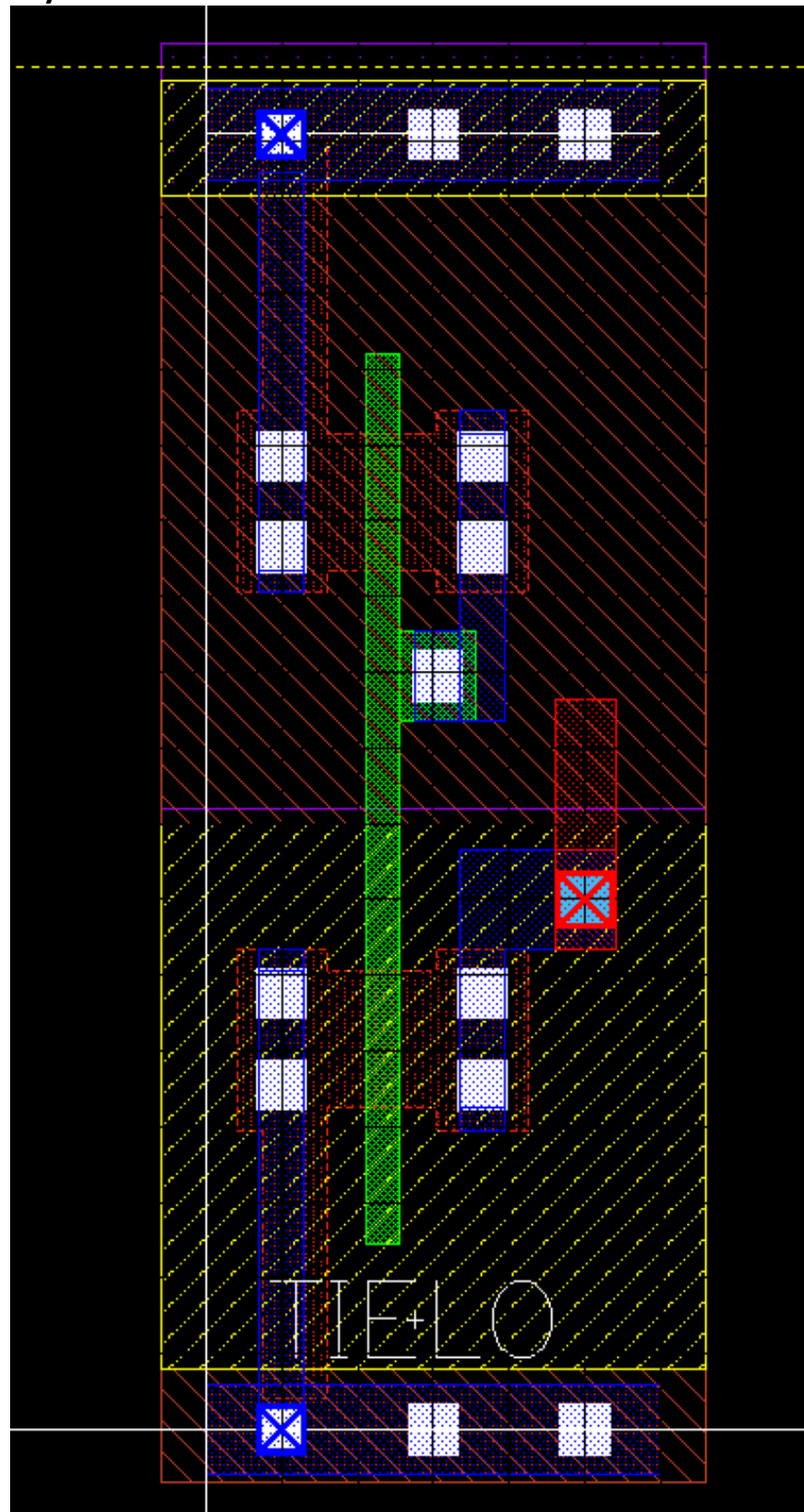
    output Y;
    input
`ifdef INCA
        (* integer inh_conn_prop_name = "VDD";
        integer inh_conn_def_value = "cds_globals.\VDD! "; *)
        \VDD! ;
    input
`ifdef INCA
        (* integer inh_conn_prop_name = "VSS";
        integer inh_conn_def_value = "cds_globals.\VSS! "; *)
        \VSS! ;

    assign Y = 1;

endmodule
```

Functional Simulation Waveforms:

Library Name:	ixw5380_ibw_lib
Cell Name:	IBW_TILOW
Layout Area: 1.4 μm^2	
Symbol with Port Names:	
	
Schematic:	
	

Layout:

Verilog Model:

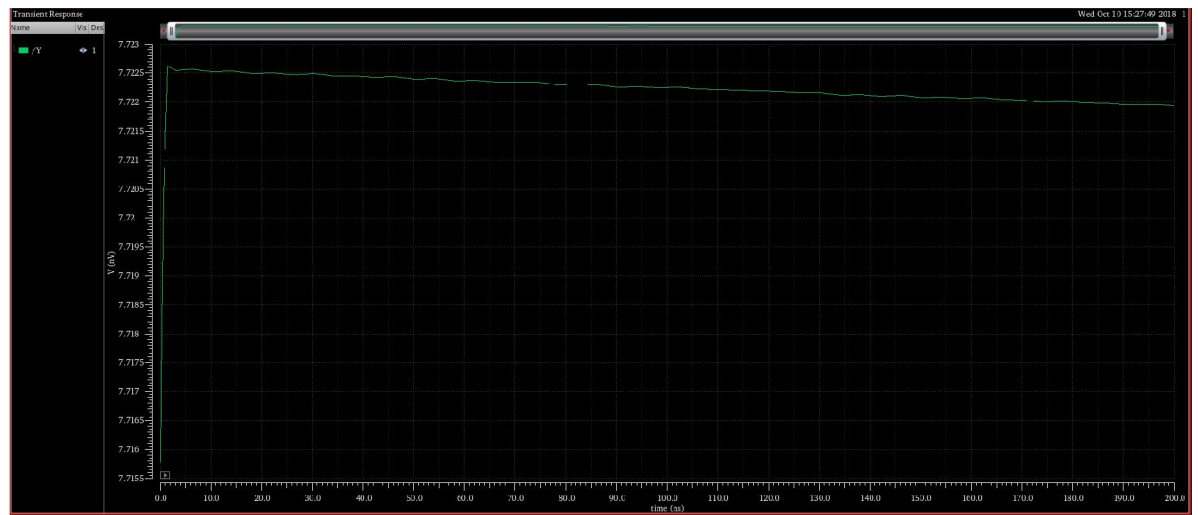
```
//Verilog HDL for "ixw5380_ibw_lib", "IBW_TIELO" "functional"

module IBW_TIELO ( Y, .VDD(\VDD! ), .VSS(\VSS! ) );

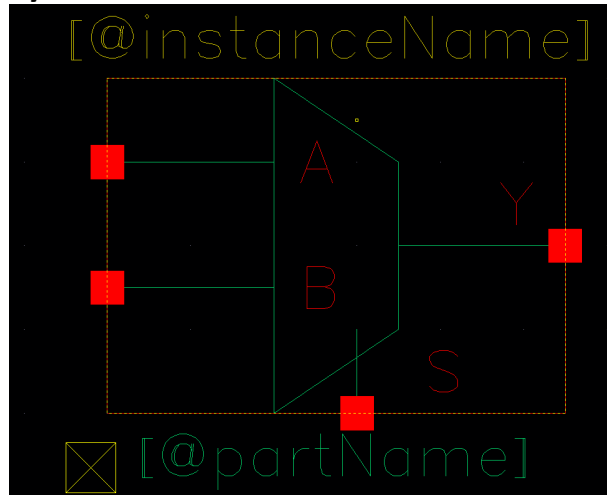
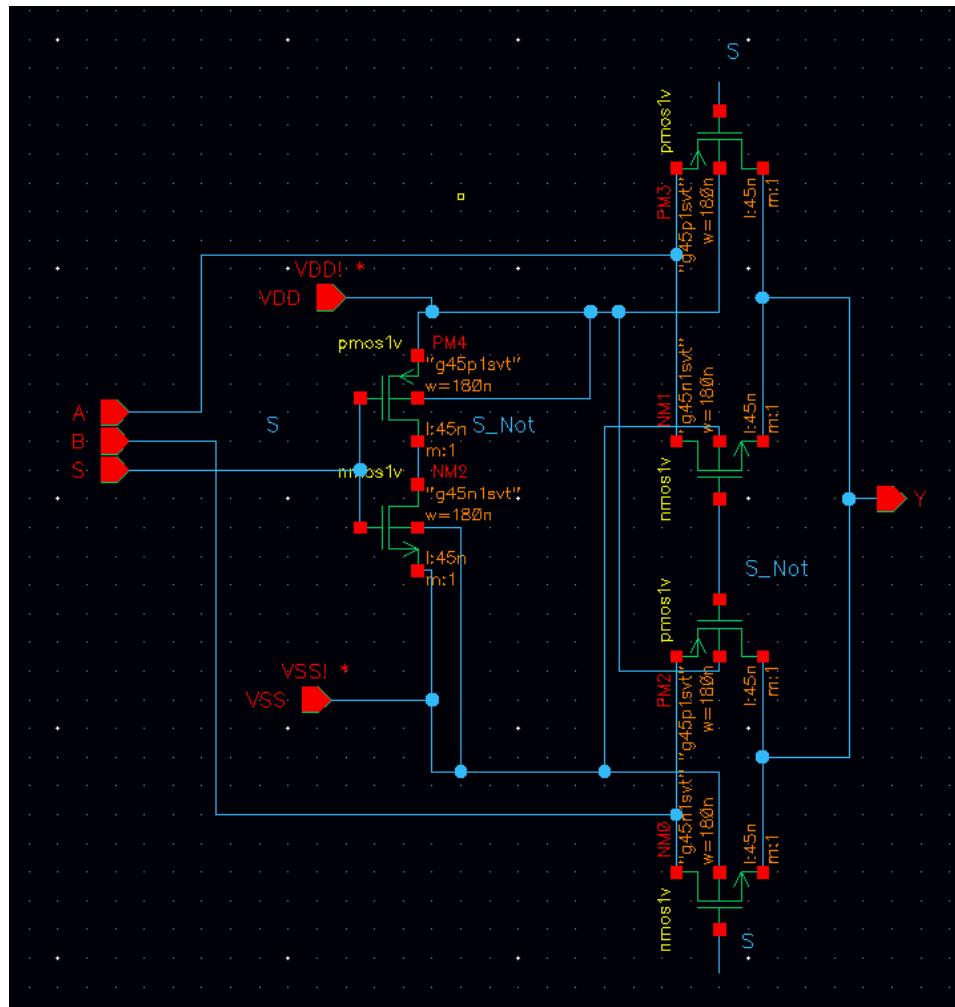
    output Y;
    input
`ifdef INCA
        (* integer inh_conn_prop_name = "VDD";
        integer inh_conn_def_value = "cds_globals.\VDD! "; *)
        \VDD! ;
    input
`ifdef INCA
        (* integer inh_conn_prop_name = "VSS";
        integer inh_conn_def_value = "cds_globals.\VSS! "; *)
        \VSS! ;

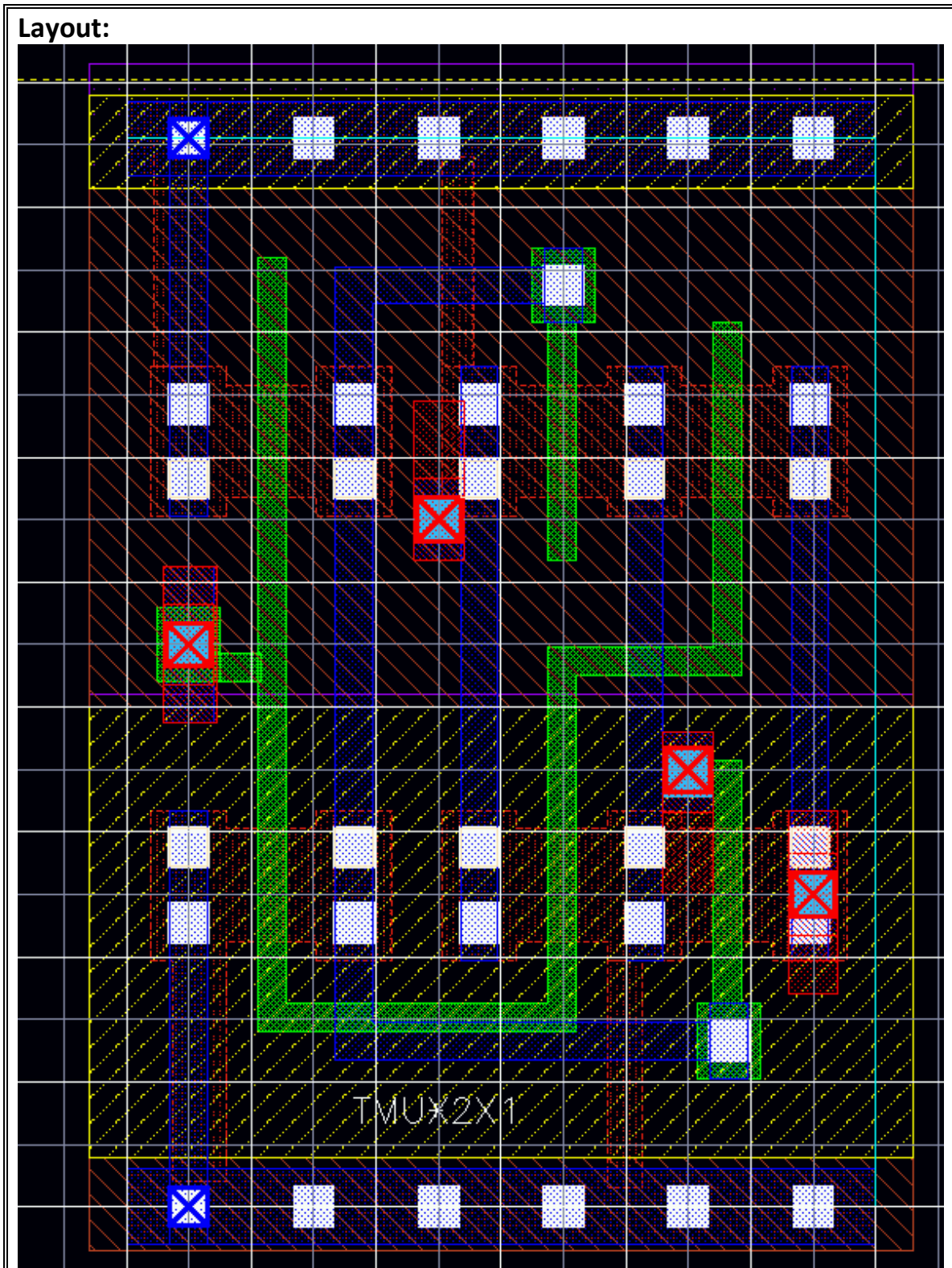
    assign Y = 0;

endmodule
```

Functional Simulation Waveforms:

Library Name:		ixw5380_ibw_lib	
Cell Name:		IBW_TMUX2X1	
Function/Truth Table:			
S	A	B	Y
0	0	Z	0
0	1	Z	1
0	1	Z	1
1	Z	0	0
1	Z	1	1
1	Z	0	0
1	Z	1	1
Delay Calculations: (ns)			
A/Y pdr		0.8355	
A/Y pdf		0.6376	
B/Y pdr		0.8362	
B/Y pdf		0.6362	
S/Y pdr		0.02598	
S/Y pdf		-0.02444	
Output Rise Time		1.551	
Output Fall Time		1.01	
Layout Area: 1.7 um ²			

Symbol with Port Names:**Schematic:**

Layout:

Verilog Model:

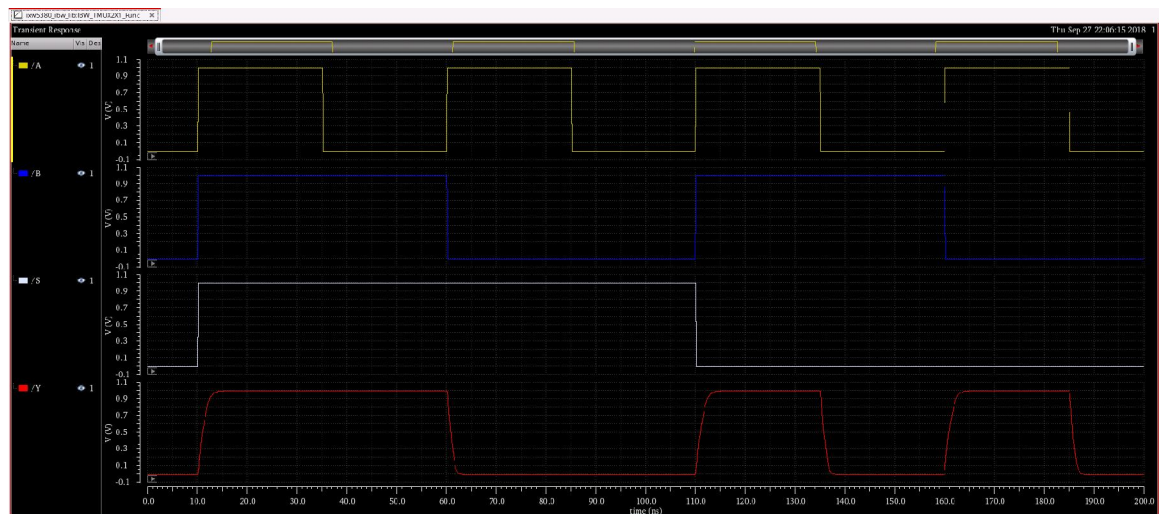
```
//Verilog HDL for "ixw5380_ibw_lib", "IBW_TMUX2X1" "functional"

module IBW_TMUX2X1 ( Y, A, B, S, .VDD(\VDD! ), .VSS(\VSS! ) );

    input A;
    input S;
    output Y;
    input
`ifdef INCA
    (* integer inh_conn_prop_name = "VDD";
    integer inh_conn_def_value = "cds_globals.\VDD! "; *)
    \VDD! ;
    input
`ifdef INCA
    (* integer inh_conn_prop_name = "VSS";
    integer inh_conn_def_value = "cds_globals.\VSS! "; *)
    \VSS! ;
    input B;

    and U1(f1, A, nS),
        U2(f2, B, S);
    or  U3(Y, f1, f2);
    not U4(nS,S);
    //assign Y = (S) ? B : A;

endmodule
```

Functional Simulation Waveforms:

5.2 Equipment Used

Item	Tool
Layout/Schematic/Test	Cadence Virtuoso 6.1.7-64b

Table 5.1 Equipment Used

5.3 References

[1] Handouts Provided By Dr. Indovina