verification HORIZONS

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Welcome to the DVCon 2015 issue of Verification Horizons

By Tom Fitzpatrick, Editor and Verification Technologist

As I write this note, it's February here in Massachusetts, which in 2015 means that there's about five feet of snow on the ground, with predictions of another foot of snow coming our way this weekend. And after that, the temperatures will drop to the single digits (°F), so even though my children will be on vacation from school next week, it's not really going to be an enjoyable week. Oh well, at least we got to enjoy the New England Patriots winning Super Bowl XLIX on a tremendous last-second interception.

The Patriots' Super Bowl win gave me an excellent opportunity to reflect on the passage of time. For those of you who don't follow (American) football, this was the Patriots' sixth Super Bowl appearance and fourth championship since 2002. Having become an avid fan since I moved to Massachusetts, this has been quite a run. I can remember each game, and my memories include watching my son grow up with each passing season. Watching him deal with the disappointment of heartbreaking losses and being able to celebrate so many exciting victories with him has truly been a blessing. And it doesn't hurt that he's now big enough to handle most of the snow shoveling, when we're not watching a game.

"If you're receiving this issue in print at DVCon, please stop by the new Verification Academy booth (#301)"

—Tom Fitzpatrick

Unfortunately, nothing about the weather or the Patriots leads me to think about verification this time around, but for those of you stuck in the snow (or those of you in Seattle), I hope this issue of Verification Horizons helps take your mind off your troubles.

Our feature article comes from my long-time colleague and friend, Harry Foster, who presents some results from the 2014 Wilson Research Group functional verification study in "Does Design Size Influence First Silicon Success?" These results build on similar surveys going back to 2007 to explore the trends, schedules and respins, as well as verification approaches taken over time. Be sure to check out the Verification Horizons blog for additional updates on this study.

Next, we have two PowerAware design and verification articles to share with you. The first, from Adnan Khan, John Biggs and Eamonn Quigley from ARM® Ltd., along with another long-time colleague and friend of mine, Erich Marschner, is actually being presented at DVCon US this year, and we're excited to share it with you. In "Successive Refinement: A Methodology for Incremental Specification of Power Intent," the authors explain how the Unified Power Format (UPF) specification can be used to specify and verify your power architecture abstractly, and then add implementation information later in the process. This methodology is still relatively new in the industry, so if you're thinking about making your next design PowerAware, you'll want to read this article to be up on the very latest approach.

Our other PowerAware article is "PowerAware RTL Verification of USB 3.0 IPs," from our friends at L&T Technology Services Limited. This article presents some of the challenges encountered in doing PowerAware design and highlights some of the cool things that UPF lets you do. In particular, you'll see how UPF can let you have two different power management architectures for the same RTL. As far as I know, this is the first published article that shows this powerful feature of UPF, so please check it out.

Next, Dr. Lauro Rizzatti, shares a bit of history with us in "Hardware Emulation: Three Decades of Evolution." This is part 1 of a three-part series in which Lauro takes us through the early years of emulation development (and for those of us who remember these events, makes us feel old). Over the next two issues, Lauro will bring us up to the present day where we'll see how far emulation has come and get a great feel for the things it can do.

Our friends at Oracle® are next up with "Evolving the Use of Formal Model Checking in SoC Design Verification," a case study of their use of formal methods as a central piece of their verification methodology for an SoC design that they recently completed. You may find it interesting to compare their experience, in which they achieved first-pass silicon success on schedule to the results of Harry's survey.

In our Partners' Corner section, we begin with "Small, Maintainable Tests" from Sondrel IC Design Services. This is a clever UVM-related article in which the author shows how to use default virtual sequences to raise the level of abstraction of tests. Check it out and see if it's something you might want to try.

Finally, we round out this edition with "Functional Coverage Development Tips: Do's and Don'ts" from our friends at eInfochips. This is a great overview of Functional Coverage, and specifically the covergroup and related features in SystemVerilog. I think you'll find their "problem-solution" approach in the article to be very useful in being able to apply their techniques to your environment.

If you're receiving this issue in print at DVCon, please stop by the new Verification Academy booth (#301) on the show floor. Or, if you see me in the halls or in one of the many technical sessions at the show, please say "hi." And for those of you who aren't at the show, please consider coming next year or, if it's more convenient, to DVCon Europe or DVCon India.

Respectfully submitted,
Tom Fitzpatrick
Editor, *Verification Horizons*

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Editor: Tom Fitzpatrick
Program Manager: Rebecca Granquist
Wilsonville Worldwide Headquarters
8005 SW Boeckman Rd.
Wilsonville, OR 97070-7777
Phone: 503-685-7000

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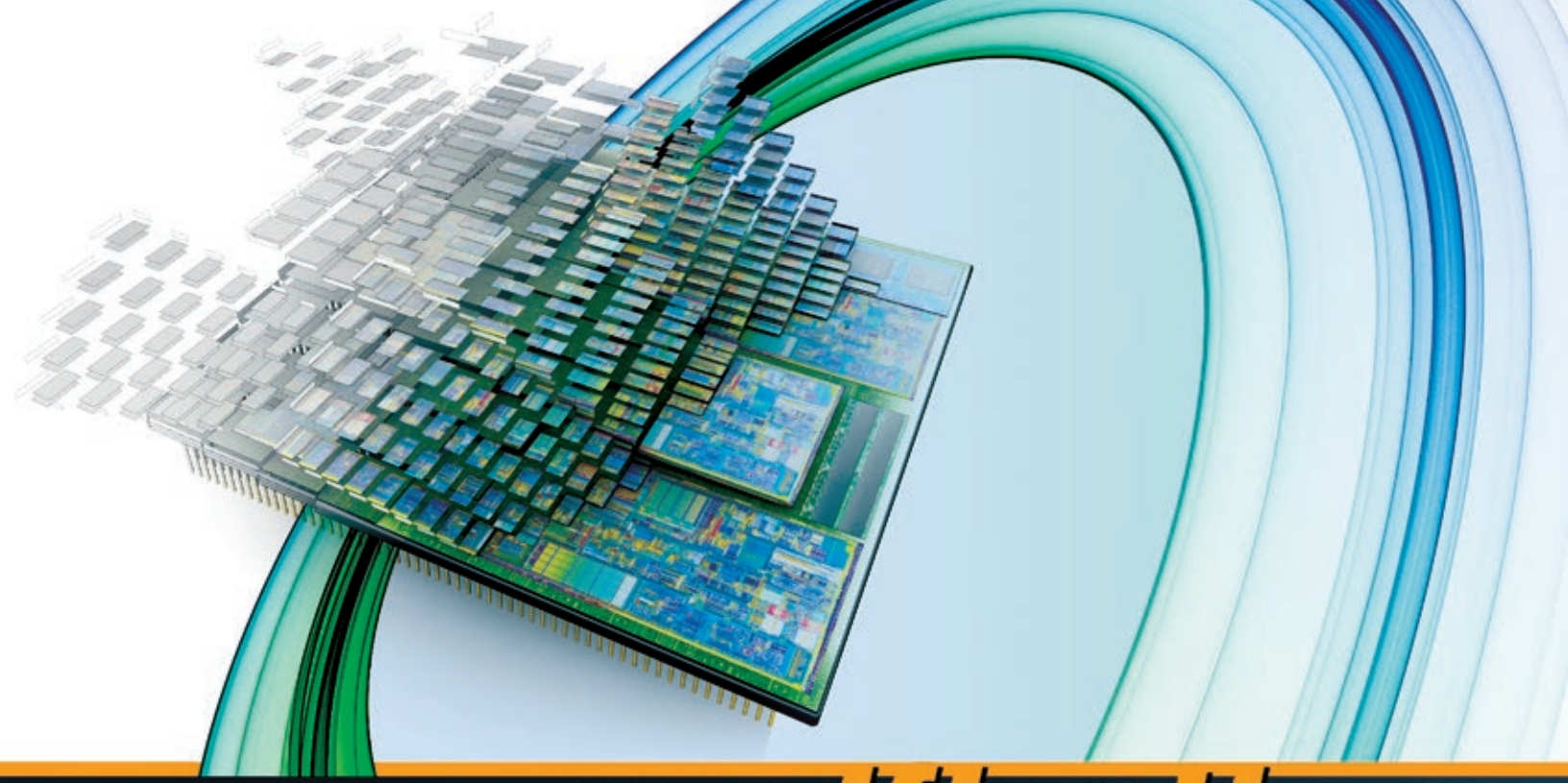

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Editor: Tom Fitzpatrick
Program Manager: Rebecca Granquist

Wilsonville Worldwide Headquarters
8005 SW Boeckman Rd.
Wilsonville, OR 97070-7777
Phone: 503-685-7000

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