Does Design Size Influence First Silicon Success?

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INTRODUCTION

In 2002 and 2004, Collett International Research, Inc. conducted its well-known ASIC/IC functional verification studies, which provided invaluable insight into the state of the electronic industry and its trends in design and verification at that point in time. However, after the 2004 study, no additional Collett studies were conducted, which left a void in identifying industry trends. To address this dearth of knowledge, over the years Mentor Graphics has commissioned multiple world-wide, double-blind, functional verification studies, covering all electronic industry market segments. In this article, we present a few highlights from our most recent study, and try to address the question: "Does design size influence the likelihood of achieving first silicon success?"

RESOURCE TRENDS

Today, the industry is experiencing growing resource demands due to rising design complexity. Figure 1 shows the percentage of total project time spent in verification. As you would expect, the results are all over the spectrum; whereas, some projects spend less time in verification, other projects spend more. The average total project time spent in verification in 2014 was 57 percent, which did not change significantly from 2012. However, notice the increase in the percentage of projects that spend more than 80 percent of their time in verification.

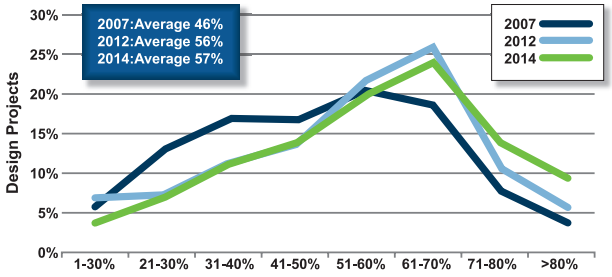

Figure 1. Percentage of Project Time Spent in Verification

Perhaps one of the biggest challenges in design and verification today is identifying solutions to increase productivity and control engineering headcount. To illustrate the need for productivity improvement, we discuss the trend in terms of increasing engineering headcount. Figure 2 shows the mean peak number of engineers working on a project. Again, this is an industry average since some projects have many engineers while other projects have few. You can see that the mean peak number of verification engineers today is greater than the mean peak number of design engineers. In other words, there are, on average, more verification engineers working on a project than design engineers. This situation has changed significantly since 2007.

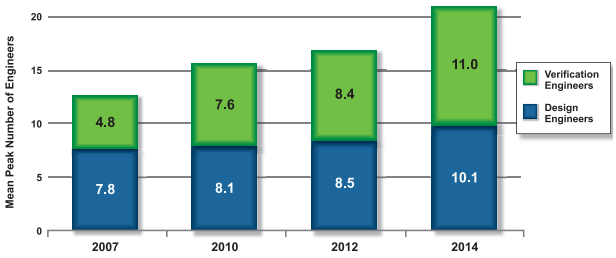

Figure 2. Mean Number of Peak Engineers per Project

Another way to comprehend the impact of today's project headcount trends is to calculate the compounded annual growth rate (CAGR) for both design and verification engineers. Between 2007 and 2014 the industry experienced a 3.7 percent CAGR for design engineers and a 12.5 percent CAGR for verification engineers. Clearly, the double-digit increase in required verification engineers has become a major project cost-management concern, and is one indicator of growing verification effort.

But verification engineers are not the only project stakeholders involved in the verification process. Design engineers spend a significant amount of their time in verification too, as shown in Figure 3. In 2014, design engineers spent on average 53 percent of their time involved in design activities and 47 percent of their time in verification.

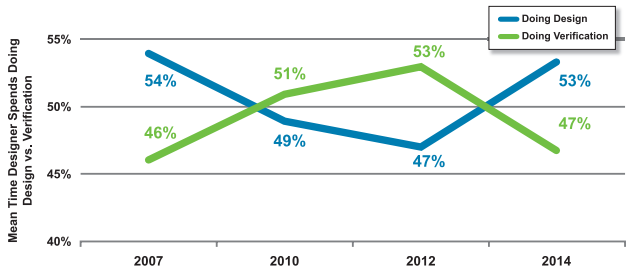

Figure 3. Where Design Engineers Spend Their Time

However, this is a reversal in the trends observed from the 2010 and 2012 studies, which indicated that design engineers spent more time in verification activities than design activities. The data suggest that design effort has risen significantly in the last two years when you take into account that: (a) design engineers are spending more time in design, and (b) there was a nine percent CAGR in required design engineers between 2012 and 2014 (shown in Figure 4), which is a steeper increase than the overall 3.7 CAGR for design engineers spanning 2007 through 2014. One factor contributing to this increase demand in design engineers relates to the complexity of creating designs that actively manage power.

Figure 4 shows where verification engineers spend their time (on average). We do not show trends here since this aspect of project resources was not studied prior to 2012, and there were no significant changes in the results between 2012 and 2014.

Our study found that verification engineers spend more of their time in debugging than any other activity. This needs to be an important research area whose future solutions will be necessary for improving productivity and predictability within a project.

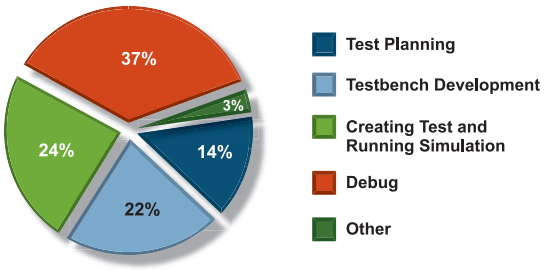

Figure 4. Where Verification Engineers Spend Their Time

SCHEDULE & RESPIN TRENDS

Today we find that a significant amount of effort is being applied to functional verification. An important question our study has tried to answer is whether this increasing effort is paying off. In this section, we present verification results findings in terms of schedules and number of required spins.

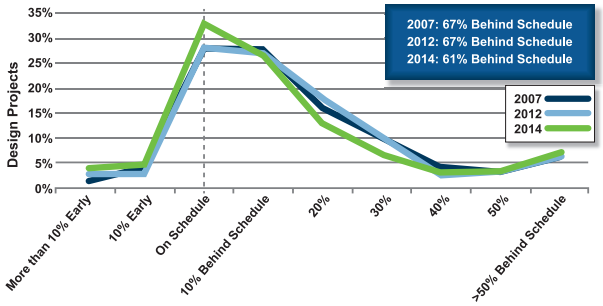

Figure 5. Design Completion Compared to Original Schedule

Figure 5 presents the design completion time compared to the project's original schedule. The data suggest that in 2014 there was a slight improvement in projects meeting their original schedule, where in the 2007 and 2012 studies, 67 percent of the projects were behind scheduled, compared to 61 percent in 2014. It is unclear if this improvement is due to the industry becoming more conservative in project planning or simply better at scheduling. Regardless, meeting the originally planned schedule is still a challenge for most of the industry.

Figure 6 shows the industry trend for the number of spins required between the start of a project and final production. Even though designs have increased in complexity, the data suggest that projects are not getting any worse in terms of the number of required spins before production. Still, only about 30 percent of today's projects are able to achieve first silicon success.

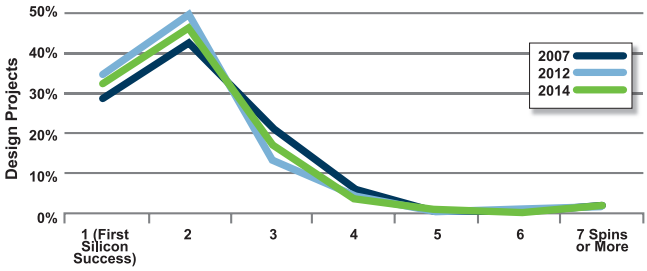

Figure 6. Required Number of Spins

DESIGN SIZE IMPACT ON RESPINS

It's generally assumed that the larger the design—the increased likelihood of the occurrence of bugs. Yet, a question worth answering is how effective projects are at finding these bugs prior to tapeout.

In Figure 7, we first extract the 2014 data from the required number of spins trends presented in Figure 6, and then partition this data into sets based on design size (that is, designs less than 5 million gates, designs between 5 and 80 million gates, and designs greater than 80 million gates). This led to perhaps one of the most startling findings from our 2014 study. That is, the data suggest that the smaller the design—the less likelihood of achieving first silicon success! While 34 percent of the designs over 80 million gates achieve first silicon success, only 27 percent of the designs less than 5 million gates are able to achieve first silicon success. The difference is statistically significant.

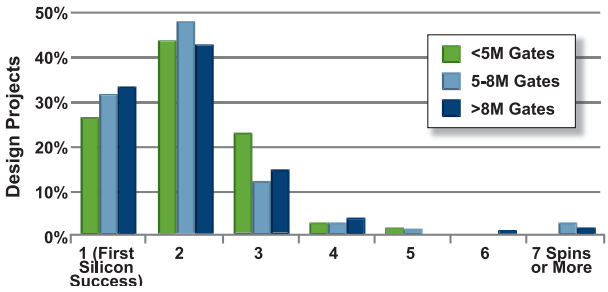

Figure 7. Number of Spins by Design Size

To understand what factors might be contributing to this phenomena, we decided to apply the same partitioning technique while examining verification technology adoption trends.

Figure 8 shows the adoption trends for various verification techniques from 2007 through 2014, which include code coverage, assertions, functional coverage, and constrained-random simulation.

One observation we can make from these adoption trends is that the electronic design industry is maturing its verification processes. This maturity is likely due to the need to address the challenge of verifying designs with growing complexity.

In Figure 9 we extract the 2014 data from the various verification technology adoptions trends presented in Figure 8, and then partition this data into sets based on design size (that is, designs less than 5 million gates, designs between 5 and 80 million gates, and designs greater than 80 million gates).

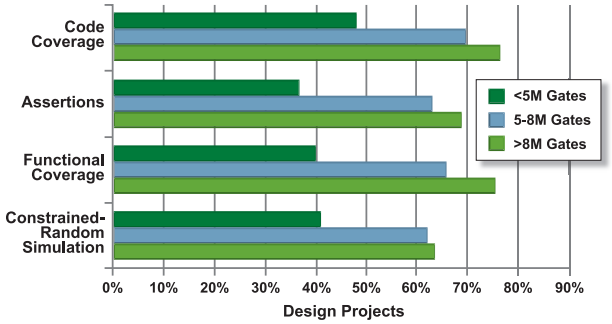

Figure 8. Verification Technology Adoption Trends

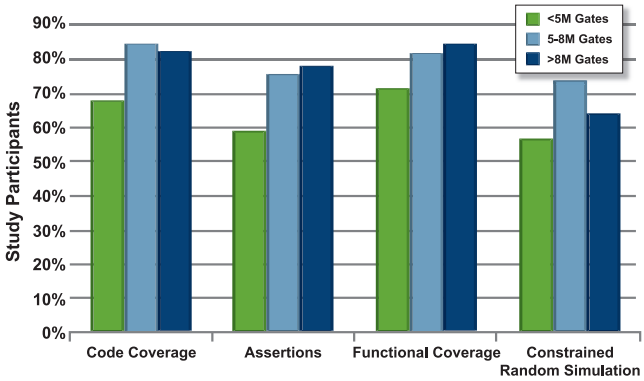

Figure 9. Verification Technology Adoption by Design Sizes

Across the board we see that designs less than 5 million gates are less likely to adopt code coverage, assertions, functional coverage, and constrained-random simulation. Hence, if you correlate this data with the number of spins by design size (as shown in Figure 7), then the data suggest that the verification maturity of an organization has a significant influence on its ability to achieve first silicon success.

As a side note, you might have noticed that there is less adoption of constrained-random simulation for designs greater than 80 million gates. There are a few factors contributing to this behavior: (1) Constrained-random works well at the IP and subsystem level, but does not scale to the full-chip level for large designs. (2) There are a number of projects working on large designs that predominately focuses on integrating existing or purchased IPs. Hence, these types of projects focus more of their verification effort on integration and system validation task, and constrained-random simulation is rarely applied here.

CONCLUSION

In this article, we presented a few highlights from the 2014 Wilson Research Group Functional Verification Study that was commissioned by Mentor Graphics. One of the key takeaways from our study is that verification effort continues to increase, which was observed by the double-digit increase in peak number verification engineers required on a project.

In general, the industry is maturing its verification processes as witnessed by the verification technology adoption trends. However, we found that smaller designs were less likely to adopt what is generally viewed as industry best verification practices and techniques. Similarly, we found that projects working on smaller designs tend to have a smaller ratio of peak verification engineers to peak designers. Could the fact that fewer available verification resources combined with the lack of adoption of more advanced verification techniques account for fewer small designs achieving first silicon success? The data suggest that this might be one contributing factor. It's certainly something worth considering.

As a closing comment to this article, our plan is to release all the findings from the 2014 Wilson Research Group Functional Verification Study over the next few months through a series of Verification Horizons blogs, and a paper to be published at the 2015 Design Automation Conference.