From Tightly Coupled
(Loosely Bolted)
to Verification Convergence
Verification Academy Membership Trends

www.verificationacademy.org

CAGR: 79%

<table>
<thead>
<tr>
<th>Year</th>
<th>Membership</th>
</tr>
</thead>
<tbody>
<tr>
<td>2009</td>
<td>1544</td>
</tr>
<tr>
<td>2010</td>
<td>3651</td>
</tr>
<tr>
<td>2011</td>
<td>8444</td>
</tr>
<tr>
<td>2012</td>
<td>14838</td>
</tr>
<tr>
<td>2013</td>
<td>21730</td>
</tr>
<tr>
<td>2014</td>
<td>28322</td>
</tr>
</tbody>
</table>
Tightly Coupled *(Loosely Bolted)*
Verification Consumes Majority of Project Time

2007: Average 46%
2012: Average 56%
2014: Average 57%


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More Verification Engineers vs Design Engineers


CAGR Designers 3.72%
CAGR Verifiers 12.52%

Mean Peak Number of Engineers

Mean Peak Number of Engineers Increasing

19% increase designers between 2012 and 2014
31% increase verifiers between 2012 and 2014

Many Projects Miss Schedule

2007: 67% behind schedule
2012: 67% behind schedule
2014: 61% behind schedule

Actual ASIC-IC design completion compared to project’s original schedule

Few Designs Achieve First Silicon Success


Number of Required Spins

- 2007
- 2012
- 2014

2014 Number of Spins by Design Size

Smaller designs are less likely to achieve first silicon success?

Chances of getting a single gate design correct is infinitely small!
Trends in Verification Techniques


- Code coverage
- Assertions
- Functional coverage
- Constrained-Random Simulation

Design Projects

Verification Technique Adoption by Design Size


2014 Verification Technique Adoption by Design Size

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Verification Language Adoption Trends

Languages Used for Verification (Testbenches)

- VHDL
- Verilog
- Synopsys Vera
- System C
- SystemVerilog
- Specman e
- C/C++


* Multiple answers possible
Verification Language Adoption Trends

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**Testbench Methodology Adoption Trends**

56% UVM growth between 2012 and 2014

<table>
<thead>
<tr>
<th>Methodologies and Testbench Base-Class Libraries</th>
<th>Design Projects</th>
</tr>
</thead>
<tbody>
<tr>
<td>Accellera UVM</td>
<td>2012</td>
</tr>
<tr>
<td>OVM</td>
<td>2014</td>
</tr>
<tr>
<td>Mentor AVM</td>
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<tr>
<td>Synopsys VMM</td>
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<tr>
<td>Synopsys RVM</td>
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<tr>
<td>Cadence eRM</td>
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</tr>
<tr>
<td>Cadence URM</td>
<td></td>
</tr>
<tr>
<td>None/Other</td>
<td></td>
</tr>
</tbody>
</table>


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Testbench Methodology Adoption Trends

56% UVM growth between 2012 and 2014
13% UVM projected growth in the next year

- Accellera UVM
- OVM
- Mentor AVM
- Synopsys VMM
- Synopsys RVM
- Cadence eRM
- Cadence URM
- None/Other

Design Projects

Methodologies and Testbench Base-Class Libraries


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* Multiple answers possible
Power Intent Standards Trends

Notation Used to Describe Power Intent

18% Increase in the Past Two Years!


Designs That Actively Managed Power

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Moving Towards Verification Convergence
Enterprise Verification

Stephen A Bailey
Director of Emerging Technologies

info@verificationacademy.com  |  www.verificationacademy.com
New Platform

12-18 months

Verification is the bottleneck

Derivative

3-6 months
3 Enduring Challenges

1. Speed – Verification Cycles
2. Productivity of the Flow
3. Automation of the Process

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Verification Complexity Means …

Verification Platforms!

OMG!

I’ll Keep it Short …

If You Promise to Visit our Booth Today
Fastest Growing Segment of EDA is Emulation

Mentor Emulation Revenue
($Millions)

>30% CAGR

2010  2012  2014

Source: Mentor Graphics
Mentor’s Enterprise Verification Platform

Vista™ Virtual Prototype

Questa® Formal

Questa® Simulation

Veloce® Emulation

FPGA Prototype

Fastest Engines
Mentor’s Enterprise Verification Platform

Verification Infrastructure

Integrated Flow

Fastest Engines
Mentor’s Enterprise Verification Platform

Process Automation

Stimulus
Management & Analysis
Visualizer™ Debug

Verification Infrastructure

Vista™ Virtual Prototype
Questa® Formal
Questa® Simulation
Veloce® Emulation
FPGA Prototype

Integrated Flow

Fastest Engines
Mentor's New Enterprise Verification Platform
by Paul McLellan
Published on 04-10-2014 01:01 AM

Synopsys Verification Continuum
by Paul McLellan
Published on 09-26-2014 03:00 PM

All other EDA Vendors to-date
Mentor at DVCon

• Exhibit Hall Booth: 801
  • West end of hall by doors to foyer

• Tutorial 5T Thursday AM Donner Ballroom
  • Advanced, High-Throughput Debug from Architectural Modeling Through Post-Silicon SoC Validation

• Tutorial 8T Thursday PM
  • Dead or Alive: Using Automated Formal Techniques to Characterize Dead Code, Reveal Paths to Hit Uncovered States, and Reach Coverage Closure Fast
From Tightly Coupled
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