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## Quad/Dual, Low-Voltage, Bidirectional RF/Video Switches

## General Description

The MAX4565/MAX4566/MAX4567 are low-voltage T-switches designed for switching RF and video signals from DC to 350 MHz in $50 \Omega$ and $75 \Omega$ systems. The MAX4565 contains four normally open single-pole/single-throw (SPST) switches. The MAX4566 contains two dual SPST switches (one normally open, one normally closed.) The MAX4567 contains two single-pole/double-throw (SPDT) switches.
Each switch is constructed in a "T" configuration, ensuring excellent high-frequency off isolation and crosstalk of -83 dB at 10 MHz . They can handle rail-to-rail analog signals in either direction. On-resistance ( $60 \Omega$ max) is matched between switches to $2.5 \Omega$ max and is flat ( $2 \Omega$ max) over the specified signal range, using $\pm 5 \mathrm{~V}$ supplies. The off leakage current is less than 5 nA at $+25^{\circ} \mathrm{C}$ and 50 nA at $+85^{\circ} \mathrm{C}$.
These CMOS switches can operate with dual power supplies ranging from $\pm 2.7 \mathrm{~V}$ to $\pm 6 \mathrm{~V}$ or a single supply between +2.7 V and +12 V . All digital inputs have $0.8 \mathrm{~V} / 2.4 \mathrm{~V}$ logic thresholds, ensuring both TTL- and CMOS-logic compatibility when using $\pm 5 \mathrm{~V}$ or a single +5 V supply.

## Applications

- RF Switching
- Video Signal Routing
- High-Speed Data Acquisition
- Test Equipment
- ATE Equipment
- Networking


## Features

- High $50 \Omega$ Off Isolation: -83 dB at 10 MHz
- Low $50 \Omega$ Crosstalk: -87 dB at 10 MHz
- DC to $350 \mathrm{MHz}-3 \mathrm{~dB}$ Signal Bandwidth
- $60 \Omega$ Signal Paths with $\pm 5 \mathrm{~V}$ Supplies
- $2.5 \Omega$ Signal-Path Matching with $\pm 5 \mathrm{~V}$ Supplies
- $2 \Omega$ Signal-Path Flatness with $\pm 5 \mathrm{~V}$ Supplies
- Low $50 \Omega$ Insertion Loss: 2.5 dB at 100 MHz
- $\pm 2.7 \mathrm{~V}$ to $\pm 6 \mathrm{~V}$ Dual Supplies +2.7 V to +12 V Single Supply
- Low Power Consumption: $<1 \mu \mathrm{~W}$
- Rail-to-Rail Bidirectional Signal Handling
- Pin Compatible with Industry-Standard DG540, DG542, DG643
- $\quad$ 2kV ESD Protection per Method 3015.7
- TTL/CMOS-Compatible Inputs with Single +5 V or $\pm 5 \mathrm{~V}$


## Ordering Information

| PART | TEMP. RANGE | PIN-PACKAGE |
| :--- | :---: | :--- |
| MAX4565CPP | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ | 20 Plastic DIP |
| MAX4565CWP | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ | 20 Wide SO |

Ordering Information continued at end of data sheet.

## Pin Configurations/Functional Diagrams/Truth Tables



19-1252; Rev 1; 2/21

[^0]
## Quad/Dual, Low-Voltage, Bidirectional RF/Video Switches

|  |  |
| :---: | :---: |
| (Voltages Referenced to GND) |  |
|  | V+................................................................-0.3V, +13.0V |
|  | -13.0V, +0.3V |
| $\mathrm{V}+$ to V - .................................................. - $0.3 \mathrm{~V},+13.0 \mathrm{~V}$All Other Pins (Note 1) ...................(V- 0.3 V$)$ to ( $\mathrm{V}++0.3 \mathrm{~V}$ ) |  |
|  |  |
| Continuous Current into Any Terminal.......................... $\pm 25 \mathrm{~mA}$ |  |
| Peak Current into Any Terminal (pulsed at $1 \mathrm{~ms}, 10 \%$ duty cycle) $\qquad$ |  |
| ESD per Method 3015.7...........................................>2000V |  |
| Continuous Power Dissipation ( $\left.\mathrm{T}_{\mathrm{A}}=+70^{\circ} \mathrm{C}\right)($ Note 2) |  |
|  | 16-Pin Plastic DIP <br> (derate $10.53 \mathrm{~mW} /{ }^{\circ} \mathrm{C}$ above $+70^{\circ} \mathrm{C}$ ) .842 mW |


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Note 1: Voltages on all other pins exceeding $\mathrm{V}+$ or V - are clamped by internal diodes. Limit forward diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## Electrical Characteristics—Dual Supplies

$\left(\mathrm{V}+=+4.5 \mathrm{~V}\right.$ to $+5.5 \mathrm{~V}, \mathrm{~V}-=-4.5 \mathrm{~V}$ to $-5.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{INL}}=0.8 \mathrm{~V}, \mathrm{~V}_{\mathrm{INH}}=2.4 \mathrm{~V}, \mathrm{~V}_{\mathrm{GND}}=0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=\mathrm{T}_{\mathrm{MIN}}$ to $\mathrm{T}_{\mathrm{MAX}}$, unless otherwise noted. Typical values are at $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$.)

| PARAMETER | SYMBOL | CONDITIONS | $\mathrm{T}_{\mathrm{A}}$ | MIN | $\begin{aligned} & \text { TYP } \\ & \text { (Note 2) } \end{aligned}$ | MAX | UNITS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| ANALOG SWITCH |  |  |  |  |  |  |  |
| Analog Signal Range | $\begin{gathered} \mathrm{V}_{\mathrm{COM}} \\ \mathrm{~V}_{\mathrm{NO}}, \mathrm{~V}_{\mathrm{NC}} \end{gathered}$ | (Note 3) | C, E | V- |  | V+ | V |
| Signal-Path On-Resistance | $\mathrm{R}_{\mathrm{ON}}$ | $\begin{aligned} & \mathrm{V}+=4.5 \mathrm{~V}, \mathrm{~V}-=-4.5 \mathrm{~V}, \\ & \mathrm{~V}_{\text {COM }}= \pm 2 \mathrm{~V}, \mathrm{I}_{\mathrm{COM}}=10 \mathrm{~mA} \end{aligned}$ | $+25^{\circ} \mathrm{C}$ |  | 46 | 60 | $\Omega$ |
|  |  |  | C, E |  |  | 80 |  |
| Signal-Path On-Resistance Match Between Channels (Note 4) | $\Delta \mathrm{R}_{\text {ON }}$ | $\begin{aligned} & \mathrm{V}+=4.5 \mathrm{~V}, \mathrm{~V}-=-4.5 \mathrm{~V}, \\ & \mathrm{~V}_{\text {COM }}= \pm 2 \mathrm{~V}, \mathrm{I}_{\text {COM }}=10 \mathrm{~mA} \end{aligned}$ | $+25^{\circ} \mathrm{C}$ |  | 1 | 2.5 | $\Omega$ |
|  |  |  | C, E |  |  | 3 |  |
| Signal-Path On-Resistance Flatness (Note 5) | $\mathrm{R}_{\text {FLAT(ON) }}$ | $\begin{aligned} & \mathrm{V}+=5 \mathrm{~V} ; \mathrm{V}-=-5 \mathrm{~V} ; \mathrm{V}_{\mathrm{COM}}=1 \mathrm{~V}, \\ & 0 \mathrm{~V},-1 \mathrm{~V} ; \mathrm{I}_{\mathrm{COM}}=10 \mathrm{~mA} \end{aligned}$ | $+25^{\circ} \mathrm{C}$ |  | 0.3 | 2 | $\Omega$ |
| NO_, NC_Off Leakage Current (Note 6) | $\mathrm{I}_{\mathrm{NO} \text { _(OFF) }}$, <br> $\mathrm{I}_{\text {NC_(OFF) }}$ | $\begin{aligned} & \mathrm{V}+=5.5 \mathrm{~V}, \mathrm{~V}-=-5.5 \mathrm{~V}, \\ & \mathrm{~V}_{\mathrm{COM}_{-}}= \pm 4.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{N}_{-}}= \pm 4.5 \mathrm{~V} \\ & \hline \end{aligned}$ | $+25^{\circ} \mathrm{C}$ | -1 | 0.02 | 1 | nA |
|  |  |  | C, E | -10 |  | 10 |  |
| COM_Off Leakage Current (Note 6) | $\mathrm{I}_{\text {COM_(OFF) }}$ | $\begin{aligned} & \mathrm{V}+=5.5 \mathrm{~V}, \mathrm{~V}-=-5.5 \mathrm{~V}, \\ & \mathrm{~V}_{\mathrm{COM}_{-}}= \pm 4.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{N}_{-}}= \pm 4.5 \mathrm{~V} \end{aligned}$ | $+25^{\circ} \mathrm{C}$ | -1 | 0.02 | 1 | nA |
|  |  |  | C, E | -10 |  | 10 |  |
| COM_On Leakage Current (Note 6) | $\mathrm{I}_{\text {COM_(ON) }}$ | $\begin{aligned} & \mathrm{V}+=5.5 \mathrm{~V}, \mathrm{~V}-=-5.5 \mathrm{~V} \\ & \mathrm{~V}_{\text {COM }}= \pm 4.5 \mathrm{~V} \end{aligned}$ | $+25^{\circ} \mathrm{C}$ | -2 | 0.04 | 2 | nA |
|  |  |  | C, E | -20 |  | 20 |  |
| LOGIC INPUT |  |  |  |  |  |  |  |
| IN_ Input Logic Threshold High | $\mathrm{V}_{\text {IN_H }}$ |  | C, E |  | 1.5 | 2.4 | V |
| IN_ Input Logic Threshold Low | $\mathrm{V}_{\text {IN_L }}$ |  | C, E | 0.8 | 1.5 |  | V |
| IN_ Input Current Logic High or Low | $\mathrm{I}_{\mathrm{INH}}{ }^{\text {, }} \mathrm{INL}^{\text {L }}$ | $\mathrm{V}_{\text {IN_ }}=0.8 \mathrm{~V}$ or 2.4 V | C, E | -1 | 0.03 | 1 | $\mu \mathrm{A}$ |

## Electrical Characteristics-Dual Supplies (continued)

$\left(\mathrm{V}+=+4.5 \mathrm{~V}\right.$ to $+5.5 \mathrm{~V}, \mathrm{~V}-=-4.5 \mathrm{~V}$ to $-5.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{INL}}=0.8 \mathrm{~V}, \mathrm{~V}_{\mathrm{INH}}=2.4 \mathrm{~V}, \mathrm{~V}_{\mathrm{GND}}=0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=\mathrm{T}_{\mathrm{MIN}}$ to $\mathrm{T}_{\mathrm{MAX}}$, unless otherwise noted. Typical values are at $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$.)

| PARAMETER | SYMBOL | CONDITIONS |  | $\mathrm{T}_{\text {A }}$ | MIN | $\begin{aligned} & \text { TYP } \\ & \text { (Note 2) } \end{aligned}$ | MAX | UNITS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SWITCH DYNAMIC CHARACTERISTICS |  |  |  |  |  |  |  |  |
| Turn-On Time | ${ }^{\text {ton }}$ | $\begin{aligned} & \mathrm{V}_{\mathrm{COM}}= \pm 3 \mathrm{~V}, \mathrm{~V}+=5 \mathrm{~V}, \\ & \mathrm{~V}-=-5 \mathrm{~V} \text {, Figure } 3 \end{aligned}$ |  | $+25^{\circ} \mathrm{C}$ |  | 75 | 150 | ns |
|  |  |  |  | C, E |  |  | 200 |  |
| Turn-Off Time | ${ }^{\text {tofF }}$ | $\begin{aligned} & \mathrm{V}_{\mathrm{COM}}= \pm 3 \mathrm{~V}, \mathrm{~V}+=5 \mathrm{~V}, \\ & \mathrm{~V}-=-5 \overline{\mathrm{~V}} \text {, Figure } 3 \end{aligned}$ |  | $+25^{\circ} \mathrm{C}$ |  | 30 | 100 | ns |
|  |  |  |  | C, E |  |  | 120 |  |
| Break-Before-Make Time Delay (MAX4566/MAX4567 only) | $t_{\text {BBM }}$ | $\begin{aligned} & \mathrm{V}_{\mathrm{COM}}= \pm 3 \mathrm{~V}, \mathrm{~V}+=5 \mathrm{~V}, \\ & \mathrm{~V}-=-5 \mathrm{~V} \text {, Figure } 4 \end{aligned}$ |  | $+25^{\circ} \mathrm{C}$ | 5 | 30 |  | ns |
| Charge Injection (Note 3) | Q | $\begin{aligned} & \mathrm{C}_{\mathrm{L}}=1.0 \mathrm{nF}, \mathrm{~V}_{\mathrm{NO}}=0 \mathrm{~V}, \\ & \mathrm{R}_{\mathrm{S}}=0 \Omega \text {, Figure } \overline{5} \end{aligned}$ |  | $+25^{\circ} \mathrm{C}$ |  | 25 | 60 | pC |
| NO_, NC_Off Capacitance | $\mathrm{C}_{\mathrm{N} \text { _(OFF) }}$ | $\mathrm{V}_{\mathrm{NO}_{-}}=\mathrm{GND}, \mathrm{f}=1 \mathrm{MHz},$ <br> Figure 7 |  | $+25^{\circ} \mathrm{C}$ |  | 2.5 |  | pF |
| COM_Off Capacitance | $\mathrm{C}_{\text {COM_(OFF) }}$ | $\begin{aligned} & \mathrm{V}_{\mathrm{COM}}=0 \mathrm{~V}, \\ & \mathrm{f}=1 \mathrm{MHz} \end{aligned}$ <br> Figure 7 | MAX4565 | $+25^{\circ} \mathrm{C}$ | 2.5 |  |  | pF |
|  |  |  | MAX4566 |  |  |  |  |  |
| COM_On Capacitance | $\mathrm{C}_{\text {COM_(ON) }}$ | $\begin{aligned} & V_{\mathrm{COM}}=\mathrm{V}_{\mathrm{NO}}=0 \mathrm{~V}, \\ & \mathrm{f}=1 \mathrm{MHz}, \text { Figure } 7 \end{aligned}$ | MAX4565 | $+25^{\circ} \mathrm{C}$ |  | 6 |  | pF |
|  |  |  | MAX4566 |  |  | 6 |  |  |
|  |  |  | MAX4567 |  |  | 7 |  |  |
| Off Isolation (Note 7) | $\mathrm{V}_{\text {ISO }}$ | $\begin{aligned} & R_{\mathrm{L}}=50 \Omega, \\ & \mathrm{~V}_{\mathrm{COM}}=1 \mathrm{~V}_{\mathrm{RMS}}, \\ & \mathrm{f}=10 \mathrm{MHz}, \text { Figure } 6 \end{aligned}$ | MAX4565 | $+25^{\circ} \mathrm{C}$ |  | -83 |  | dB |
|  |  |  | MAX4566 |  |  | -82 |  |  |
|  |  |  | MAX4567 |  |  | -83 |  |  |
| Channel-to-Channel Crosstalk (Note 8) | $\mathrm{V}_{\mathrm{CT}}$ | $\begin{aligned} & R_{L}=50 \Omega, \\ & V_{C O M}=1 V_{R M S}, \\ & f=10 \overline{M H z} \text {, Figure } 6 \end{aligned}$ | MAX4565 | $+25^{\circ} \mathrm{C}$ |  | -92 |  | dB |
|  |  |  | MAX4566 |  |  | -85 |  |  |
|  |  |  | MAX4567 |  |  | -87 |  |  |
| -3dB Bandwidth (Note 9) | BW | Figure 6, $\mathrm{R}_{\mathrm{L}}=50 \Omega$ |  | $+25^{\circ} \mathrm{C}$ |  | 350 |  | MHz |
| Distortion | THD+N | $\mathrm{V}_{\mathrm{IN}}=5 \mathrm{Vp}-\mathrm{p}, \mathrm{f}<20 \mathrm{kHz},$ <br> $600 \Omega$ in and out |  | $+25^{\circ} \mathrm{C}$ |  | 0.02 |  | \% |
| POWER SUPPLY |  |  |  |  |  |  |  |  |
| Power-Supply Range | V+, V- |  |  | C, E | -6 |  | +6 | V |
| V+ Supply Current | I+ | $\mathrm{V}+=5.5 \mathrm{~V}$, all $\mathrm{V}_{\text {IN_ }}=0 \mathrm{~V}$ or $\mathrm{V}^{+}$ |  | $+25^{\circ} \mathrm{C}$ | -1 | 0.05 | 1 | $\mu \mathrm{A}$ |
|  |  |  |  | C, E | -10 |  | 10 |  |
| V - Supply Current | I- | $\mathrm{V}-=-5.5 \mathrm{~V}$ |  | $+25^{\circ} \mathrm{C}$ | -1 | 0.05 | 1 | $\mu \mathrm{A}$ |
|  |  |  |  | C, E | -10 |  | 10 |  |

## Electrical Characteristics—Single +5V Supply

$\left(\mathrm{V}+=+4.5 \mathrm{~V}\right.$ to $+5.5 \mathrm{~V}, \mathrm{~V}-=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{INL}}=0.8 \mathrm{~V}, \mathrm{~V}_{\mathrm{INH}}=2.4 \mathrm{~V}, \mathrm{~V}_{\mathrm{GND}_{-}}=0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=\mathrm{T}_{\mathrm{MIN}}$ to $\mathrm{T}_{\mathrm{MAX}}$, unless otherwise noted. Typical values are at $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$.)

| PARAMETER | SYMBOL | CONDITIONS | $\mathrm{T}_{\text {A }}$ | MIN | $\begin{gathered} \text { TYP } \\ \text { (Note 2) } \end{gathered}$ | MAX | UNITS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| ANALOG SWITCH |  |  |  |  |  |  |  |
| Analog Signal Range | $\begin{gathered} \mathrm{V}_{\mathrm{COM}} \\ \mathrm{~V}_{\mathrm{NO}}, \mathrm{~V}_{\mathrm{NC}}^{-} \end{gathered}$ | (Note 3) | $+25^{\circ} \mathrm{C}$ | 0 |  | V+ | V |
| Signal-Path On-Resistance | $\mathrm{R}_{\mathrm{ON}}$ | $\begin{aligned} & \mathrm{V}+=4.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{COM}}=3.5 \mathrm{~V}, \\ & \mathrm{I}_{\mathrm{COM}}^{-}=1 \mathrm{~mA} \end{aligned}$ | $+25^{\circ} \mathrm{C}$ |  | 68 | 120 | $\Omega$ |
|  |  |  | C, E |  |  | 150 |  |
| Signal-Path On-Resistance Match | $\Delta \mathrm{R}_{\mathrm{ON}}$ | $\begin{aligned} & \mathrm{V}+=4.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{COM}}=3.5 \mathrm{~V}, \\ & \mathrm{I}_{\mathrm{COM}}^{-}=1 \mathrm{~mA} \end{aligned}$ | $+25^{\circ} \mathrm{C}$ |  | 2 | 5 | $\Omega$ |
|  |  |  | C, E |  |  | 6 |  |
| NO_, NC_Off Leakage Current (Notes 6, 10) | ${ }^{\text {In }}$ NO_(OFF), ${ }^{\text {I }}$ NC_(OFF) | $\begin{aligned} & \mathrm{V}+=5.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{COM}_{-}}=1 \mathrm{~V}, \\ & \mathrm{~V}_{\mathrm{N}_{-}}=4.5 \mathrm{~V} \end{aligned}$ | $+25^{\circ} \mathrm{C}$ | -1 |  | 1 | nA |
|  |  |  | C, E | -10 |  | 10 |  |
| COM_Off Leakage Current (Notes 6, 10) | ICOM_(OFF) | $\begin{aligned} & \mathrm{V}+=5.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{COM}}=1 \mathrm{~V}, \\ & \mathrm{~V}_{\mathrm{N}_{-}}=4.5 \mathrm{~V} \end{aligned}$ | $+25^{\circ} \mathrm{C}$ | -1 |  | 1 | nA |
|  |  |  | C, E | -10 |  | 10 |  |
| COM_On Leakage Current (Notes 6, 10) | ICOM_(ON) | $\mathrm{V}+=5.5 \mathrm{~V} ; \mathrm{V}_{\text {COM }}=1 \mathrm{~V}, 4.5 \mathrm{~V}$ | $+25^{\circ} \mathrm{C}$ | -2 |  | 2 | nA |
|  |  |  | C, E | -20 |  | 20 |  |
| LOGIC INPUT |  |  |  |  |  |  |  |
| IN_ Input Logic Threshold High | $\mathrm{V}_{\mathrm{IN}} \mathrm{H}$ |  | C, E |  | 1.5 | 2.4 | V |
| IN_ Input Logic Threshold Low | $\mathrm{V}_{\text {IN L }}$ |  | C, E | 0.8 | 1.5 |  | V |
| IN_ Input Current Logic High or Low | ${ }^{\text {I }}{ }_{\text {NH_, }} \mathrm{I}_{\text {INL }}$ | $\mathrm{V}_{\text {IN_ }}=0.8 \mathrm{~V}$ or 2.4 V | C, E | -1 | 0.001 | 1 | $\mu \mathrm{A}$ |
| SWITCH DYNAMIC CHARACTERISTICS |  |  |  |  |  |  |  |
| Turn-On Time | ${ }^{\text {toN }}$ | $\mathrm{V}_{\mathrm{COM}}=3 \mathrm{~V}, \mathrm{~V}+=5 \mathrm{~V},$ <br> Figure 3 | $+25^{\circ} \mathrm{C}$ |  | 130 | 200 | ns |
|  |  |  | C, E |  |  | 250 |  |
| Turn-Off Time | ${ }^{\text {tofF }}$ | $\mathrm{V}_{\mathrm{COM}}=3 \mathrm{~V}, \mathrm{~V}+=5 \mathrm{~V} \text {, }$ <br> Figure 3 | $+25^{\circ} \mathrm{C}$ |  | 30 | 120 | ns |
|  |  |  | C, E |  |  | 150 |  |
| Break-Before-Make Time Delay (MAX4566/MAX4567 only) | $\mathrm{t}_{\text {BBM }}$ | $\mathrm{V}_{\mathrm{COM}}=3 \mathrm{~V}, \mathrm{~V}+=5 \mathrm{~V},$ <br> Figure 4 | $+25^{\circ} \mathrm{C}$ | 10 | 90 |  | ns |
| Charge Injection | Q | $\begin{aligned} & C_{\mathrm{L}}=1.0 \mathrm{nF}, \mathrm{~V}_{\mathrm{NO}}=2.5 \mathrm{~V}, \\ & \mathrm{R}_{\mathrm{S}}=0 \Omega, \text { Figure } 5 \end{aligned}$ | $+25^{\circ} \mathrm{C}$ |  | 7 | 25 | pC |
| Off-Isolation (Note 7) | $\mathrm{V}_{\text {ISO }}$ | $\begin{aligned} & R_{\mathrm{L}}=50 \Omega, \mathrm{f}=10 \mathrm{MHz}, \\ & \mathrm{~V}_{\mathrm{COM}}=1 \mathrm{~V}_{\mathrm{RMS}}, \text { Figure } 6 \end{aligned}$ | $+25^{\circ} \mathrm{C}$ |  | -81 |  | dB |
| Channel-to-Channel Crosstalk (Note 8) | $\mathrm{V}_{\mathrm{CT}}$ | $\begin{aligned} & R_{\mathrm{L}}=50 \Omega, \mathrm{f}=10 \mathrm{MHz}, \\ & \mathrm{~V}_{\mathrm{COM}}=1 \mathrm{~V}_{\mathrm{RMS}}, \text { Figure } 6 \end{aligned}$ | $+25^{\circ} \mathrm{C}$ |  | -86 |  | dB |
| -3dB Bandwidth (Note 9) | BW | $\mathrm{R}_{\mathrm{L}}=50 \Omega$, Figure 6 | $+25^{\circ} \mathrm{C}$ |  | 320 |  | MHz |
| POWER SUPPLY |  |  |  |  |  |  |  |
| V+ Supply Current | I+ | $\mathrm{V}+=5.5 \mathrm{~V}$, all $\mathrm{V}_{1 \mathrm{~N}_{-}}=0 \mathrm{~V}$ or $\mathrm{V}+$ | $+25^{\circ} \mathrm{C}$ | -1 | 0.05 | 1 | $\mu \mathrm{A}$ |
|  |  |  | C, E | -10 |  | 10 |  |

## Quad/Dual, Low-Voltage, Bidirectional RF/Video Switches

## Electrical Characteristics-Single +3V Supply

$\left(\mathrm{V}+=+2.7 \mathrm{~V}\right.$ to $+3.6 \mathrm{~V}, \mathrm{~V}-=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{INL}}=0.8 \mathrm{~V}, \mathrm{~V}_{\mathrm{INH}}=2.4 \mathrm{~V}, \mathrm{~V}_{\mathrm{GND}}=0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=\mathrm{T}_{\mathrm{MIN}}$ to $\mathrm{T}_{\mathrm{MAX}}$, unless otherwise noted. Typical values are at $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$.)

| PARAMETER_ | SYMBOL | CONDITIONS | $\mathrm{T}_{\text {A }}$ | MIN | $\begin{gathered} \text { TYP } \\ \text { (Note 2) } \end{gathered}$ | MAX | UNITS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| ANALOG SWITCH |  |  |  |  |  |  |  |
| Analog Signal Range | $\begin{gathered} \mathrm{V}_{\mathrm{COM}}, \\ \mathrm{~V}_{\mathrm{NO}_{-}}, \mathrm{V}_{\mathrm{NC}}^{-} \end{gathered}$ | (Note 3) | $+25^{\circ} \mathrm{C}$ | 0 |  | V+ | V |
| Signal-Path On-Resistance | $\mathrm{R}_{\mathrm{ON}}$ | $\begin{aligned} & \mathrm{V}+=2.7 \mathrm{~V}, \mathrm{~V}_{\mathrm{COM}}=1 \mathrm{~V}, \\ & \mathrm{I}_{\mathrm{COM}}=1 \mathrm{~mA} \end{aligned}$ | $+25^{\circ} \mathrm{C}$ |  | 150 | 350 | $\Omega$ |
|  |  |  | C, E |  |  | 450 |  |
| LOGIC INPUT |  |  |  |  |  |  |  |
| IN_ Input Logic Threshold High | $\mathrm{V}_{\mathrm{IN} \text { H }}$ | (Note 3) | C, E |  | 1.0 | 2.4 | V |
| IN_ Input Logic Threshold Low | $\mathrm{V}_{\text {IN L }}$ | (Note 3) | C, E | 0.8 | 1.0 |  | V |
| IN_ Input Current Logic High or Low | ${ }^{\text {I }}{ }_{\text {NH_- }} \mathrm{I}_{\text {INL }}$ | $\mathrm{V}_{1 \mathrm{~N}_{-}}=0.8 \mathrm{~V}$ or 2.4 V (Note 3 ) | C, E | -1 |  | 1 | $\mu \mathrm{A}$ |
| SWITCH DYNAMIC CHARACTERISTICS (Note 3) |  |  |  |  |  |  |  |
| Turn-On Time | ${ }^{\text {toN }}$ | $\mathrm{V}_{\mathrm{COM}_{-}}=1.5 \mathrm{~V}, \mathrm{~V}+=2.7 \mathrm{~V},$ <br> Figure 3 (Note 3) | $+25^{\circ} \mathrm{C}$ |  | 270 | 500 | ns |
|  |  |  | C, E |  |  | 600 |  |
| Turn-Off Time | ${ }^{\text {tofF }}$ | $\begin{aligned} & \mathrm{V}_{\mathrm{COM}}=1.5 \mathrm{~V}, \mathrm{~V}+=2.7 \mathrm{~V}, \\ & \text { Figure } 3 \text { (Note 3) } \end{aligned}$ | $+25^{\circ} \mathrm{C}$ |  | 40 | 100 | ns |
|  |  |  | C, E |  |  | 120 |  |
| Break-Before-Make Time Delay (MAX4566/MAX4567 only) | ${ }^{\text {t }}$ BBM | $\begin{aligned} & \mathrm{V}_{\mathrm{COM}}=1.5 \mathrm{~V}, \mathrm{~V}+=2.7 \mathrm{~V}, \\ & \text { Figure } \\ & \hline \text { (Note 3) } \end{aligned}$ | $+25^{\circ} \mathrm{C}$ | 10 | 120 |  | ns |
| POWER SUPPLY |  |  |  |  |  |  |  |
| V+ Supply Current | + | $\mathrm{V}+=3.6 \mathrm{~V}$, all $\mathrm{V}_{\text {IN_- }}=0 \mathrm{~V}$ or $\mathrm{V}+$ | $+25^{\circ} \mathrm{C}$ | -1 | 0.05 | 1 | $\mu \mathrm{A}$ |
|  |  |  | C, E | -10 |  | 10 |  |

Note 2: The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.
Note 3: Guaranteed by design.
Note 4: $\quad \Delta R_{\mathrm{ON}}=\Delta \mathrm{R}_{\mathrm{ON}(\mathrm{MAX})}-\Delta \mathrm{R}_{\mathrm{ON}(\mathrm{MIN})}$.
Note 5: Resistance flatness is defined as the difference between the maximum and the minimum value of on-resistance as measured over the specified analog signal range.
Note 6: Leakage parameters are $100 \%$ tested at the maximum rated hot temperature and guaranteed by correlation at $+25^{\circ} \mathrm{C}$.
Note 7: Off isolation $=20 \log _{10}\left[\mathrm{~V}_{\mathrm{COM}} /\left(\mathrm{V}_{\mathrm{NC}}\right.\right.$ or $\left.\left.\mathrm{V}_{\mathrm{NO}}\right)\right], \mathrm{V}_{\mathrm{COM}}=$ output, $\mathrm{V}_{\mathrm{NC}}$ or $\mathrm{V}_{\mathrm{NO}}=$ input to off switch.
Note 8: Between any two switches.
Note 9: -3dB bandwidth is measured relative to 100 kHz .
Note 10: Leakage testing for single-supply operation is guaranteed by testing with dual supplies.

## Quad/Dual, Low-Voltage, Bidirectional RF/Video Switches

## Typical Operating Characteristics

$\left(\mathrm{V}+=+5 \mathrm{~V}, \mathrm{~V}-=-5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}, \mathrm{GND}=0 \mathrm{~V}\right.$, packages are surface mount, unless otherwise noted.)


## Typical Operating Characteristics (continued)

$\left(\mathrm{V}+=+5 \mathrm{~V}, \mathrm{~V}-=-5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}, \mathrm{GND}=0 \mathrm{~V}\right.$, packages are surface mount, unless otherwise noted.)


MAX4567
TOTAL HARMONIC DISTORTION
vs. FREQUENCY


## Quad/Dual, Low-Voltage, Bidirectional RF/Video Switches

## Pin Description

| PIN |  |  | NAME | FUNCTION* |
| :---: | :---: | :---: | :---: | :--- |
| MAX4565 | MAX4566 | MAX4567 |  |  |
| $1,10,11$, <br> 20 | 1,16 | 1,9 | IN_ $^{*}$ | Digital Control Input |
| $3,6,8,13$, <br> 15,18 | $3,7,10,14$ | $4,6,12,14$ | GND_ $^{\prime}$ | RF and Logic Ground. Grounds are not internally connected to each other, <br> and should all be connected to a ground plane (see Grounding section). |
| 16 | 12 | 7,15 | V+ | Positive Supply-Voltage Input (analog and digital) |
| 5 | 5 | 3,11 | V- | Negative Supply-Voltage Input. Connect to ground plane for single-supply <br> operation. |
| $4,7,14,17$ | 4,13 | 2,16 | NO_ | Analog Switch Normally Open** Terminals |
| - | 6,11 | 8,10 | NC_ | Analog Switch Normally Closed** Terminals |
| $2,9,12,19$ | $2,8,9,15$ | 5,13 | COM_ | Analog Switch Common** Terminals |

* All pins have ESD diodes to $V$ - and $V+$.
** NO_ (or NC_) and COM_ pins are identical and interchangeable. Either may be considered as an input or output; signals pass equally well in either direction.


## Theory of Operation

The MAX4565/MAX4566/MAX4567 are high-frequency "T" switches. Each "T" switch consists of two series CMOS switches, with a third N-channel switch at the junction that shunts capacitively-coupled signals to ground when the series switches are off. This produces superior high-frequency signal isolation when the switch is turned off.

## Logic-Level Translators

The MAX4565/MAX4566/MAX4567 are constructed as high-frequency "T" switches, as shown in Figure 1. The logic-level input, IN_, is translated by amplifier A1 into a V+ to V - logic signal that drives amplifier A 2 . (Amplifier A2 is an inverter for normally closed switches.) Amplifier A2 drives the gates of N -channel MOSFETs N 1 and N 2 from $\mathrm{V}+$ to V-, turning them fully on or off. The same signal drives inverter A3 (which drives the P-channel MOSFETs P1 and P2) from $V+$ to $V$-, turning them fully on or off, and drives the N -channel MOSFET N3 off and on.
The logic-level threshold is determined by $\mathrm{V}+$ and GND_. The voltage on GND_ is usually at ground potential, but it may be set to any voltage between ( $\mathrm{V}+-2 \mathrm{~V}$ ) and V -. When the voltage between $\mathrm{V}+$ and $\mathrm{GND}_{-}$is less than 2 V , the level translators become very slow and unreliable. Since individual switches in each package have individual GND_pins, they may be set to different voltages. Normally, however, they should all be connected to the ground plane.


Figure 1. T-Switch Construction

## Switch On Condition

When the switch is on, MOSFETs N1, N2, P1, and P2 are on and MOSFET N3 is off. The signal path is COM_ to NO_, and because both N-channel and P-channel MOSFETs act as pure resistances, it is symmetrical (i.e., signals may pass in either direction). The off MOSFET, N3, has no DC conduction, but has a small

## Quad/Dual, Low-Voltage, Bidirectional RF/Video Switches

amount of capacitance to GND_. The four on MOSFETs also have capacitance to ground that, together with the series resistance, forms a lowpass filter. All of these capacitances are distributed evenly along the series resistance, so they act as a transmission line rather than a simple R-C filter. This helps to explain the exceptional 350 MHz bandwidth when the switches are on.

Typical attenuation in $50 \Omega$ systems is -2.5 dB and is reasonably flat up to 300 MHz . Higher-impedance circuits show even lower attenuation (and vice versa), but slightly lower bandwidth due to the increased effect of the internal and external capacitance and the switch's internal resistance.
The MAX4565/MAX4566/MAX4567 are optimized for $\pm 5 \mathrm{~V}$ operation. Using lower supply voltages or a single supply increases switching time, increases on-resistance (and therefore on-state attenuation), and increases nonlinearity.

## Switch Off Condition

When the switch is off, MOSFETs $\mathrm{N} 1, \mathrm{~N} 2, \mathrm{P} 1$, and P 2 are off and MOSFET N3 is on. The signal path is through the off-capacitances of the series MOSFETs, but it is shunted to ground by N3. This forms a highpass filter whose exact characteristics are dependent on the source and load impedances. In $50 \Omega$ systems, and below 10 MHz , the attenuation can exceed 80 dB . This value decreases with increasing frequency and increasing circuit impedances. External capacitance and board layout have a major role in determining overall performance.

## Applications Information

## Power-Supply Considerations

## Overview

The MAX4565/MAX4566/MAX4567 construction is typical of most CMOS analog switches. It has three supply pins: $\mathrm{V}+$, V -, and GND. $\mathrm{V}+$ and V - are used to drive the internal CMOS switches and set the limits of the analog voltage on any switch. Reverse ESD protection diodes are internally connected between each analog signal pin and both $\mathrm{V}+$ and V -. If the voltage on any pin exceeds $\mathrm{V}+$ or V -, one of these diodes will conduct. During normal operation these reverse-biased ESD diodes leak, forming the only current drawn from V -.
Virtually all the analog leakage current is through the ESD diodes. Although the ESD diodes on a given signal pin are identical, and therefore fairly well balanced, they are reverse biased differently. Each is biased by either $\mathrm{V}+$ or V - and the analog signal. This means their
leakages vary as the signal varies. The difference in the two diode leakages from the signal path to the $\mathrm{V}+$ and V pins constitutes the analog signal-path leakage current. All analog leakage current flows to the supply terminals, not to the other switch terminal. This explains how both sides of a given switch can show leakage currents of either the same or opposite polarity.
There is no connection between the analog signal paths and GND. The analog signal paths consist of an N -channel and P-channel MOSFET with their sources and drains paralleled and their gates driven out of phase with $\mathrm{V}+$ and V - by the logic-level translators.
V+ and GND power the internal logic and logic-level translators, and set the input logic thresholds. The logic-level translators convert the logic levels to switched $\mathrm{V}+$ and V - signals to drive the gates of the analog switches. This drive signal is the only connection between the logic supplies and the analog supplies. All pins have ESD protection to $\mathrm{V}+$ and to V -.
Increasing V - has no effect on the logic-level thresholds, but it does increase the drive to the P-channel switches, reducing their on-resistance. V- also sets the negative limit of the analog signal voltage.
The logic-level thresholds are CMOS and TTL compatible when $\mathrm{V}+$ is +5 V . As $\mathrm{V}+$ is raised, the threshold increases slightly; when $\mathrm{V}+$ reaches +12 V , the level threshold is about 3.1 V , which is above the TTL output high-level minimum of 2.8 V , but still compatible with CMOS outputs.

## Bipolar-Supply Operation

The MAX4565/MAX4566/MAX4567 operate with bipolar supplies between $\pm 2.7 \mathrm{~V}$ and $\pm 6 \mathrm{~V}$. The $\mathrm{V}+$ and V - supplies need not be symmetrical, but their sum cannot exceed the absolute maximum rating of 13.0 V . Do not connect the MAX4565/MAX4566/MAX4567 V+ pin to +3 V and connect the logic-level input pins to TTL logic-level signals. TTL logic-level outputs can exceed the absolute maximum ratings, causing damage to the part and/or external circuits.

## CAUTION:

The absolute maximum $\mathrm{V}+$ to V - differential voltage is 13.0 V . Typical " $\pm 6$-Volt" or " 12 -Volt" supplies with $\pm 10 \%$ tolerances can be as high as 13.2 V . This voltage can damage the MAX4565/MAX4566/MAX4567. Even $\pm 5 \%$ tolerance supplies may have overshoot or noise spikes that exceed 13.0 V .

## Quad/Dual, Low-Voltage, Bidirectional RF/Video Switches

## Single-Supply Operation

The MAX4565/MAX4566/MAX4567 operate from a single supply between +2.7 V and +12 V when V - is connected to GND. All of the bipolar precautions must be observed. Note, however, that these parts are optimized for $\pm 5 \mathrm{~V}$ operation, and most AC and DC characteristics are degraded significantly when departing from $\pm 5 \mathrm{~V}$. As the overall supply voltage ( $\mathrm{V}+$ to V -) is lowered, switching speed, on-resistance, off isolation, and distortion are degraded. (See Typical Operating Characteristics.)
Single-supply operation also limits signal levels and interferes with grounded signals. When $\mathrm{V}-=0 \mathrm{~V}, \mathrm{AC}$ signals are limited to -0.3 V . Voltages below -0.3 V can be clipped by the internal ESD-protection diodes, and the parts can be damaged if excessive current flows.

## Power Off

When power to the MAX4565/MAX4566/MAX4567 is off (i.e., $\mathrm{V}+=0 \mathrm{~V}$ and $\mathrm{V}-=0 \mathrm{~V}$ ), the Absolute Maximum Ratings still apply. This means that neither logic-level inputs on IN_ nor signals on COM_, NO_, or NC_ can exceed $\pm 0.3 \overline{\mathrm{~V}}$. Voltages beyond $\pm 0 . \overline{\mathrm{V}}$, cause the internal ESD-protection diodes to conduct, and the parts can be damaged if excessive current flows.

## Grounding

## DC Ground Considerations

Satisfactory high-frequency operation requires that careful consideration be given to grounding. For most applications, a ground plane is strongly recommended, and all GND_ pins should be connected to it with solid copper. While the $\mathrm{V}+$ and V - power-supply pins are common to all switches in a given package, each switch has separate ground pins that are not internally connected to each other. This contributes to the overall high-frequency performance and provides added flexibility in some applications, but it can cause problems if it is overlooked. All the GND_ pins have ESD diodes to $\mathrm{V}+$ and V -.
In systems that have separate digital and analog (signal) grounds, connect these switch GND_ pins to analog ground. Preserving a good signal ground is much more important than preserving a digital ground.
The logic-level inputs, $\mathbb{I N}_{2}$, have voltage thresholds determined by $\mathrm{V}+$ and GND.. (V- does not influence the logic-level threshold.) With +5 V and 0 V applied to $\mathrm{V}+$ and GND_, the threshold is about 1.6 V , ensuring compatibility with TTL- and CMOS-logic drivers.
The various GND_ pins can be connected to separate voltage potentials if any or all of the logic-level inputs is
not a normal logic signal. (The GND_ voltages cannot exceed ( $\mathrm{V}+-2 \mathrm{~V}$ ) or V -.) Elevating GND_ reduces off isolation. For example, using the MAX4565, if GND2-GND6 are connected to 0 V and GND1 is connected to V -, then switches 2,3 , and 4 would be TTL/CMOS compatible, but switch 1 (IN1) could be driven with the rail-to-rail output of an op amp operating from $\mathrm{V}+$ and V -. Note, however, that $\mathbb{I N}_{-}$can be driven more negative than GND_, as far as V -. GND_ does not have to be removed from 0 V when $\mathrm{IN}_{\mathrm{N}}$ is driven from bipolar sources, but the voltage on $\mathrm{IN}_{-}$ should never exceed V-. GND_ should be separated from OV only if the logic-level threshold has to be changed.
Any GND_ pin not connected to 0 V should be bypassed to the ground plane with a surface-mount 10 nF capacitor to maintain good RF grounding. DC current in the IN_ and GND_ pins is less than 1 nA , but increases with switching frequency.
On the MAX4565 only, two extra ground pins-GND5 and GND6-are provided to improve isolation and crosstalk. They are not connected to the logic-level circuit. These pins should always be connected to the ground plane with solid copper.

## AC Ground and Bypassing

A ground plane is mandatory for satisfactory highfrequency operation. (Prototyping using hand wiring or wire-wrap boards is strongly discouraged.) Connect all OV GND_ pins to the ground plane with solid copper. (The GND_ pins extend the high-frequency ground through the package wire-frame, into the silicon itself, thus improving isolation.) The ground plane should be solid metal underneath the device, without interruptions. There should be no traces under the device itself. For DIP packages, this applies to both sides of a two-sided board. Failure to observe this will have a minimal effect on the "on" characteristics of the switch at high frequencies, but it will degrade the off isolation and crosstalk.
Bypass all $\mathrm{V}+$ and V - pins to the ground plane with sur-face-mount 10 nF capacitors. For DIP packages, mount the capacitors as close as possible to the pins on the same side of the board as the device. Do not use feedthroughs or vias for bypass capacitors.
For surface-mount packages, bypass capacitors should be mounted on the opposite side of the board from the device. In this case, use short feedthroughs or vias, directly under the $\mathrm{V}+$ and V - pins. Any GND_ pin not connected to 0 V should be similarly bypassed. If V is 0 V , connect it directly to the ground plane with solid copper. Keep all leads short.

The MAX4567 has two V+ and two V- pins. Make DC connections to only one of each to minimize crosstalk. Do not route DC current into one of the $\mathrm{V}+$ or V - pins and out the other $\mathrm{V}+$ or V - pin to other devices. The second set of $\mathrm{V}+$ and V - pins is for AC bypassing only.
For dual-supply operation, the MAX4567 should have four 10 nF bypass capacitors connected to each $\mathrm{V}+$ and V - pin as close to the package as possible. For single-supply operation, the MAX4567 should have two 10 nF bypass capacitors connected (one to each $V+$ pin) as close to the package as possible.

On the MAX4565, GND5 and GND6 should always be connected to the ground plane with solid copper to improve isolation and crosstalk.

## Signal Routing

Keep all signal leads as short as possible. Separate all signal leads from each other and other traces with the ground plane on both sides of the board. Where possible, use coaxial cable instead of printed circuit board traces.

## Board Layout

IC sockets degrade high-frequency performance and should not be used if signal bandwidth exceeds 5 MHz . Surface-mount parts, having shorter internal lead frames, provide the best high-frequency performance. Keep all bypass capacitors close to the device, and separate all signal leads with ground planes. Such grounds tend to be wedge-shaped as they get closer to the device. Use vias to connect the ground planes on each side of the board, and place the vias in the apex of the wedge-shaped grounds that separate signal leads. Logic-level signal lead placement is not critical.


Figure 2. 4-Channel Multiplexer

## MAX4565/MAX4566/

MAX4567

## Quad/Dual, Low-Voltage, Bidirectional RF/Video Switches

## Multiplexer

With its excellent off isolation, the MAX4565 is ideal for use in high-frequency video multiplexers. Figure 2 shows such an application for switching any one of four video inputs to a single output. The same circuit may be used as a demultiplexer by simply reversing the signal direction.

Stray capacitance of traces and the output capacitance of switches placed in parallel reduces bandwidth, so the outputs of no more than four individual switches should be placed in parallel to maintain a high bandwidth. If more than four mux channels are needed, the 4-channel circuit should be duplicated and cascaded.

## Test Circuits/Timing Diagrams




ALL GND_PINS ARE CONNECTED TO GROUND PLANE (OV). V- IS CONNECTED TO GND (OV) FOR SINGLE-SUPPLY OPERATION.

Figure 3. Switching Time

## Test Circuits/Timing Diagrams (continued)



Figure 4. Break-Before-Make Interval (MAX4566/MAX4567 only)

Test Circuits/Timing Diagrams (continued)


Figure 5. Charge Injection


MEASUREMENTS ARE STANDARDIZED AGAINST SHORT AT IC TERMINALS.
OFF ISOLATION IS MEASURED BETWEEN COM_ AND "OFF" NO_ OR NC_ TERMINAL ON EACH SWITCH.
ON LOSS IS MEASURED BETWEEN COM_ AND "ON" NO_ OR NC_-TERMINAL ON EACH SWITCH.
CROSSTALK IS MEASURED FROM ONE CHANNEL TO ALL OTHER CHANNELS.
SIGNAL DIRECTION THROUGH SWITCH IS REVERSED; WORST VALUES ARE RECORDED.
V- IS CONNECTED TO GND (OV) FOR SINGLE-SUPPLY OPERATION.

Figure 6. On Loss, Off Isolation, and Crosstalk

## Test Circuits/Timing

 Diagrams (continued)

ALL GND_PINS ARE CONNECTED TO GROUND PLANE (OV).

Figure 7. NO_, NC_, COM_ Capacitance

MAX4566


MAX4567


TRANSISTOR COUNT: 257
SUBSTRATE INTERNALLY CONNECTED TO V+

Ordering Information (continued)

| PART | TEMP. RANGE | PIN-PACKAGE |
| :--- | :--- | :--- |
| MAX4565CAP | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ | 20 SSOP |
| MAX4565C/D | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ | Dice* |
| MAX4565EPP | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | 20 Plastic DIP |
| MAX4565EWP | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | 20 Wide SO |
| MAX4565EAP | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | 20 SSOP |
| MAX4566CPE | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ | 16 Plastic DIP |
| MAX4566CSE | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ | 16 Narrow SO |
| MAX4566CEE | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ | 16 QSOP |
| MAX4566C/D | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ | Dice* |
| MAX4566EPE | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | 16 Plastic DIP |
| MAX4566ESE | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | 16 Narrow SO |
| MAX4566EEE | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | 16 QSOP |


| PART | TEMP. RANGE | PIN-PACKAGE |
| :--- | :--- | :--- |
| MAX4567CPE | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ | 16 Plastic DIP |
| MAX4567CSE | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ | 16 Narrow SO |
| MAX4567CEE | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ | 16 QSOP |
| MAX4567C/D | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ | Dice ${ }^{*}$ |
| MAX4567EPE | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | 16 Plastic DIP |
| MAX4567ESE | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | 16 Narrow SO |
| MAX4567EEE | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | 16 QSOP |
| MAX4565CWP+ | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ | 20 Wide SO |
| MAX4565CWP+T | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ | 20 Wide SO |
| MAX4565EWP+ | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | 20 Wide SO |
| MAX4565EWP+T | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | 20 Wide SO |
| MAX4565ESE+T | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | 16 Narrow SO |

*Contact factory for dice specifications.

## Package Information

| PACKAGE <br> TYPE | PACKAGE <br> CODE | OUTLINE <br> NO. | LAND PATTERN <br> NO. |
| :---: | :---: | :---: | :---: |
| 20 SSOP | A20+5 | $\underline{21-0056}$ | $\underline{90-0094}$ |
| 20 SOIC (W) | $\mathrm{W} 20+2$ | $\underline{21-0042}$ | $\underline{90-0108}$ |
| 20 PDIP | $\mathrm{P} 20+4$ | $\underline{21-0043}$ | NOTAVAILABLE |
| 16 SOIC (N) | $\mathrm{S} 16+1$ | $\underline{21-0041}$ | $\underline{90-0097}$ |
| 16 QSOP | $\mathrm{E} 16+1$ | $\underline{21-0055}$ | $\underline{90-0167}$ |

## Revision History

| REVISION <br> NUMBER | REVISION <br> DATE | DESCRIPTION | PAGES <br> CHANGED |
| :---: | :---: | :--- | :---: |
| 0 | $6 / 97$ | Initial Release. | - |
| 1 | $2 / 21$ | Added new packages to Ordering Information, added Package Information and <br> Revision History. | 1,16 |

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