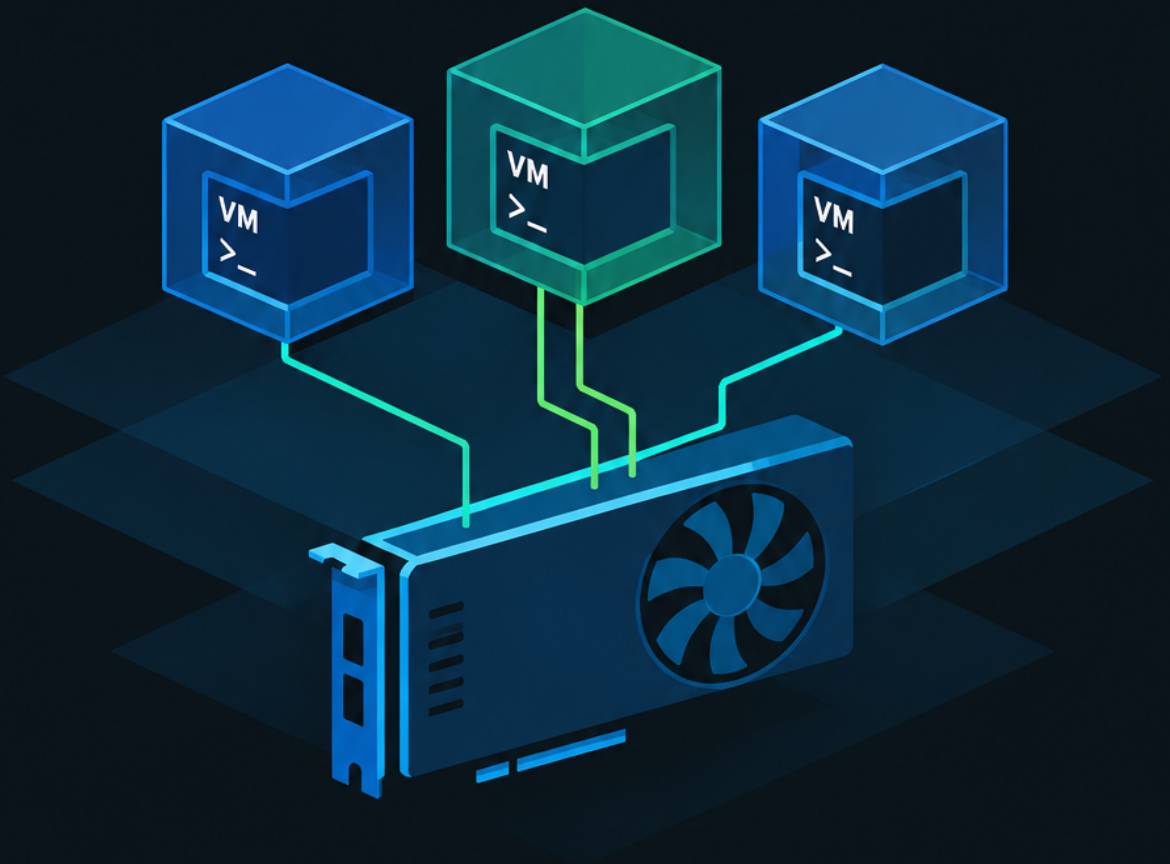


Virtual GPUs and Modern KVM Virtualization

Architectures, Implementations and
Deployment Patterns for Near-Native
GPU Access in Virtual Machines



Viktor Neumann

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Architectures, Implementations and Deployment Patterns for Near-Native GPU Access in Virtual Machines

About this book

This book is a technically rigorous treatment of GPU virtualization on Linux, focused on the KVM/QEMU stack and the emerging virtio-nvgpu architecture for shared NVIDIA GPU access in virtual machines. It covers the complete technology stack from hardware fundamentals through production deployment, with working configurations, architecture diagrams and source code analysis drawn from upstream Linux kernel, QEMU and NVIDIA implementations. The audience is experienced systems engineers who need to understand not just how to deploy GPU virtualization, but how the entire stack works internally.

Introduction

In September 2026, a research team from Nestri Labs demonstrated something that until then had been reserved for proprietary enterprise platforms: four Linux virtual machines sharing a single consumer-grade NVIDIA GeForce RTX 3060, each running full Vulkan rendering and H.264 hardware encoding, with performance within two percent of bare metal and CPU overhead so small that the backend handler averaged one message per sixty frames. The project was called `virtio-nvgpu`, it was experimental, it carried explicit warnings about its security posture, and within forty-eight hours of its announcement it had attracted more attention than any GPU virtualization project in the previous decade.

Why did this demonstration matter so much?

Because GPUs are expensive and they have been difficult to share.

If you wanted to run graphics workloads or CUDA compute jobs in virtual machines, the options were historically stark. You could dedicate an entire physical GPU to a single virtual machine using PCIe passthrough, achieving near-native performance at the cost of total inflexibility and zero multi-tenancy. You could buy proprietary virtual GPU solutions from NVIDIA or VMware that partitioned GPU resources across tenants through vendor-specific drivers and firmware, accepting the cost of licensing and the constraints of vendor lock-in. Or you could accept severely diminished performance through software rendering and API-level translation layers that serialized every draw call across the virtualization boundary.

There was no open solution that combined near-native performance with true resource sharing across multiple virtual machines on commodity hardware without requiring enterprise hardware or proprietary firmware.

`virtio-nvgpu` changed that calculus by taking a path that had been explored before but never completed: instead of translating graphics API calls or emulating a GPU, it forward the NVIDIA kernel driver ABI directly between guest and host. The guest runs the real NVIDIA user-mode libraries unchanged, building GPU command buffers locally, and only the driver-level `ioctl` calls cross the virtualization boundary. The result is an architecture that avoids the

serialization overhead of API translation while maintaining the flexibility of a paravirtualized device.

This book tells the story of how we arrived at this point, explains every layer of the technology stack that makes it possible, and provides the detailed technical knowledge needed to design, deploy, debug and operate GPU virtualization systems in production environments.

What You Will Learn

After reading this book, you will be able to:

- Explain the complete architecture of KVM/QEMU virtualization and how GPUs fit into the model, including EPT/NPT memory translation, vCPU scheduling, device emulation, and the KVM ioctl interface.
- Design and deploy PCIe passthrough configurations using VFIO and IOMMU for exclusive GPU assignment to virtual machines, with working configurations for NVIDIA and AMD GPUs across diverse hardware topologies.
- Implement and manage mediated device virtualization for GPU time-slicing and partitioning, including the mdev framework, NVIDIA vGPU, and Intel GVT-g architectures.
- Understand the virtio paravirtualization protocol thoroughly, including virtqueue operation, feature negotiation, device discovery, and the mechanisms that make virtio the foundation for efficient virtual I/O.
- Analyze VirtIO-GPU architecture, its command submission paths, resource management model, virglrenderer integration, and the native context extension that is reshaping GPU paravirtualization.
- Trace NVIDIA GPU driver internals from ioctl submission through command buffer construction to hardware execution, including BAR mapping, unified memory management, and the Resource Manager architecture.
- Explain the complete architecture of virtio-nvgpu, including its two-queue design, shared memory window, ioctl forwarding mechanism, memory management strategy, and the trade-offs that enable near-native performance without full hardware isolation.
- Measure, analyze and optimize GPU virtualization performance across workloads, including vCPU pinning strategies, NUMA placement, huge page configuration, interrupt handling and PCIe bus utilization.

- Evaluate security and isolation properties of different GPU virtualization approaches, including IOMMU protection, DMA attack vectors, trusted computing base analysis, and multi-tenant threat modeling.
- Deploy production GPU virtualization architectures for AI/ML training clusters, inference serving, graphics workloads, CI/CD pipelines, and multi-tenant cloud environments.
- Diagnose failures systematically using kernel tracing, QEMU debugging facilities, eBPF observability, GPU-specific profiling tools, and structured troubleshooting procedures for common failure modes.
- Compare GPU virtualization approaches based on architectural trade-offs rather than marketing features, making informed decisions based on your specific workload requirements and operational constraints.

How to Read This Book

The book is organized as a progression from foundation to mastery.

Chapters 1 through 4 establish the problem space and the virtualization infrastructure: why GPUs are difficult to virtualize, how KVM/QEMU works as a hypervisor stack, the IOMMU and VFIO isolation mechanisms, and the PCIe passthrough approach that has been the workhorse of GPU virtualization for over a decade.

Chapters 5 through 8 build the knowledge required to understand paravirtualized GPU approaches: mediated devices and their role in GPU sharing, the virtio protocol that makes paravirtualization efficient, VirtIO-GPU as the established virtio graphics device, and NVIDIA GPU hardware and driver architecture that shapes every virtualization decision.

Chapters 9 through 13 focus specifically on virtio-nvgpu: its architecture and design philosophy, host and guest components, end-to-end command submission paths, and the memory management challenges that GPU virtualization must solve.

Chapters 14 through 19 address the practical concerns of production deployment: performance engineering and measurement, security analysis, comparison of competing approaches, deployment architectures for different use cases, observability and debugging, and systematic failure diagnosis.

Chapter 20 looks forward: where the technology is heading, what remains unresolved, and how emerging workloads and hardware features will reshape GPU virtualization in the next decade.

The code examples and configurations throughout are drawn from real upstream implementations and tested deployments. Where complete implementation requires kernel or QEMU modifications that are not yet upstream, the book provides representative compilable examples, pseudocode and clear explanation of how the pieces integrate with existing architecture. Nothing here is fictional: if a capability requires specific kernel versions, QEMU versions or NVIDIA driver versions, those dependencies are stated explicitly.

Conventions and Source References

Throughout this book, you will encounter references to specific source files in the Linux kernel tree, QEMU repository, virtio specification documents, and NVIDIA documentation. These references point to real code in upstream implementations:

- Linux kernel source paths follow the tree at kernel.org and [torvalds/linux](https://github.com/torvalds/linux) on GitHub
- QEMU source paths reference the official [qemu/qemu](https://qemu.org) repository
- virtio specification references point to the OASIS Virtual I/O Device Technical Committee specifications
- NVIDIA references cite the [open-gpu-kernel-modules](https://open-gpu-kernel-modules.github.io) repository where available, or official documentation

All URLs in the references section are formatted as markdown links for easy access. Inline citations use bracketed numbers [n] that correspond to full references at the end of the book.

The book reflects the state of the technology as of late 2026. `virtio-nvgpu` remains experimental and requires patched software. NVIDIA vGPU and MIG are production technologies with well-documented deployment procedures. PCIe passthrough via VFIO is mature and widely deployed. Some technologies discussed, such as Intel GVT-g, are deprecated but remain important for understanding the evolution of GPU virtualization and for maintaining legacy systems.

Where information is version-dependent or environment-specific, it is labeled explicitly. Do not assume that a configuration that works on one kernel version, QEMU version, or NVIDIA driver version will work unchanged on another: GPU virtualization is a rapidly evolving space, and always verify against the versions you are running.

Now let us begin with the fundamental problem that all GPU virtualization must solve.

Chapter 1: The GPU Virtualization Problem

Why GPUs Are Hard to Virtualize

Modern GPUs are not simple coprocessors that you can command and forget. They are complex, partially non-reentrant systems with their own memory management units, firmware-loaded processors, power management controllers, and tightly timed hardware state machines. They were designed for performance, not for sharing, and they were designed with the assumption that a single operating system and a single driver have exclusive access.

That is a problem for virtualization.

Virtualization works best when resources can be cleanly partitioned and independently scheduled. A CPU can be time-sliced: a hypervisor lets guest A run for ten milliseconds, then guest B, and the hardware state transitions happen at well-defined points. Memory can be mapped and remapped using page tables, with the hypervisor controlling the translation structures. A network card can process packets independently for each virtual function, with its own queues and descriptors.

GPUs resist these patterns in several fundamental ways.

Privileged operations and hardware state. A GPU contains hardware registers and state that only the driver should access, operations that are not designed to be reentrant, and initialization sequences that assume exclusive ownership. When you try to run two guest drivers against one GPU, you must either serialize their access to this state or ensure that their operations do not interfere. Many GPU operations touch global hardware state that cannot be simply partitioned.

The NVIDIA Linux driver, for example, programs the GPU through memory-mapped I/O in BAR0 and interacts with on-chip firmware processors for power management and thermal control. The driver initialization sequence is elaborate: it probes the card, reads hardware IDs, loads firmware blobs,

programs clock controllers, enables power domains, and initializes the GPU System Processor that handles housekeeping. None of this was designed to be called twice simultaneously by two independent instances that think they own the card.

Huge memory and tight coupling. Modern GPUs have tens of gigabytes of dedicated memory, and they access it through hardware address translation units that expect a single, contiguous virtual address space managed by a single driver. When a GPU performs DMA to read textures, write render targets, or transfer compute buffers, it uses physical addresses or GPU-managed virtual addresses that the driver has set up. In a virtualized environment, you must ensure that the GPU never accesses memory belonging to another tenant, and that DMA operations go through proper translation that the hypervisor can control.

The BAR1 aperture on NVIDIA GPUs provides a CPU-visible window into GPU memory space. With Resizable BAR enabled, this window can span the entire VRAM capacity of the card. In a passthrough scenario, the guest can map this region directly. In a shared scenario, you must ensure that each guest sees only its allocated portion and that GPU DMA operations respect those boundaries. The IOMMU provides the hardware mechanism for this protection, but the driver must participate: it must not program DMA addresses that fall outside allowed ranges.

Non-reentrant firmware. GPUs contain embedded processors that run firmware for tasks such as power management, thermal monitoring, clock control, and video decoding. NVIDIA calls this component the GPU System Processor (GSP). AMD calls its equivalent the System Management Controller (SMC). This firmware runs on the card itself and communicates with the host driver through command rings and memory-mapped registers.

The firmware is not designed to serve multiple independent clients. When a guest driver sends a command to the GSP to change power state or query temperature, the firmware executes it with the expectation that the caller is the legitimate, sole owner of the card. You cannot simply multiplex firmware commands from multiple guests without risking state corruption or security issues.

Tight timing requirements. Real-time graphics rendering has strict latency budgets. A display running at 60 Hz has approximately 16.7 milliseconds per frame. Within that window, the GPU must complete all rendering, present

the frame buffer to the display controller, and be ready for the next frame. Any latency introduced by virtualization (a context switch, a memory copy, a serialized command) shows up directly as dropped frames or stutter.

Compute workloads are less sensitive to absolute latency but extremely sensitive to throughput. A deep learning training job running on a cluster of GPUs measures efficiency in terms of floating-point operations per second, and any overhead that reduces GPU utilization translates directly into increased cost and longer training times.

These constraints make GPUs fundamentally different from other virtualized resources.

Goals of GPU Virtualization

Given these challenges, what are we actually trying to achieve? Different workloads impose different requirements, and understanding these requirements is essential for choosing the right approach.

Full graphics with display output. The original driver for GPU virtualization was desktop virtualization: giving each user in a VDI environment access to a GPU-accelerated desktop with hardware-accelerated rendering, video playback, and display output. Requirements here include real-time rendering with acceptable latency, support for multiple displays at various resolutions, video decoding acceleration and cursor handling. Performance does not need to match bare metal perfectly but must be good enough for interactive use.

3D graphics and gaming. Games and CAD applications push GPUs to their limits with complex rendering pipelines, high frame rates, and large texture sets. Here performance matters critically: users will notice even small degradations, and the graphics APIs (DirectX, Vulkan, OpenGL) expect specific hardware behavior. Hypervisor detection must be avoided because some games refuse to run in virtualized environments or reduce quality when virtualization is detected.

CUDA and general-purpose GPU compute. Scientific computing, data processing, and financial modeling use GPUs as massively parallel processors through CUDA, OpenCL, or SYCL. Requirements include full API support, correct numerical results, acceptable performance and GPU memory access from the guest. Latency sensitivity varies: batch jobs care about throughput, interactive tools care about responsiveness.

AI and machine learning. This is where GPU demand has exploded. Training large models requires massive GPU clusters with high-bandwidth interconnects. Inference serving requires many GPUs to process requests with low latency. Requirements include full CUDA support, GPU memory capacity, GPU-to-GPU communication (NVLink, NVSwitch), and the ability to scale to hundreds or thousands of GPUs. Cost efficiency drives the demand for GPU sharing: GPUs are expensive, and utilization in training clusters can vary dramatically.

Video processing and encoding. Content creation and streaming platforms use GPUs for video encoding (NVENC, NVDEC on NVIDIA) and image processing. Requirements include hardware encoder/decoder access, low-latency processing for real-time streaming, and support for various formats and resolutions.

Multi-tenant resource pooling. Across all these workloads, a common operational goal is multi-tenancy: allowing many independent users or organizations to share GPU resources on the same physical hardware. This is the key driver for GPU virtualization in cloud environments and shared data centers. Without it, each tenant needs a dedicated GPU, which leads to poor utilization and high cost.

These goals are sometimes in tension. A gaming VM needs exclusive GPU access and hypervisor invisibility. An AI training cluster needs maximum throughput and multi-GPU scaling. A VDI environment needs many lightweight virtual GPUs sharing one physical card with good isolation. No single virtualization approach satisfies all goals equally well.

The Evolution Timeline

GPU virtualization has evolved over more than fifteen years as both hardware capabilities and software techniques have advanced. Understanding this evolution helps explain why current solutions look the way they do and what problems remain unsolved.

Early attempts (2008-2012). The first serious GPU virtualization efforts targeted Xen and focused on graphics passthrough. The approach was simple: let one VM own the GPU completely. This worked but provided no sharing and required the guest to run the native driver, which complicated management. Some early work explored trap-and-emulate approaches where privileged

GPU operations were intercepted by the hypervisor and emulated, but these suffered from terrible performance due to the granularity of GPU operations.

SR-IOV emerges (2012-2015). PCIe SR-IOV (Single Root I/O Virtualization) arrived as a standardized way for PCIe devices to expose multiple virtual functions that could be assigned independently to VMs. SR-IOV worked excellently for network adapters: a single NIC could expose dozens of virtual functions, each with dedicated hardware queues and DMA rings. But GPU vendors were slow to adopt SR-IOV for graphics, largely because the hardware requirements were more demanding and the market for GPU sharing was smaller at the time.

Intel XenGT/GVT-g (2011-2018). Intel began developing GPU virtualization for its integrated graphics starting around 2011. The project went through several phases: early XenGT proof of concepts, then the KVMGT implementation for KVM, and finally the production-ready Intel GVT-g solution starting with Broadwell (5th generation Core processors).

GVT-g used a mediated pass-through model that became influential for later designs. The physical GPU was partitioned into virtual GPUs, each with allocated graphics memory and hardware contexts. The host driver maintained a device model for each guest VM, mediating access to privileged resources while allowing performance-critical paths to go directly to the hardware. Guests ran a lightly modified version of the native i915 driver that was made virtio-aware. Performance was good enough for desktop use, and up to seven virtual GPUs could share one physical iGPU.

GVT-g was eventually deprecated in favor of Intel's SR-IOV implementation for Xe architecture GPUs, but its mediated-device architecture influenced subsequent designs.

NVIDIA GRID and vGPU (2013-present). NVIDIA entered the virtualization market seriously in 2013 with the GRID K1 product and its vGPU software stack. The solution was designed for datacenter GPUs (Tesla, Quadro, later A-series) and provided time-sliced sharing across multiple VMs with hardware-accelerated rendering, video encoding, and CUDA compute.

The architecture used proprietary firmware and drivers. The host ran a special NVIDIA vGPU driver that partitioned the GPU into virtual instances (vGPUs), each with guaranteed resources such as memory, encoder slots, and compute time. Guests ran NVIDIA vGPU guest drivers that presented the virtualized GPU as a regular NVIDIA card. Licensing was required and expensive.

NVIDIA extended vGPU to support mediated devices (mdev) in the Linux kernel starting around 2016, integrating with the kernel's standard device virtualization framework. With the introduction of Multi-Instance GPU (MIG) on the A100 (2020), NVIDIA added hardware-level spatial partitioning for datacenter GPUs, providing true isolation between instances with dedicated compute units, memory slices and caches.

AMD MxGPU and SR-IOV (2016-present). AMD introduced MxGPU for its professional GPUs (FirePro, later Radeon Pro) with mediated device support for Linux. The approach was similar to NVIDIA vGPU but focused on datacenter and professional workloads. More recently, AMD has emphasized PCIe SR-IOV for GPU virtualization, particularly for its Instinct accelerators used in AI workloads.

VirtIO-GPU and virglrenderer (2013-present). On the open-source side, the virtio-gpu device was added to the virtio specification and implemented in QEMU and the Linux kernel around 2013. It provided a paravirtualized graphics adapter using the standard virtio protocol, supporting 2D graphics with display output. The virglrenderer project added 3D acceleration by translating Gallium state from the guest into OpenGL commands executed on the host GPU.

VirtIO-GPU was suitable for desktop use and basic 3D acceleration but not for performance-critical workloads or compute. Command serialization overhead limited performance, and the graphics API translation model did not work well for CUDA or other compute APIs.

DRM native context and Venus (2023-2026). The virtio-gpu project evolved with new extensions. The DRM native context capability allowed the guest to run a modified version of the native GPU driver directly, with virtio handling only control and resource management. The Venus protocol provided Vulkan command serialization for virtio-gpu. These approaches improved performance for graphics workloads but were not designed for NVIDIA GPUs specifically and did not address compute workloads directly.

virtio-nvgpu (2026). Nester Labs introduced virtio-nvgpu in September 2026 with a fundamentally different approach: instead of translating graphics APIs, it forwards the NVIDIA kernel driver ABI. The guest runs the real NVIDIA user-mode libraries unmodified, building GPU command buffers locally, and only ioctl calls cross the virtualization boundary through virtio queues. The shared memory window maps GPU buffers directly into guest address space without copying. Performance is within two percent of bare metal for typical

rendering workloads, and multiple guests can share one GPU.

The approach is experimental and has trade-offs, most notably weaker security isolation than VFIO passthrough. But it demonstrates that near-native performance GPU sharing is achievable with open software on commodity hardware.

Taxonomy of GPU Virtualization Approaches

Before diving into the technical details of each approach, it is useful to have a vocabulary for discussing them. GPU virtualization techniques can be classified along several dimensions.

By level of hardware access:

- *Full passthrough*: The physical GPU is assigned directly to a single guest VM via VFIO and IOMMU. The guest sees and accesses the GPU as if it were bare metal. Performance is near-native, but the GPU cannot be shared.
- *Mediated devices*: A single physical GPU is partitioned into multiple virtual devices that can be assigned to different guests. Each virtual device appears as an independent GPU but shares the underlying hardware. Isolation and scheduling are managed by the host driver and firmware.
- *Paravirtualized devices*: A virtual GPU device is presented to the guest using a known protocol (such as virtio). The guest driver is aware of virtualization and communicates with the host through well-defined interfaces. Performance depends on the protocol efficiency.
- *Software rendering*: Graphics operations are emulated in software on the host CPU with no GPU acceleration. Performance is very poor but compatibility is maximum and no special hardware is needed.

By API translation level:

- *Driver-level forwarding*: The guest kernel driver's ioctl calls or command buffers are forwarded to the host driver with minimal translation. This preserves the guest driver's native command generation and achieves near-native performance. Examples: VFIO passthrough, virtio-nvgpu.

- *API-level translation*: Graphics API calls (OpenGL, Vulkan, DirectX) from the guest are serialized and translated to equivalent calls executed by the host graphics stack. Performance is limited by serialization overhead and translation complexity. Examples: virtio-gpu with virglrenderer, Venus protocol.
- *Command buffer translation*: GPU command buffers generated by the guest are modified and replayed on the host GPU. This requires understanding the GPU's command language and can achieve better performance than API translation but is GPU-specific.

By memory model:

- *Direct DMA*: The guest can program GPU DMA operations that access guest memory directly through IOMMU translation. This is used in passthrough and some mediated device approaches.
- *Buffer sharing*: GPU buffers are mapped into both guest and host address space through shared memory mechanisms (such as DRM render nodes or virtio shared memory windows). This avoids copying but requires coordination between guest and host.
- *Copy-based*: Guest memory is copied to host memory before GPU operations and results are copied back. Simplest to implement but adds significant latency and bandwidth consumption.

Each approach makes different trade-offs among performance, isolation, flexibility and implementation complexity. No single approach is universally optimal. The rest of this book examines each approach in technical detail, with particular attention to how modern implementations solve the core problems and where their limitations lie.

The chapter ends here with the problem space defined. The next chapter examines the hypervisor stack that makes all of this possible: KVM and QEMU.

Chapter 2: KVM and QEMU: The Modern Linux Hypervisor Stack

The Two-Part Architecture

KVM (Kernel-based Virtual Machine) and QEMU (Quick Emulator) together form the standard virtualization stack on Linux. Despite their close integration, they are distinct components with separate responsibilities, and understanding this separation is fundamental to understanding how GPU virtualization fits into the architecture.

KVM is a kernel module that turns the Linux kernel into a hypervisor. It provides hardware-accelerated virtualization using Intel VT-x or AMD-V, manages virtual CPU execution, handles memory virtualization through EPT/NPT, and exposes an ioctl-based interface to user space. KVM knows nothing about emulated devices, disk images, or networking: it knows about virtual machines as collections of virtual CPUs with memory regions and device address spaces.

QEMU is a user-space process that emulates the rest of the computer: the CPU (when not accelerated by KVM), the chipset, PCIe buses, memory controllers, network adapters, storage controllers, display devices, and everything else a guest operating system expects to find. When QEMU is configured with the KVM accelerator, it delegates CPU execution and memory management to KVM while retaining control of device emulation and I/O.

This separation has implications for GPU virtualization. Some approaches require only QEMU changes (adding a virtio-gpu device model). Some require only kernel changes (adding a virtio backend or modifying the vfio-pci driver). Some require both (VFIO passthrough needs kernel IOMMU support and QEMU device model integration). And some require host drivers beyond the kernel and QEMU (NVIDIA vGPU needs the proprietary vGPU driver installed on the host).

KVM Architecture

KVM is implemented as a set of kernel modules that register with the Linux kernel's core subsystems. The primary modules are:

- **kvm.ko**: The core KVM module that provides architecture-independent functionality. It implements the userspace interface through the `/dev/kvm` character device, manages VM and vCPU lifecycle, and handles memory region registration.
- **kvm_intel.ko** or **kvm_amd.ko**: The architecture-specific module that interfaces with hardware virtualization extensions. This module sets up VMX root mode (Intel) or SVM mode (AMD), manages the VMCS (Virtual Machine Control Structure) or VMCB (Virtual Machine Control Block) for each vCPU, and handles hardware-specific virtualization features.
- **kvm_vmware.ko** or similar: Modules for nested virtualization support, allowing a KVM guest to run its own virtual machines using virtualized virtualization extensions.

When KVM initializes, it creates a character device at `/dev/kvm` that user-space programs (primarily QEMU) use to control virtualization. The interface is entirely ioctl-based, with a stable API versioned through `KVM_GET_API_VERSION`. The API is deliberately low-level: KVM exposes primitives for creating VMs, creating vCPUs, mapping memory and running vCPUs. Higher-level concepts like devices, buses and guest operating systems are left to user space.

The VMCS and Hardware Virtualization

At the hardware level, Intel VT-x defines two operating modes: VMX root mode and VMX non-root mode. In VMX root mode, the hypervisor (KVM) runs with full privilege and controls virtualization. In VMX non-root mode, the guest OS runs, but the hardware intercepts specific events and transitions back to root mode for the hypervisor to handle.

Each virtual CPU has a VMCS (Virtual Machine Control Structure), a large data structure that contains:

- Control fields defining which instructions and events cause VM exits (CPUID, I/O port access, MSR access, interrupts, EPT violations, etc.)

- Guest state fields that are restored when entering the guest (general-purpose registers, RIP, RSP, RFLAGS, CR0-4, segment registers)
- Host state fields that are saved when exiting the guest (the host's RIP, RSP, CR3, etc.)
- Execution control fields for features like APIC virtualization, pause loop exiting, and secondary execution controls

When KVM wants to run a vCPU, it loads the VMCS and executes the VMX instruction (VMLAUNCH or VMRESUME). The CPU switches to non-root mode and begins executing guest instructions. When a configured event occurs (the guest executes CPUID, accesses a device MMIO address, violates EPT permissions, or receives an interrupt), the hardware performs a VM exit: it saves the guest state, restores the host state, and transfers control to a VM exit handler specified by KVM.

The VM exit handler in KVM processes the event. If the guest executed CPUID, KVM returns filtered CPUID information to prevent the guest from detecting the underlying hardware or hypervisor. If the guest accessed an MMIO region mapped to an emulated device, KVM injects an exit reason into the `kvm_run` structure and pauses the vCPU, allowing QEMU to handle the emulated I/O. If the guest triggered an EPT violation by accessing unmapped memory, KVM may install the missing page table entry or forward the fault to QEMU.

After handling the event, KVM reloads the VMCS (if necessary) and resumes guest execution with VMRESUME. This cycle (run guest, exit, handle, resume) is the fundamental loop of hardware-assisted virtualization.

Memory Virtualization: EPT and NPT

Virtualizing memory efficiently is critical for GPU workloads, which perform massive amounts of DMA and require predictable memory access patterns. KVM uses hardware-assisted two-dimensional paging rather than the older shadow page table approach.

On Intel, this is Extended Page Tables (EPT). On AMD, it is Nested Page Tables (NPT). Both mechanisms work the same way conceptually: the CPU maintains two levels of translation.

The first level is the guest's own page tables (pointed to by CR3 or RFLAGS.LM mode page table roots). These translate guest virtual addresses

to guest physical addresses, exactly as they would on bare metal. The second level is the EPT/NPT tables, maintained by KVM, which translate guest physical addresses to host physical addresses.

When the guest accesses memory, the CPU performs both translations in hardware: guest virtual -> guest physical -> host physical. This happens transparently and efficiently, without hypervisor intervention, as long as the translations are cached in the TLB.

EPT violations occur when:

- The guest accesses a guest physical address that is not mapped in the EPT (no corresponding host physical page)
- The guest violates permissions (writes to a read-only page, accesses a page with wrong execute permission)
- The guest accesses a page mapped for monitoring (write-protected for dirty page tracking during migration)

KVM handles EPT violations through a page fault handler that walks the EPT page tables and installs or updates entries as needed. For GPU DMA, this mechanism ensures that the GPU's DMA operations are subject to the same translation and protection as CPU accesses: the IOMMU provides an additional level of translation for DMA, which KVM configures through the VFIO interface.

The `kvm_run` Structure and User-Space Interface

Communication between KVM (kernel) and QEMU (user space) happens through a shared memory structure called `kvm_run`, which is mapped into both kernel space and user space. When a VM exit requires user-space handling, KVM writes information about the exit into `kvm_run` and returns control to the user-space caller. The caller (QEMU) processes the exit, updates the `kvm_run` structure with any response, and calls `KVM_RUN` again to resume.

The `kvm_run` structure contains:

- `exit_reason`: an enum indicating why the VM exited (`KVM_EXIT_IO`, `KVM_EXIT_MMIO`, `KVM_EXIT_IRQ_WINDOW_OPEN`, `KVM_EXIT_SHUTDOWN`, `KVM_EXIT_FAIL_ENTRY`, etc.)

- Architecture-specific fields for different exit reasons (IO port data, MMIO address and data, interrupt information)
- Registers state that can be read and written (RAX, RCX, RDX, RBX, RSP, RBP, RSI, RDI, RIP, RFLAGS on x86)
- Synchronization fields for vCPU requests and interrupts

For GPU virtualization, several exit reasons are relevant:

- `KVM_EXIT_IO`: The guest executed an IN or OUT instruction to access an I/O port (legacy ISA device access)
- `KVM_EXIT_MMIO`: The guest accessed a memory-mapped I/O region that is not backed by RAM (typically a device register)
- `KVM_EXIT_INTR`: An external interrupt was delivered to the vCPU

PCI devices, including GPUs, typically use memory-mapped I/O rather than I/O ports, so `KVM_EXIT_MMIO` is the primary mechanism through which device emulation happens. When a guest accesses a device's BAR space or config space, KVM triggers a VM exit with the exit reason and MMIO details, QEMU processes the access through the device model, and KVM resumes execution.

QEMU Architecture

QEMU is a user-space process that implements device emulation using a combination of techniques. When run with the KVM accelerator, its responsibilities are reduced but remain significant:

- **System initialization**: Building the emulated hardware topology (chipset, buses, devices), loading firmware, initializing memory regions
- **Device emulation**: Implementing the behavior of every device visible to the guest (PCI configuration space, device registers, DMA engines, interrupt controllers)
- **Virtio backend**: Processing virtio queue operations, handling virtio device configuration and feature negotiation
- **VFIO integration**: Setting up PCIe passthrough devices, mapping DMA regions through IOMMU, handling device interrupts

- **I/O and networking:** Emulating network devices (virtio-net, e1000), storage devices (virtio-blk, virtio-scsi), USB controllers, and other I/O peripherals

QEMU's device model architecture is object-oriented, using QOM (QEMU Object Model), an introspection and inheritance framework. Each device type is a QOM type that inherits from base device types (DEVICE, PCI_DEVICE, VIRTIO_DEVICE, etc.). Device instances have properties that can be configured, lifecycle callbacks (realize, unrealize, reset), and methods that implement device behavior.

PCIe Bus Emulation

For GPU virtualization, the PCIe bus emulation is particularly important. QEMU emulates a complete PCIe topology with root ports, bridges and device slots. Each device has:

- PCI configuration space (256 bytes base, plus extended config space) containing device IDs, capabilities, BARs and interrupt routing information
- BARs (Base Address Registers) that define memory or I/O port windows mapped into the guest's address space
- MSI/MSI-X interrupt vectors for message-signaled interrupts
- Capability structures describing optional features (PCIe capabilities, SR-IOV capabilities, ACS, etc.)

When the guest reads or writes PCI configuration space, QEMU intercepts the access through the PCI config space read/write handlers and returns or updates the appropriate field. When the guest accesses a BAR region, the access is routed to the device model's memory region callbacks. When the device raises an MSI interrupt, QEMU injects it into the guest through KVM's interrupt injection API.

For virtio devices, QEMU uses a specialized PCI device model (VirtIOPCIProxy) that implements the virtio PCI transport protocol: capability structures for virtio, config space for virtio-specific configuration, BARs for virtqueue ring buffers, and MSI-X vectors for queue notifications.

QEMU and KVM Integration

The integration between QEMU and KVM is mediated through the KVM accelerator and the `/dev/kvm` interface. When QEMU starts with `-accel kvm` or `-enable-kvm`, it:

1. Opens `/dev/kvm` and checks the API version with `KVM_GET_API_VERSION`
2. Creates a virtual machine with `KVM_CREATE_VM`, which returns a file descriptor for the VM
3. Sets up the VM's memory regions with `KVM_SET_USER_MEMORY_REGION`, mapping guest physical address ranges to QEMU's anonymous memory allocations
4. Creates vCPUs with `KVM_CREATE_VCPU`, which returns a file descriptor for each vCPU
5. For each vCPU, maps a `kvm_run` structure shared with the kernel
6. Enters the main loop: for each vCPU thread, calls `KVM_RUN` in a loop, handling exits when KVM returns

The memory region setup is where GPU virtualization becomes interesting. For virtio devices, the virtqueue ring buffers are placed in guest RAM and mapped through `KVM_SET_USER_MEMORY_REGION`. QEMU can access these buffers directly in its address space because they are backed by mmap'd anonymous memory that is shared between KVM (for guest physical addressing) and QEMU (for device model access).

For VFIO passthrough, the memory region setup is more complex. The physical GPU's BARs are mapped into the guest's address space, and DMA from the GPU goes through the IOMMU. KVM and VFIO coordinate through the `vfio_iommu_type1` interface to set up the appropriate translation entries so that GPU DMA accesses to guest RAM are translated correctly through the IOMMU to host physical addresses.

Async I/O and NUMA Awareness

Modern QEMU uses asynchronous I/O extensively to avoid blocking vCPU threads. For storage and network I/O, event loops with `epoll` handle completions on separate threads. For virtio devices, `ioeventfds` allow devices to

wake up a dedicated I/O thread instead of triggering a VM exit for every I/O operation.

NUMA awareness is critical for GPU workloads. QEMU can be configured to allocate VM memory on specific NUMA nodes using `-numa` options and memory backends. vCPUs can be pinned to specific physical cores using `-smp` with CPU topology and the `cpuset` options in libvirt XML. For GPUs, placing the VM on the same NUMA node as the GPU minimizes cross-node memory access and PCIe traversal latency.

For `virtio-nvgpu` specifically, NUMA placement matters because the `virtio` device's `virtqueue` processing runs in QEMU (or in a separate `vhost` process), and the NVIDIA driver runs in the host kernel. If the vCPU running GPU-intensive work, the QEMU thread processing `virtio` queues, and the GPU itself are all on different NUMA nodes, the resulting cross-node traffic adds measurable overhead.

The KVM IOCTL Interface in Detail

Understanding the KVM API is essential for understanding how GPU virtualization interacts with the hypervisor. The primary `ioctl`s are:

KVM_CREATE_VM: Creates a new virtual machine and returns a file descriptor. The VM starts with no vCPUs and no memory regions.

KVM_CREATE_VCPU: Creates a new virtual CPU for the VM, returning a vCPU file descriptor. Each vCPU runs in its own thread in user space, with its own `kvm_run` structure.

KVM_RUN: The main `ioctl` that runs a vCPU. It blocks until a VM exit occurs, then returns with the exit reason written in `kvm_run`. User space handles the exit and calls `KVM_RUN` again.

KVM_SET_USER_MEMORY_REGION: Maps a guest physical address range to user-space memory. Used for RAM, ROM and device MMIO regions. For GPU virtualization, this is how guest framebuffers and `virtio` shared memory regions are set up.

KVM_SET_CPUID2: Sets the CPUID information that the guest sees. Used to filter features and hide hypervisor presence. For NVIDIA Code 43 avoidance in passthrough scenarios, modifying CPUID output to hide the hypervisor is sometimes necessary.

KVM_IRQ_LINE and **KVM_IRQFD**: Control interrupt lines. **KVM_IRQ_LINE** injects a level-triggered interrupt. **KVM_IRQFD** associates an eventfd with an interrupt line, so that when the eventfd becomes signaled, the interrupt is automatically injected. Used for virtio ioeventfds and VFIO interrupt remapping.

KVM_CREATE_DEVICE: Creates a virtual device that is managed by the kernel rather than user space. Used for kernel-managed devices such as the in-kernel APIC, pit timer, and vhost devices.

For GPU passthrough via VFIO, an additional ioctl, **KVM_ASSIGN_DEVICE** (deprecated, replaced by VFIO's own interface), was historically used to assign physical PCI devices to a VM. Modern implementations use VFIO's container and group mechanism directly, with QEMU setting up the appropriate mappings and KVM handling interrupt injection through **KVM_IRQFD**.

Guest Execution Lifecycle

To understand where GPU virtualization fits into the overall picture, consider the complete lifecycle of a guest boot with GPU access:

1. **QEMU starts** with its command line or XML configuration, which includes CPU topology, memory size, disk images, network configuration, and GPU device specification.
2. **QEMU initializes KVM** by opening `/dev/kvm` and creating the VM and vCPUs.
3. **QEMU sets up memory regions** using **KVM_SET_USER_MEMORY_REGION**. This includes guest RAM, firmware images, and any MMIO regions needed by emulated devices.
4. **GPU device is configured**. For passthrough, QEMU binds the physical GPU to the VM through VFIO, sets up DMA mappings through the IOMMU, and creates an emulated PCIe device that represents the passed-through GPU. For virtio-gpu, QEMU creates a virtio-gpu PCI device model, allocates virtqueue ring buffers, and sets up shared memory regions for framebuffers and resources.
5. **QEMU launches the firmware** (SeaBIOS for legacy, OVMF for UEFI) which begins executing as a guest CPU.
6. **The guest firmware enumerates hardware**, including PCI devices. It discovers the GPU device, reads its config space, maps its BARs, and loads any required VBIOS.

7. **The guest OS boots**, loads its device drivers, and initializes the GPU. For passthrough, the guest NVIDIA driver talks directly to the physical GPU through BARs and DMA, mediated only by the IOMMU. For virtio-gpu, the guest virtio_gpu DRM driver sets up virtqueues and communicates with QEMU through the virtio protocol.
8. **GPU workloads execute** in the guest. Commands and DMA operations flow through whatever path the chosen virtualization approach provides: direct PCIe for passthrough, mediated device firmware for vGPU, virtio queues for virtio-gpu, or ioctl forwarding for virtio-nvgpu.
9. **Completion events and interrupts** return from the GPU path through whatever mechanism is appropriate: direct MSI/MSI-X for passthrough (remapped through IOMMU interrupt translation), host-generated events forwarded through mediated device interfaces, or virtio used ring updates for virtio devices.
10. **Shutdown** reverses the process. For passthrough, the GPU is reset (FLR, bus reset, or hot reset), VFIO mappings are torn down, and the GPU can be re-bound to the host or another guest.

Each step in this lifecycle can fail in characteristic ways, and understanding the normal flow is essential for diagnosing problems when things go wrong. The remaining chapters explore each GPU virtualization approach's specific variations on this lifecycle in detail.

The chapter ends with the hypervisor foundation laid. The next chapter examines the isolation and device assignment infrastructure (IOMMU and VFIO) that makes GPU access to virtual machines possible and safe.

Chapter 3: IOMMU, VFIO and Device Assignment Foundations

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Issue: IOMMU Group Contains Unwanted Devices

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Issue: GPU Reset Fails or Hangs

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Issue: High CPU Usage or Performance Degradation

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Issue: NVIDIA Driver Installation Fails Inside Guest

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Issue: VM Crashes on GPU Access

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Chapter 20: The Future of GPU Virtualization

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