STARC RECOMMENDS POWERPRO’S CLOCK GATING FOR RTL POWER OPTIMIZATION
ABSTRACT

“PowerPro’s ability to read in an RTL design and generate a substantially lower-power, functionally equivalent RTL is very impressive. We found that Calypto’s unique Sequential Analysis approach to automating RTL power optimization identified many additional clock-gating opportunities and saved design time.”
-Nobuyuki Nishiguchi, Vice President, General Manager Development Department

BACKGROUND

The Semiconductor Technology Academic Research Center (STARC) is an engineering consortium co-founded by major Japanese semiconductor companies in December 1995. STARC’s mission is to contribute to the growth of the Japanese semiconductor industry by developing leading-edge SoC design technologies (http://www.starc.jp/).

To aid its member companies in the design and development of LSI circuits, STARC develops and publishes reference flows. One of these, the RTL-to-layout STARCAD-CEL digital design flow, addresses the challenges of advanced process technologies below 65nm. Because power optimization is a central part of this flow, STARC is looking for new and effective ways to automate power optimization.

Calypto Systems’ PowerPro® CG and SLEC ® Pro were evaluated and incorporated into version 2.0 of the STARCAD-CEL design flow. This case study discusses the evaluation criteria, process and results that led to the certification of PowerPro by STARC for its member companies.

CHALLENGE

Power consumption has become a leading concern for STARC’s member companies since many of them are creating SoC’s for consumer devices that demand increased functionality, smaller form factors, and extended battery life.

Today, designers perform manual clock gating to reduce power. But this is time-consuming and error-prone. More so, many clock-gating optimizations are sequential in nature and thus cannot be verified by traditional combinational equivalence checking tools. This causes designers to spend additional time developing clock gating tests and running simulations to ensure their changes have not introduced functional errors.

STARC was faced with the challenge of developing a low-power design flow with a solution that:

- Automated the current manual process of optimizing power
- Could be comprehensively verified with little effort
- Easily fit within the existing RTL design flow
- Did not adversely affect the timing or area of the device

SOLUTION

STARC ensures that all new tools pass a comprehensive and objective evaluation process before being recommended as part of a reference flow for member companies. The PowerPro evaluation consisted of three primary phases outlined below.
TECHNOLOGY VALIDATION

Detailed tests were conducted to confirm that specific PowerPro functionalities worked as advertised; e.g., to make sure clock gating was implemented with optimal logic and that report data matched actual measurements. Four small, controllable test cases were created to determine exactly how the tool operated. Each had a different logic condition in which sequential clock gating could be applied. PowerPro performed correctly on all of these tests. Clock gating logic was optimally inserted, power was reduced, and the reports correctly indicated the enable logic and clock gating efficiency improvements.

The use model was found to be straightforward and easy to learn. PowerPro only requires the synthesizable Verilog RTL files and a few TCL setup commands to define clocks and blackboxes to get started. Once the initial “vector-less” runs were complete, switching activity data in the form of SAIF files was added to the setup. The output of PowerPro was a power optimized RTL design. The power optimized RTL was then formally verified to be equivalent to the original RTL using SLEC Pro by running the verification script created by PowerPro. (See figure 1)

Figure 1: PowerPro Clock Gating Use Model

“Our evaluation demonstrated that PowerPro correctly inserted clock gating enable logic. On all tests we were able to formally prove equivalence between the original RTL and optimized RTL using sequential equivalence checking (SLEC Pro)”

MEASURING PRODUCTIVITY

For the second phase of the evaluation focused on how easy the PowerPro was to use. The evaluation compared implementation time and power savings of PowerPro to existing power optimization flows based on STARC’s manual clock gating rules. Several characteristics of flow were measured including runtime, number of code changes, power savings and fit with other tools such as verification.

The time to implement and test the power optimizations in each flow was measured as the sum of time to generate switching activity files, identify clock gating enable conditions, modifying the RTL, and verify the power optimized RTL. (See Comparison Graph). In the manual B flow two power optimizations were manually implemented which made it easy and fast to modify the RTL code. Verification with simulation was also fast but as expected this flow yielded the lowest power savings. In the manual A flow, 43 power optimizations were made which increased the power savings by 3.4 times over manual B flow. However, as is clear in the graph, this method took much longer to implement and formally verify. In comparison PowerPro’s Clock Gating and SLEC Pro’s formal verification took the least amount of time while at the same time PowerPro saved over 5.8 times more power than manual B flow!
Productivity can be defined as the power saved from a set of optimizations divided by the time it takes to implement and test them. If we compare the productivity of each flow, PowerPro is over 10 times more productive than either manual flow. (See Productivity Comparison Graph).
RUNNING THE NUMBERS

The final phase of the evaluation measured power savings. This included taking both the original RTL and PowerPro optimized RTL designs through synthesis and measuring power at the gate-level. The results were calculated on a multimedia signal processing design: an Ogg Vorbis audio decoder. The design was 90K gates, not including RAM and ROMs.

Common metrics for measuring power are the clock gate percentage and clock gating efficiency of a RTL design block. While it is simple to compute the number of registers that have been clock gated in a design, this metric has poor correlation to actual switching activity and power savings. Clock-Gating Efficiency measures the percentage of time a register is gated (turned off) for a given set of activity vectors. Since Clock-Gating Efficiency takes into account switching activity, it is a much better indicator of clock gating effectiveness and dynamic power savings.

The Ogg Vorbis audio decoder design had previously been power optimized which included manually adding clock gate enable logic to the RTL. Consequently the original RTL design had 79 percent of its registers clock gated and clock gating efficiency of 68 percent. The following table summarizes the characteristics of the original and PowerPro optimized RTL designs:

<table>
<thead>
<tr>
<th></th>
<th>Original Design</th>
<th>PowerPro Optimized RTL</th>
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</thead>
<tbody>
<tr>
<td>Timing</td>
<td>Met</td>
<td>Met</td>
</tr>
<tr>
<td>Formal Verification (SLEC Pro)</td>
<td>Verified Equivalent</td>
<td>Verified</td>
</tr>
<tr>
<td>Gate-level simulation</td>
<td>Verified</td>
<td>Verified</td>
</tr>
<tr>
<td>% registers clock gated</td>
<td>79%</td>
<td>88%</td>
</tr>
<tr>
<td>% clock gating efficiency</td>
<td>68.8%</td>
<td>75.8%</td>
</tr>
<tr>
<td>Clock &amp; Register power*</td>
<td>2.28 mW</td>
<td>1.83 mW</td>
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*measured at gate-level switching activity

Power was measured on the gate-level netlist generated from synthesizing of the PowerPro optimized RTL. The result was that PowerPro reduced clock and register power by 19.7 percent compared to the original design.

PowerPro added 11 clock gating optimizations to the original RTL, increasing the number of registers gated from 79 to 88 percent. The evaluation showed that PowerPro automatic sequential clock gating was able to improve clock gating on a design that had already been manually clock gated.
STARC Recommends PowerPro's Clock Gating For RTL Power Optimization

**BENEFITS**

“PowerPro was able to save power on a RTL that had been designed for low power. In the future PowerPro can be used earlier in the design flow to reduce design efforts and save more power.”

STARC recommends using PowerPro to optimize power. The favorable results from this thorough evaluation show that PowerPro correctly and effectively identifies clock gating enable logic that reduces power. PowerPro increases productivity by inserting clock gating enable logic into the original RTL code such that the resulting optimized RTL is compatible and complementary to existing RTL design flows. PowerPro can be used on larger blocks, earlier in the design process to provide greater power savings and eliminate the effort spent on manual clock gating optimizations.