Comprehensive Place-and-Route Platform
Olympus-SoC

Olympus-SoC is a comprehensive netlist-to-GDSII physical design implementation platform.

Solving Advanced Design Challenges
The Olympus-SoC™ Netlist-to-GDSII system comprehensively addresses the performance, capacity, time-to-market, power, and variability challenges. Olympus-SoC is a complete physical design implementation tool with best-in-class physical implementation engines including design planning, placement, physical synthesis, clock tree synthesis, routing, power optimization, manufacturability and a native sign-off quality timer with patented virtual timing graph technology.

Olympus-SoC provides the highest capacity in the industry with a very compact and scalable database to handle designs that contain hundreds of millions of instances. The low power suite enables both leakage and dynamic power reduction throughout the flow and power-aware clock tree synthesis.

Olympus-SoC also offers multi-threaded and distributed analysis and optimization throughout the flow to significantly reduce design cycle time. Native integration with Calibre minimizes physical verification ECOs and enables signoff checks during implementation.

Flexible Routing Architecture
Olympus-SoC features a scalable and flexible routing architecture that integrates the global, track, and detailed routing engines best suited to handle complex DRC and DFM requirements for all the technology nodes of the leading foundries. The Olympus-SoC router is able to address the increased number and complexity of DRC rules with fast runtimes and no loss in accuracy by performing a comprehensive and detailed analysis of the design rules and

BENEFITS:
- Optimal performance, power and area with true and concurrent optimization throughout the flow
- Flexible architecture to support complex mult-VDD design styles including MTCMOS and DVFS
- Compact and scalable database provides highest capacity in the industry to effectively handle growing design sizes
- Minimizes design planning iterations with data flow graph driven Automatic Macro Placement
- Speed time-to-market with fewer design iterations and a suite of scalable parallelization technologies
- Best area and highest utilization with proprietary area recovery technologies throughout the flow
- Highest performance with patented multi-corner, multi-mode (MCMN) analysis and optimization architecture
- Integrated Calibre signoff to achieve manufacturing closure during physical design implementation

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minimizing the number of operations that the router has to perform to ensure fast runtime without loss in accuracy. The unified Global Router based congestion modeling ensures excellent correlation in all stages of the design flow. The routing engine incorporates signoff-quality, variation-aware timing and optimization engine for SI- and timing-driven routing.

The router is highly flexible, with support for both gridded and non-gridded models and the use of a universal connectivity model for a friendly ECO flow. It also supports sophisticated non-default rules (NDRs) and all the DFM requirements for advanced nodes including recommended rules, pattern matching, redundant vias, wire spreading/widening, and timing-aware smart metal and via fill.

**Signoff Physical Verification**

Olympus-SoC uses an “open router” architecture that allows it to natively invoke all the signoff Calibre engines during implementation through the Calibre InRoute advanced design and manufacturing closure platform. Invoking Calibre facilities directly within the Olympus-SoC environment provides automated, intelligent prevention of DRC/DFM/MP issues, true signoff analysis, and automatic fixing of DRC/DFM/MP violations during the physical design process.

Calibre InRoute ensures that all manufacturability issues are addressed without introducing new ones, and without degrading the performance of the design. The open router architecture also eliminates the need for any serial data transfers, as all the engines use the same hosted data model.

**Flexible Design Planning**

To tackle the challenges of growing design sizes, such as runtime and tool capacity, Olympus-SoC provides multiple design planning options including flat, hierarchical and pseudo flat floorplanning technologies. Hierarchical floorplanning supports both channel-based and channel-less (abutted) flows and offers unique technologies such as timing-aware and congestion-aware pin placement and feed-through insertion. The data flow graph-driven automatic macro placement for both top and block level (AMP) ensures the best QoR by facilitating design space exploration with multiple parallel recipes, which significantly reduces the number of macro placement iterations. Olympus-SoC offers the highest tool capacity, compact memory footprint, and intuitive, easy to use GUI.
Olympus-SoC reduces area with technologies like the unified global router-based congestion modeling, intelligent white space management, smart MP fixing for nested and interdependent cycles, Fin grid-aware placement, Vt- and implant-aware spacing and concurrent SI and MP fixing.

Other area reduction technologies used throughout the flow include proprietary density management, dynamic area recovery, and congestion mitigation through clock tree synthesis (CTS) and post-CTS optimization.

**Highest Performance**

Leading-edge designs need to be analyzed and optimized for various design contexts and timing variations due to device/interconnect scaling. Using approximations, like constraint merging or adding margins, results in loss of accuracy that impacts design performance, and time-to-market. Designers can avoid unpredictability in sign-off ECO loops, eliminate performance-killing pessimism, and speed the time-to-tapeout by considering all the scenarios concurrently, from floorplanning to GDSII-out.

Olympus-SoC’s patented and tape-out proven multi-corner–multi-mode (MCMM) architecture drives the router and optimization engines to automatically achieve best timing and SI across all modes and corners concurrently. Additional technologies such as 3D opportunistic shielding of clock nets, CTS-based timing optimization and advanced trap placement help push the performance envelope.

**Clock Tree Synthesis**

Variations in resistance can cause large deviations in clock skew across different process corners. Olympus-SoC addresses this problem by using advanced MCMM clock tree synthesis technology to optimize skews across all process corners concurrently. This results in robust, low-power clock trees that are resilient to process variations and show significant improvement in the number of buffers, total area, timing and power. Advanced OCV-driven CTS helps significantly improves timing, both setup and hold, and speed up design convergence time.

**Productivity and Big Data**

Olympus-SoC has an ultra-compact database that provides the industry’s highest capacity and smallest memory footprint, allowing it to handle 100 million + instance designs. Patented physical synthesis technology gives highly-optimized results for multi-million gate flat designs in a single overnight run.

Fully-multithreaded and distributed analysis and optimization engines and a fully-parallelized timing and optimization engine reduce run times by efficiently using the latest platforms, providing a significant speedup. The combination of these features allows designers to achieve design closure on large complex designs in a fraction of the time required for existing design flows.

**Low-Power Support**

Olympus-SoC provides seamless concurrent optimization for both power and timing, covering all operating modes and process corners through all stages of the flow. Olympus-SoC supports the Unified Power Format (UPF) throughout the netlist-to-GDSII flow, including the ability to describe design intent through power state definition tables.

A multi-voltage layout shown in Olympus-SoC. The shaded areas at left and right are separate power domains. All Olympus-SoC engines honor power domain boundaries.

Olympus-SoC completely automates multi-supply-voltage design flows with automatic power grid routing for multiple voltage supplies, support for dynamic voltage and frequency scaling (DVFS) to handle varying supply voltages and clock frequencies, and auto placement and routing of special cells such as level shifters, isolation cells, and MTCMOS switches.
Olympus-SoC also provides concurrent multi-Vt optimization, power gating, retention flop synthesis, support for gas station methodology flows, and power-aware buffering and sizing. Power-aware CTS minimizes power in the clock network with smart clock gate placement, slew shaping, clock gate cloning/de-cloning, register clumping and concurrent MCMM optimization, which ensures a balanced clock tree with optimal power.

Premier Chip Assembly Flow
Olympus-SoC allows designers to read in all the partitions of a large, complex design without any timing or physical abstractions, and to optimize the top level with a seamless view of the whole chip. This improves chip closure by enabling accurate top-level interface logic optimization with fewer iterations and engineering resources.

The key strengths of Olympus-SoC for top-level optimization in flat or hierarchical flows include ILMs with physical information (PILMs) for more accurate timing, SI, and DRC analysis and optimization, hierarchical timing policy that reduces memory requirements and runtime, accurate physical SDCs, timing and congestion-driven pin assignment, port sliding and layer promotion for improved timing.

Olympus-SoC also offers synchronized optimization to automatically update any change in one instance of a replicated block to all other instantiations of the same block at the top level.

Key Features
■ Design Planning
  – Design planning including flat, hierarchical, and pseudo flat floorplanning
  – Support for both channel-less and channel-based flows
  – Timing and congestion aware pin placement and feed-through insertion
  – Data flow graph driven automatic macro placement
  – Timing-driven placement engine for optimal QoR
  – Powerful and efficient GUI

■ Flexible Routing
  – Native coloring, verification and conflict resolution
  – DRC and DFM rule support for all key nodes and foundries
  – Intelligent conflict double/multi-patterning resolution engine
  – Pattern matching and recommended rules support
  – Variation-aware timing and SI driven routing

■ Low Power
  – UPF 2.0 (IEEE 1801) based multi-voltage flow
  – Power state table (PST) based advanced buffering
  – Support for level shifters, isolation cells, and retention registers
  – Distributed and ring style multi-threshold (MTCMOS) switch cell insertion
  – Hierarchical UPF support
  – Power-aware CTS featuring cloning, restructuring, and slew shaping
  – Concurrent power and timing optimization for all corner/mode/power scenarios

■ High Performance
  – True and concurrent MCMM optimization during all design steps
  – Best-in-class MCMM-based CTS
  – On-chip variation (OCV) driven CTS and opportunistic 3D clock shielding
  – Resistance-aware concurrent cell and wire optimization
  – Extremely fast and accurate, on-the-fly parasitic extraction
  – Sign-off quality timing analysis and optimization

■ Area Reduction
  – Unified global router based congestion modeling
  – Channel-less floorplanning flow
  – Intelligent white space management
  – Precision DP fixing for minimal perturbation
– Dynamic area recovery throughout the flow
– Proprietary density management

■ TAT Reduction
– Distributed and multithreaded analysis and optimization
– Signoff physical verification during implementation with Calibre InRoute
– Minimal ECO iterations through MCMM optimization
– Signoff quality built-in timing and extraction engines
– Industry’s first multi-threaded timing engine

■ Highest Capacity
– Compact database and flexible architecture
– Ability to handle 100+ million instance designs
– Flexible abstraction capabilities including SI-ILM, HTP, and black boxes
– Unique synchronized optimization at the top-level design
– Advanced memory reduction technologies