Automated Fill Solutions
Calibre® YieldEnhancer’s SmartFill

SmartFill combines advanced design density analysis with multiple filling solutions to mitigate
manufacturing challenges for advanced node designs.

SmartFill Density Analysis and Filling
Fill has been essential to the successful manufacturing of IC designs for many
nodes. Adding non-functional polygons to open areas in a layout helps ensure
layer planarity during chemical/mechanical polishing (CMP).

At leading-edge process nodes, however, fill helps mitigate additional
manufacturing issues, such as manufacturing stress, and helps reduce the
variability caused by etch, lithography, and rapid thermal annealing. In addition,
expanding design sizes combined with the shrinking space and feature size of
these layouts requires new fill shapes to ensure open areas can be effectively filled
and remain DRC-compliant. This increase in both the role of fill and the number of
fill shapes has led to an exponential growth in the amount of fill used in a design.
New strategies are needed for fill management and database control to ensure
the design process remains manageable, the fill process remains effective, and the
impact on schedules is minimized.

The Calibre® YieldEnhancer product’s SmartFill capability combines advanced
design density analysis with multiple filling solutions to supply the optimum filling
strategy for correct-by-construction results in both digital and custom/analog
designs. The SmartFill process allows designers to satisfy complex IC fill
constraints in a single pass, with minimal impact on circuit performance. SmartFill
also produces a smaller post-fill GDS database and faster runtimes, compared to
dummy fill.

Advanced Fill Rule Decks
At advanced technology nodes, density constraints expand to include control of
variations between adjacent windows (gradient), including local and chip-wide
gradient targets. Other new requirements include balancing of perimeter values
on a layer-by-layer basis, and uniformity of fill spanning multiple layers. Foundries
and independent device manufacturers (IDMs) provide fill rule decks that include
these constraints to ensure fill placement is both optimized and DRC-clean. With
its innovative fill techniques, the SmartFill process enables rule deck developers to

www.mentor.com
implement checks that accurately and efficiently analyze rule compliance. In fact, most foundries and IDMs use SmartFill technology as their tool of choice for fill rule deck development because it delivers correct-by-construction results.

With this added complexity, designers need an environment specifically tuned for the expanding set of fill constraints. The SmartFill tool offers specialized functions that address new requirements like cell-based fill, as well as functions that maximize the fill insertion rate and manage color-aware and finFET fill. SmartFill analysis capabilities evaluate the fill constraints and automatically determine the best fill patterns and shapes to ensure compliance.

Cell-Based Multi-Layer Fill
Designers must now add fill not just to metal layers, but also to poly, diffusion, and via layers. The SmartFill cell-based fill approach enables designers to define a multi-layer pattern of fill shapes that can be repeated in many places across the chip.

Multi-Patterning Compliance
Fill in multi-patterning (MP) designs, like many of the drawn shapes, must be decomposed into separate masks. At 20 nm, fill coloring is assigned to balance the mask loading. At smaller nodes, fill shapes are colored based on the color of the drawn layers. The SmartFill process automatically enables “color-aware” fill to ensure MP layouts remain compliant after filling.

FinFET Fill
SmartFill functionality ensures the regularity of fill shapes as required by the fill process. The selection of fill shapes and placement in both the x and y coordinates automatically maintains the pitch and uniformity required for finFET transistors.

Efficient Design Methodologies for Fill
Because the latest designs require billions of fill shapes, there are several important design flow issues. At 20 nm and below, almost all designers adopt a “fill as you go” strategy using a hierarchical approach, which allows design teams to control both the fill database size, and run time for fill and post fill DRC. In addition, keeping fill information separate from the design database is now a common practice to avoid slowing down design tool response. SmartFill allows designers to keep fill in a separate DB and only merge with the design DB when required. By raising the level of abstraction from individual polygons to a cell-based solution, the SmartFill process helps control not only fill database size, but also fill runtime.

ECO Fill
Another critical design flow issue is minimizing the impact of an ECO change on fill. The SmartFill process incorporates an ECO fill strategy that ensures late design changes can be implemented and the design refilled quickly and efficiently while minimizing runtime, fill database size, and timing impacts. This ECO fill flow uses the same fill sign-off deck for both the initial and ECO fill flow, and restricts the ECO fill operation only to those areas where actual mask-making changes occur, which limits the size of the region that must be evaluated for errors, edited, and refilled. All other fill shapes are kept in their original locations so that re-timing is limited to the ECO changes.

The SmartFill ECO process reduces fill runtime, manages fill file size, and minimizes timing impacts. If the ECO changes require a design re-spin, the SmartFill flow enables designers to minimize the number of new masks required. By using the power of the Calibre platform to analyze the design with the sign-off verification tool, only those layers that are affected are modified.

Fast Implementation and Lower Ramp Time
Because the leading foundries use SmartFill technology and provide foundry-qualified Calibre signoff rule decks, your advanced fill learning curve is minimized, enhancing your productivity and time to market. Using the same fill technology as your foundry not only ensures signoff-quality results, but also provides the earliest qualification during new process ramps.

For the latest product information, call us or visit: www.mentor.com

©2015 Mentor Graphics Corporation, all rights reserved. This document contains information that is proprietary to Mentor Graphics Corporation and may be duplicated in whole or in part by the original recipient for internal business purposes only, provided that this entire notice appears in all copies. In accepting this document, the recipient agrees to make every reasonable effort to prevent unauthorized use of this information. All trademarks mentioned in this document are the trademarks of their respective owners.