Introduction

Xpedition® Package Designer is a complete, powerful, and proven design solution for High Density Advanced IC Packaging (HDAP). It delivers leading-edge capabilities throughout the design process, enabling designers to start designing from scratch using Layout Driven Design (LDD) and move all the way through to final sign-off and mask-ready manufacturing output. Combining ease-of-use with innovative design functionality including verification and electrical model extraction, Xpedition Package Designer is the industry’s most comprehensive solution for HDAP.

Xpedition Package Designer supports single- and multi-die configurations and a variety of attachment technologies including wire bond, flip-chip, stacked-die, system-in-package (SiP), and package-on-package (PoP). It also supports the latest silicon-based technologies, such as fan-out wafer level packaging (FOWLP) and 2.5D interposers without requiring costly add-ons or upgrades.

Key features in Xpedition Package Designer include:

- High Density Advanced Packaging (HDAP, FOWLP etc.) ready
- Comprehensive import and construction utilities for device creation
- Rapid, on-the-fly, route-driven, connectivity logic creation via Layout Driven Design
- 2D/3D editing and visualization all within core layout

FEATURES AND BENEFITS:

- Enables designers to meet size, performance, cost, and manufacturing requirements in a predictable, reliable process
- Provides faster, predictable design completion through real-time design visualization and interaction in 2D and 3D
- Removes/reduces time-consuming, post-design, signoff-driven ECOs by enabling designers to address design-for-manufacture requirements during design with integrated HyperLynx DRC
- Reduces the post-design task of creating SI/PI 3D simulation model creation with the integrated HyperLynx Fast 3D field solver
- Shortest path and cycle time to full GDS, LVS, and LVL signoff through integration with Calibre
- Capacity and performance for the largest flip-chip designs (10K pins and up)
- Patented sketch-routing technology for the industry’s highest routing productivity
- Fast, accurate area fill/plane processing for the smallest geometries
- Embedded HyperLynx 3D quasi-static field solver for package model creation
- User-customizable HyperLynx DRC engine for in-process verification of complex rules
- Fast, predictable path to GDS verification & signoff

Optional technologies that integrate with Xpedition Package Designer include HyperLynx® power integrity, signal integrity, and 3D full-wave EM analysis tools, FloTHERM® CFD thermal modeling, Valor® NPI organic substrate fabrication checking, and Calibre® nmDRC/RVE for wafer-level mask foundry signoff.

Meeting the HDAP Challenge
A common response to today’s system scaling demands is advanced packaging technology. Popular options include FOWLP, 2.5D multi-substrate/multi-device interposers, system-in-package (SIP), or high-density flip-chip. A common theme across these technologies is the unique challenges they present to traditional design tools and methodologies. It might be accuracy and GDS quality for FOWLP, capacity and performance for high-density flip-chip, or 2D/3D interoperability for multi-substrate/multi-device interposers.

Xpedition Package Designer has been engineered and architected to specifically address the disruptive challenges of HDAP design. It delivers innovative design automation, verification, optimization, and yield-enhancing technology to ensure your design meets all performance, manufacturing, and reliability requirements.

Fast and Flexible Design Creation
Powerful import utilities enable the rapid capture of die, interposer, or BGA data from a variety of sources including csv/txt, AIF, ODB++, and DXF. Easily create devices on-the-fly with parametric construction including advanced features for asymmetrical pattern support. Start designing with or without a netlist using the Layout Driven Design (LDD) features.

Multi-Substrate Optimization with Xpedition Substrate Integrator
Pre-optimized IC package designs can be imported from Xpedition Substrate Integrator, significantly accelerating initial design while ensuring compatibility with the die and PCB. Tuned connectivity assignments and routing from detailed implementation can be back-annotated to Xpedition Substrate Integrator for review and system-level impact assessment (Figure 1).

2D/3D Interoperability
Design and verify complex packages in a fully supported 3D environment that’s seamlessly integrated within the design canvas. Simultaneous 2D/3D editing and checking can be done within the core layout, without add-ons or separate windows, and comprehensive built-in 3D DRC easily detects and avoids 3D-related designs issues.

Performance and Capacity for the Largest Designs
Many of today’s packages for high-performance server, networking, or computing applications exceed 10,000 pins which can be challenging for legacy design tools. Xpedition Package Designer delivers the capacity, performance, and efficiency for these large designs and has been proven on designs exceeding 30,000 pins.

Figure 1: Package prototyping in Xpedition Substrate Integrator
Comprehensive Wire Bonding

Cost-sensitive SiP packages for mobile or IoT applications utilize die-to-die wire bonding as a method for minimizing substrate layers and cost. Xpedition Package Designer provides a rich and powerful suite of automation and editing capabilities within a real-time 3D DRC environment for fast, accurate generation of the most complex bonding scenarios (Figure 2).

Parametric bond-shell automation integrates the construction and generation of complex wire bond and power rings. Multi-tier, multi-ring scenarios are supported along with push-and-shove editing for precise refinement. User-definable wire profiles enable construction of complex high-density bonding with 3D DRC providing the confidence that the package is correct and can be manufactured.

High-Performance Routing

Patented sketch-routing technology combines the power of automatic routing with user control and guidance for high-quality results with exceptional performance. It’s ideal for the non-uniform, flow-oriented routing common to both single- and multi-die packages. The sketch-plan feature makes it easy to do floor planning and coordinate large busses by defining editable paths for establishing intent and an overall route flow. Easily optimize and order traces into high-density, multi-row bump or ball patterns.

Sketch-route features reduce the interactive routing effort by minimizing incremental mouse clicks. A powerful plowing algorithm can push and shove traces and vias with automatic plane-clearing and healing to deliver high-quality results. Sketch routing also provides smooth movement of large trace groups with automatic removal of extra segments, even across rule areas. It supports automatic differential pair routing with symmetrical pad entry and short convergence, including broadside or adjacent pair routing (Figure 3).

High-Speed Design

Many package designs have strict requirements for maintaining signal quality and performance. Designers must manage signal quality as part of the design process to achieve system performance and reduce iterations. High-speed design is an integral component of Xpedition Package Designer with support for electrical performance constraints and dynamic DRC of high-speed rules. It provides both automatic and interactive tuning of high-performance interfaces. Tuned nets are maintained automatically throughout the design process.

Differential pairs are easily implemented and managed. Impedances can be controlled by layer and pair-spacing rules can be established by both layer and net class. If one trace is edited, the other trace in the pair automatically moves with it. Adjacent-layer differential pair routing capabilities add another valuable option for routing critical signals on dense substrates.
Rules by Area

The rules-by-area function greatly improves routing around flip-chip bump patterns and other arrayed devices. Rule areas represent complete rule sets that are obeyed by online and batch DRC and during interactive and automatic routing. Rule areas can be defined by layer and assigned to any polygon, rectangle, or circle. Trace widths and clearances automatically change when within the rule area. Designers can also change via sizes and spans to maximize route completion in high-density areas (Figure 4).

Efficient Via Definition and Management

Routing advanced-packaging substrates requires the use of complex via patterns in a variety of configurations such as stacked, staggered, spiral, or staircase. Many substrates have core layers that require a larger via than the build-up layers, adding additional complexity to these patterns. The constraint-driven approach of Xpedition Package Designer to these complex patterns eliminates the error-prone, time-consuming process of having to build dozens (or even hundreds) of unique pad stack definitions corresponding to all potential layer combinations.

Xpedition Package Designer utilizes a set of robust via rules to generate patterns as needed using basic pad stacks definitions (Figure 5). This results in a much more efficient approach without the pad stack library overhead. An additional benefit is the ability to automatically remove unused vias from the pattern once routing is satisfied, freeing up space on adjacent layers.

Dynamic Metal Area Fill

Advanced packages have a number of unique area-fill requirements that are beyond the capability of legacy tools’ generalized fill algorithms. Xpedition Package Designer delivers industry-leading accuracy and performance in area-fill implementation and processing. Native capabilities eliminate the need for error-prone secondary processing of complex patterns. Dynamic planes enable rapid push-and-shove of traces and vias with automatic plowing and healing of the metal areas while maintaining design rules.

Many of today’s FOWLP technologies require unique stress relief and degassing features in their designs. Xpedition Package Designer supports a number of these features, including octagon cutouts and graduated degassing voids (Figure 6).
Predictable Quality and Accuracy of Results

While Xpedition Package Designer employs a correct-by-construction methodology to ensure design accuracy, there are additional features that drive its efficient, predictable, high-quality results. One example is the use of true arc and circle database constructs that minimize GDS errors due to polygon faceting. Another is its patented bump-compensation technology that expedites die changes while ensuring accurate trace and via alignment. An optimized GDS output algorithm helps ensure accurate output and representation of non-Manhattan geometries.

To support an increasing number of HDAP technologies and ecosystem providers, use of vendor-specific Process Design Kits (PDK) is becoming standard practice. Elements and constraints from Xpedition Package Designer, HyperLynx DRC, and Calibre can be captured and incorporated into these PDKs. The PDKs enable foundries and OSATs to develop and deliver process optimized rules to their customers.

Manufacturing Readiness

HDAP and FOWLP design rules continue to evolve as manufacturers refine or introduce new processes. A number of these rules present unique challenges to DRC engines in legacy design tools. To address the rapidly changing design rules of HDAP/FOWLP, Xpedition Package Designer includes HyperLynx DRC technology which combines a powerful geometry processing engine with a field solver.

Fast, Full-Package Electrical Model Generation

Xpedition Package Designer also includes the proven HyperLynx Fast 3D Solver for full-package model extraction (Figure 7). It’s ideally suited for power integrity, low-frequency SSN/SSO, and complete-system SPICE model creation while accounting for skin effect impact on resistance and inductance. Multi-core parallel processing drives extremely fast run times, allowing multiple “what if” scenarios to be run in a minimal amount of time. This enables package designers to quickly deliver models for inclusion in signal integrity simulation by the package’s consumer, often a system designer integrating the package into a PCB design.

Final Mask Signoff

Based on IC foundry methodologies and techniques, many leading and emerging HDAP processes demand GDSII and IC-like manufacturing constraints on metal areas to control yield, process out-gassing, and improve design quality. As with IC fabrication, the GDSII mask data undergo rigorous verification against very detailed process design rules (PDK).

Figure 7: Xpedition Package Designer includes a built-in, HyperLynx, quasi-static, 3D full-package simulation model generator that allows designers to quickly and simply generate a model for inclusion in signal integrity simulation.
The industry’s golden standard for this verification/signoff process is Calibre (Figure 8) which is integrated with Xpedition Package Designer to ensure fast, efficient, and accurate GDSII mask signoff. Direct integration enables back-annotation and error display in Xpedition Package Designer to ensure the layout database matches the manufacturing output.

3D Electromagnetic Simulation

Optional HyperLynx 3D electromagnetic simulation solutions for signal integrity, power integrity, and EMI (electromagnetic interference) address the challenges for chip-package-board design, enabling users to quickly and accurately generate S-parameter models for full system analysis.

Thermal Analysis

As products get faster and smaller, thermal management issues increase. Adding FloTHERM to the Xpedition Package Designer flow provides thermal-analysis capabilities for the complete IC package, from detailed, substrate-level, power hotspots to complete thermal modeling of packages for use at the PCB and system level (Figure 9).

Figure 8: Full verification signoff is streamlined through direct integration of advanced Calibre DRC signoff validation with the designer’s Xpedition Package Designer desktop.

Figure 9: Complete package signoff can include detailed thermal analysis and modeling using FloTHERM.

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