Constraint Management

Overview
As PCBs increase in complexity and density, a higher percentage of the design must be implemented with strict adherence to design rules. Manual documentation, translation, and interpretation of design rules often cause longer product development cycles and increased costs. The constraint manager in Xpedition provides a fully integrated, constraint-driven design methodology that reduces design costs and time-to-market by automating design rules communication and eliminating unnecessary PCB prototypes and re-spins. It provides both electrical engineers and PCB designers with direct control over the most advanced routing technology in Xpedition to solve current and future system design requirements.

Constraint Integration Throughout the Design Flow
The constraint manager supports bi-directional cross probing, highlighting and selection between a spreadsheet-based constraint interface, and schematic capture and physical design tools in the flow. Constraint values are fully synchronized during the forward and backward annotation processes with intelligent handling of connectivity changes. You can also import constraint templates developed with Mentor Graphics HyperLynx® pre-layout environment.

Concurrent Design
Increased complexity puts more pressure on design teams to get things done on time. The constraint manager allows many designers to work on the constraint data at the same time. The database architecture was designed to allow multiple edits simultaneously. This eliminates overhead of manual techniques that other systems must use. Locking mechanisms prevent concurrent users from editing the same data, and also provide notification of who is changing which data to the team. This means project schedules can be met by applying more resources to a project.

MAJOR BENEFITS:
- Single, integrated constraint entry and edit tool for design, layout, analysis, and manufacturing rules.
- Powerful and easy-to-use spreadsheet-like GUI guided by the design database and cross probing to applications.
- Hierarchical constraint entry speeds input of complex rules on many objects.
- Speeds time-to-market with informal and formal constraint reuse, concurrent constraint entry, and editing.
- Improves design productivity with extensions allowing in-tool constraint editing.
Hierarchical Rule Classes

Users can create hierarchical rule classes that greatly ease the association of constraints to design objects. With more common “flat” systems, users must apply constraints to many individual nets or pins, but with the use of hierarchy, and the inheritance of constraints that this facilitates, those same nets can be constrained by one rule at the class level. This greatly reduces the number of constraints manually entered in the design; when changes occur, due to packaging or other requirement changes, constraint modification is simple and straightforward.

Topology Assignment

The constraint manager allows user-defined and pre-defined automatic topologies. Users can create a topology and associated constraints with virtual pins or they can use the more sophisticated automatic topologies where the Xpedition layout environment intelligently manages virtual pin locations.

Parallelism/Crosstalk Rule Assignment

The constraint manager provides a simple parallelism rule creation and assignment dialog box. Parallelism rules apply on the same or adjacent layers and can be assigned at the net or class level for maximum control and flexibility. Alternatively, users may provide constraints on a crosstalk basis; that is, using electrical specification of the rules as well as physical (parallelism) rules.

Net Class Schemes

Schemes allow users to have area-specific manufacturing constraints, which override the design-wide or layer specific constraints. These include constraints such as widths and clearances, which may have to be modified, for example, around a Ball Grid Array device. These schemes are then mapped to rule areas in the layout environment.

Differential Pair Creation

Differential pairs have become more and more prevalent in designs. Users can easily assign these with a differential pair finder utility. This utility allows users to assign differential pairs using common naming conventions, wild card searches on net names, and information from interactive selection of pairs of nets across the entire design.

Impedance Planning

Users can view or modify the stackup properties associated with a design. By doing so, users can verify existing stackup characteristics, such as differential pair impedance, modify layer attributes, and/or augment the stackup to meet width, spacing, and impedance constraints. This is the same stackup editor and field solver used in HyperLynx, the industry leading signal integrity analysis tool.