Tanmay Arvind

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Education

Georgia Institute of Technology **Expected Graduation: Dec 2025**

Bachelor of Science in Electrical Engineering and Computer Science *GPA: 3.94*

Relevant Coursework

- VLSI, Advanced Digital Design, Verification
- Computer Architecture
- Physical Foundations of Computer/Silicon Engineering
- Embedded Systems Design
- Machine Learning, Neural Networks
- Microelectronics, Circuit Design and Analysis
- HW/SW System Programming (C, C++, Python)
- ECE Design Lab & Rapid Prototyping
- Control System Design and Feedback
- AI Foundations and Hardware Acceleration

Experience

NVIDIA **May 2025 – Present**

GPU/ASIC Hardware Engineering Infrastructure Intern *Santa Clara, CA*

- Supporting efforts on AI-driven programming, workflow acceleration, RTL build efficiency, compute farm/LSF.
- Developed Python/YAML automation suite to provision pre-built, access-controlled RTL caches for rapid DV and design iteration; reduced manual setup to 10 second execution (99% reduction) runtime with integrated security handling.
- Built secure CLI tool to automate creation and cleanup of access-controlled content distribution namespaces.
- Modernized legacy infra scripts via Perl-to-Python conversion pipeline; experimented across model context selection, prompt techniques, dependency resolution, code patterns to develop AI-driven optimal code conversion methodology.
- Built Cursor rules package with embedded best practices and top-level orchestrator for automated, optimal script conversion; developed agentic AI system for scalable conversions with generative unit test framework/feedback loop.

RWE AG **Jun 2024 – Aug 2024**

Operations Hardware Engineering Intern *New York, NY*

- Developed Python scripts (NumPy/Pandas) and SCADA integration for real-time power-plant fault detection, reducing manual intervention by 250+ hours/year and improving resolution times by 50% through predictive pattern recognition.
- Spearheaded cross-functional (engineering, tech, software) root-cause analysis investigation on transformer loss discrepancies with Schneider Electric, using PI Datalink, Power BI, statistical analysis, saving 8 MWh/week in losses.
- Collaborated with 6 interns to propose AI strategy for process automation using Python (TensorFlow, PyTorch), MS Copilot, AWS, estimated to boost productivity by 25% for US DevOps, projected $4M savings over 5 years.

Wreck Techs at Georgia Tech **Apr 2023 – May 2024**

Resident Technology Engineer *Atlanta, GA*

- Orchestrated and maintained 35+ Ethernet/fiber-optic systems, repunched data cables, conducted UART signal tests.
- Provided onsite HW/SW support to 500+ students annually achieving a 98% success rate in incident resolution.
- Coordinated IoT device setup and resolved 20 incidents involving WiFi/ MANETs installation repair with IP testing.

Larsen and Toubro (L&T Ltd.) **May 2023 – Jul 2023**

Engineering and Technology Development Intern - Digital SCM *Mumbai, India*

- Boosted L&T's B2B market platform adoption by 11% WAU with Python, Power BI visualizations of 1.2M orders.
- Created a buyer dashboard now used by 15,000+ employees/clients, improving purchase turnaround times by 20%.
- Implemented ML frameworks (LightGBM, Random Forest) for material categorization, increasing accuracy by 80% and cutting procurement timeline by over 50%.

Doori: Pandemic Prevention Prototypes **May 2020 – Jun 2023**

Co-Founder *Mumbai, India*

- Conceptualized IoT home-automation devices for touchless door/appliance operation, directed complete process of digital logic design, circuit design, and physical fabrication with Arduino, Raspberry Pi, ESP32; controlled by Django web app.
- Conducted ASIC validation & pilot testing measuring 45% enhancement in contagion prevention in locality.
- Integrated sensors (HC-SR04, CMOS Cameras, Servo) with CV ML models, achieved 96% object detection accuracy.

Projects

Custom SoC ALU Pipeline: Physical Design, VLSI & DV | *Cadence Virtuoso, Spectre* **Jan 2025 – May 2025**

- Designed ALU with subtraction, 2's complement, and overflows using schematic and layout tools in Cadence PD.
- Performed transistor-level simulation & timing analysis using Spectre/ Calibre to evaluate critical path delays.
- Executed full custom SoC layout physical design with DRC/LVS checks, architectural functional modeling, pre-silicon waveform-based functional design verification.

Accelerated Deep Learning Projects | *PyTorch, CNNs, Transformers, CUDA* **Jan 2025 – May 2025**

- Implemented CNN, RNN, and Transformer models in PyTorch for image classification, clustering, and sequence tasks.
- Developed MLP and convolutional autoencoders for image reconstruction and anomaly detection; won 1st place in Kaggle competition (96.44% reconstruction accuracy).
- Accelerated training of ResNet, AlexNet, VGG on GPUs; explored Grad-CAM, transfer learning, explainability.

Nvidia AI Makerspace: AI Acceleration for HPC | *PyTorch, OpenCV, Seaborn, CUDA* **Aug 2024 – Dec 2024**

- Developed high-performance deep learning models & implemented CNN architectures (AlexNet, VGG; with ReLU Activation) on LiDAR data with parallel data structures for real-time ML inference optimization.
- Performed logistic regression for fraud detection, optimized with Euclidean computations and Seaborn visualizations.
- Leveraged Nvidia H100 HGX GPUs on GT supercomputing cluster for CUDA-accelerated high-performance computing.

Computer Architecture: Multicycle Processor Design | *RISC-V Assembly, C/C++, Verilog* **Aug 2024 – Dec 2024**

- Simulated a high-performance multi-cycle processor using SystemVerilog with out-of-order execution and parallel programming on ModelSim (Siemens), executing multiple pipelined instructions per clock cycle.
- Implemented required data structures and algorithms to optimize CPU cache with LRU policy and hierarchy, built custom ALU, LSU, Decode, RAM units, programmed RTL memory-register file interfaces with virtual memory.
- Designed and validated a hierarchical memory architecture with functional modeling to simulate latency, throughput, and performance tradeoffs.

DE-10 FPGA Peripheral Solar Tracker | *VHDL, Assembly, Intel Quartus Prime* **Aug 2023 – Dec 2023**

- Interfaced Quartus with real-time photocell to dynamically adjust solar panel orientation, increasing generation by 35%.
- Validated & built analog design using oscilloscope and signal generator ensuring optimal calibration of servo peripheral.
- Programmed peripheral using VHDL with light source angle detection algorithm on Assembly (to 0.5 degree precision).

Skills

Languages/Frameworks: Python, C, C++, Verilog, VHDL, MIPS Assembly, RISC-V, MATLAB, PyTorch, Nvidia CUDA
Hardware: FPGA (Intel Quartus), GPUs (H100), ARM Mbed, ModelSim, Altium, Oscilloscope, DMM, PCB Fabrication
Software Tools: Git, AutoCAD, Power BI, LabVIEW, Seaborn, SCADA, MS Office (Copilot), Aveva PI, Unix, OpenCV
Technologies: Parallel Computing, Digital/Analog Circuit Design, RTL, AI-powered Programming, Signal Processing