Nujhat Tasneem

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Google Scholar: https://scholar.google.com/citations?user=JSw5PqYAAAAJ&hl=en

Education

Georgia Institute of Technology | Atlanta, GA *Aug 2017 – Present*
PhD in Electrical and Computer Engineering, **Current CGPA:** 3.92/4.00 Expected Graduation, *Dec 2022*

Bangladesh University of Engineering and Technology | Atlanta, GA *Feb 2011 – Mar 2016*
BS in Electrical and Electronic Engineering, **CGPA:** 3.93/4.00

Skills

Microfabrication	Process flow design, Device fabrication and optimization, including lithography, deposition, etching, metrology, ion Implantation, oxidation etc.
Characterization	Low Temperature (cryogenic) and high temperature electrical characterization (I-V, P-V, C-V), Pulsed I-V, Reliability testing.
Programming and Simulation Tools	MATLAB, Python, ATHENA Supreme, Cadence Virtuoso, LTspice, COMSOL Multiphysics.
Relevant Courseworks	Microelectronics Technology, IC Fabrication, Giga-scale Integration, Advanced VLSI systems, Digital System in Nanometer Nodes, Biomedical Applications of MEMS, Machine Learning, Linear Algebra.

Research Interest

Semiconductor process integration, Semiconductor device physics, Memory technologies, Ferroelectric devices, Logic transistors, Material characterization.

Research Experience

Graduate Research Assistant – Georgia Institute of Technology *Aug 2017 – Present*

- Designed and fabricated Ferroelectric Field Effect Transistors (FEFETs) and performed systematic experimental investigation of these devices to understand the underlying device physics, necessary to optimize its design, especially as a non-volatile memory (NVM) element.
- Investigated the trap dynamics during write operations in ferroelectric field-effect transistors (FEFETs) by directly and separately measuring the trap related hole and electron currents through the body terminal and shorted source-drain, respectively (IEDM 2021).
- Explored the thickness scaling effect on the ultra-thin antiferroelectric zirconia (ZrO2) films and discovered that the critical electric fields (*E*) for antiferroelectric phase transition in ZrO2 follows the Janovec-Kay-Dunn Law, $E \propto d^{-2/3}$, where *d* is the crystallite size of the material (Advanced Electronic Materials 2021, cover story).
- Co-led the detection of antiferroelectric negative capacitance employing pulsed measurement on the dielectric-antiferroelectric heterostructure (arXiv 2020, accepted in Nature Communication, 2021).

Undergraduate Thesis – Bangladesh University of Engineering and Technology *July 2015 – Mar 2016*

- Evaluated Electrostatic & Transport Characteristics of Different Structures of Junction Less Nanowire Field Effect Transistor Using Self-Consistent Analysis.

Publications (Selected)

1. "*Antiferroelectric negative capacitance from a structural phase transition in zirconia*", M. Hoffmann, Z. Wang, **N. Tasneem**, ... & A. I. Khan, Accepted in Nature Communications, 2021.
2. *"Trap Capture and Emission Dynamics in Ferroelectric Field-Effect Transistors and their Impact on Device Operation and Reliability"*, **N. Tasneem,** Z. Wang, Z. Zhao, N. Upadhyay, S. Kurinec, S. Datta, S. Yu, K. Ni, M. Passlack, W. Chern, & A I. Khan, Accepted in IEEE International Electron Devices Meeting, 2021.
3. "Standby Bias Improvement of Read After Write Delay in Ferroelectric Field Effect Transistors", Z. Wang, **N. Tasneem**, J. Hur, H. Chen, S. Yu, W. Chern, A. I. Khan, Accepted in IEEE International Electron Devices Meeting, 2021.

4. "*Efficiency of ferroelectric field-effect transistors: An experimental study*", **N. Tasneem,** M. M. Islam, Z. Wang, Z. Zhao, N. Upadhyay, S. F. Lombardo, H. Chen, ... & A. I. Khan, Accepted in IEEE Transactions on Electron Devices, 2021.
5. "*A Janovec-Kay-Dunn-like behavior at thickness scaling in ultra-thin antiferroelectric ZrO_2 films*", **N. Tasneem**, Y. M. Yousry, M. Tian, M. Dopita, S. E. Reyes-Lillo, J. Kacher, N. Bassiri-Gharb, & A. I. Khan, Advanced Electronic Materials, 2021.
6. *"The Impacts of Ferroelectric and Interfacial Layer Thicknesses on Ferroelectric FET Design"*, **N. Tasneem**, M. M. Islam, Z. Wang, H. Chen, J. Hur, D. Triyoso, S. Consiglio K. Tapily R. Clark, G. Leusink, S. Yu, W. Chern, & A. I. Khan, IEEE Electron Device Letters (2021), 42(8), 1156-1159.
7. *"Differential charge boost in hysteretic ferroelectric–dielectric heterostructure capacitors at steady state"*, **N. Tasneem,** P. V. Ravindran, Z. Wang, J. Gomez, J., Hur, S. Yu, ... & A. I. Khan, Applied Physics Letters, 118(12), 122901, 2021.
8. "Charge Trapping Effects on Memory Window in Ferroelectric Field Effect Transistors", **N. Tasneem**, Z. Wang, M. M. Islam, S. F. Lombardo, H. Chen, J. Hur, S. Yu, W. Chern & A. I. Khan, Accepted in IEEE Semiconductor Interface Specialists Conference, 2021.
9. *"On the possibility of Dynamically Tuning and Collapsing the Ferroelectric Hysteresis/Memory Window in an Asymmetric DG MOS Device: A Path to A Reconfigurable Logic-Memory Device",* **N. Tasneem**, A. I. Khan, Device Research Conference, CA, USA, June 2018.
10. *"Interlayer Scavenging in Ferroelectric Hafnium-Zirconium Oxide Metal-Insulator-Semiconductor"*, **N. Tasneem,** H. Kashyap, K. Chae, C. Park, S. Yu, P. Bandaru, K. J. Cho, A. C. Kummel, & A. I. Khan, Submitted to ACS Applied Materials and Interfaces **(Currently Under Review).**

Professional Experience

Graduate Teaching Assistant – Georgia Institute of Technology *Aug 2017 – July 2018*

- Assisted with the *Physical Foundations of Computer Engineering* course designed for ECE undergrads.

Lecturer – BRAC University, Bangladesh *May 2016 – July 2017*

- Conducted undergraduate courses on basic electronic circuits and systems.

Leadership Experience and Synergistic Activities

Member of Executive Committee – Bangladesh Student Association at Georgia Tech *May 2018 – April 2020*

- Served as President (2020-2021), Vice President (2019-2020) and Treasurer (2018-2019).
- Organized various cultural festivals and events, Organized fundraisers, Mentored Bangladeshi Students at Georgia Tech

Mentor – SURE Program, Georgia Institute of Technology *May 2018 – July 2018*

- Served as a Mentor to the SURE Program (Summer Research Program for undergraduate students) hosted by Georgia Institute of Technology.

Member of Executive Committee – IEEE Women in Engineering (WIE) Bangladesh Section *July 2016 – July 2017*

- Served as Technical Activities Coordinator (Jan 2017 – July 2017) and Student Activities Coordinator (July 2016 – Dec 2016).
- Organized multiple technical workshops, Organized entrepreneurship, and leadership development sessions for women engineers in different events.

Accomplishments and Recognition

- *Academic Paper Reviewer:* IEEE Electron Device Letters (IEEE EDL), IEEE Transactions on Electron Devices (IEEE TED), Materials Research Society Advances (MRS Advances).
- Received COVID-19 Disruption GRA Fund in December 2021.
- Travel Grant received to participate in *CRAW Grad Cohort – 2018.*
- Spring 2018 *Colonel Oscar P. Cleaver Award* winner for receiving the highest score in PhD Preliminary exam.
- Fall 2017 Georgia Tech *Institute for Electronics and Nanotechnology (IEN) Seed Grant Program Winner.*
- *Dr. Johurul Haque-Fayaj Zunaid Scholarship* for academic excellence in BUET, 2014.