AADIT PANDEY

404-543-1762 ⋄ aadit@gatech.edu ⋄ 1031 State St NW, Apt. 211, Atlanta, GA 30318

EDUCATION

Georgia Institute of Technology, Atlanta, GA *August 2020 - Dec 2021*
Master of Science in Electrical and Computer Engineering GPA: 4.0/4.0

Georgia Institute of Technology, Atlanta, GA *August 2017 - May 2020*
Bachelor of Science in Electrical Engineering with Highest Honor GPA: 3.79/4.0
Minor in Mathematics

SKILLS

Technical: Op-Amps, Switched-Cap Circuits, Bandgap References, LDOs, Comparators, Biasing, ADC/DAC Architectures, PLLs, LNAs, PAs, Mixers, Oscillators, RF/Microwave Coupler & Filter Design, Smith Charts, Noise & Non-Linearity Analysis
CAD Tools: Cadence Virtuoso, Advanced Design System (ADS), Momentum, LTSpice, NI Multisim
Lab equipment: Oscilloscope, Spectrum analyzer, VNAs, Function Generator, FPGAs, Microcontrollers, Soldering
Software Languages: Python (NumPy, Pandas, scikit-learn, TensorFlow), C/C++, MATLAB

WORK EXPERIENCE

Texas Instruments, Dallas, TX
Analog Design Engineering Intern *June 2021 - Aug 2021*

- Analog Design engineering intern at the PSIL/Power Interface group
- Designed a programmable voltage shunt regulator with output voltage regulation from $V_{ref} = 1.5$V to 42V for given specifications
- Designed a binary-weighted current steering DAC for programmability with step resolution of 2k steps.
- Partnered with business teams and system engineers to develop mutually agreeable design specifications

Georgia Institute of Technology, Atlanta, GA
Graduate Research Assistant at Packaging Research Center (PRC) *Aug 2021 - Present*

- Working as a GRA on RF Chip Embedding on Glass Interposer for 5G Applications under the guidance of Prof. Madhavan Swaminathan
- Designed stack chip-embedding packaging model for 18W GaN Power Amplifier on HFSS satisfying system interconnect Insertion Loss > -0.1 dB for a frequency bandwidth of 1-6 GHz.
- Designed stack chip-embedding packaging model for RF Thru structure on HFSS satisfying system interconnect Insertion Loss > -0.39 dB dB for a frequency bandwidth of 1-50 GHz.

Georgia Institute of Technology, Atlanta, GA
Graduate Teaching Assistant for Analog Electronics (ECE 3400) *Aug 2020 - Present*

- Explained challenging concepts of analog electronics to over 70 students
- Held office hours, wrote assignment solutions and graded assignments & quizzes.

Philips Lighting India Limited, Noida, India
Hardware Engineering Intern *May 2018 - July 2018*

- Performed electrical & thermal testing of Xitanium 60W 0.7A LED Drivers
- Performed PCBA troubleshooting to reduce THD below 8% and increase power efficiency above 90%
- Conducted PCBA failure analysis and rework for 60W 0.7A LED Drivers

Indian Institute of Technology, Delhi, India
Research Assistant in Machine Learning & Neuromorphic Computing *May 2019 - July 2019*

- Simulated a supervised Spiking Neural Network (SNN) with Spike Time Dependent Plasticity (STDP) algorithm as the synapses learning scheme on popular ML datasets including MNIST, Fisher Iris
- Achieved 91.1% training accuracy on MNIST dataset through SNN by enforcing homeostasis in the algorithm
- Demonstrated comparable energy consumption for synaptic weight update during training of the designed SNN with the same for training/on-chip learning of domain wall synapse based non-spiking neural network

PUBLICATIONS

Spike time dependent plasticity (STDP) enabled learning in spiking neural networks using domain wall based synapses and neurons (2^{nd} author). AIP Advances Vol. 9, 12 (2019). (`https://doi.org/10.1063/1.5129729`). This paper was presented at the 64th Annual Conference on Magnetism and Magnetic Materials.

PROJECTS

Design of Wideband Direct Downconversion Receiver

- Designed a wideband direct downconversion receiver in ADS environment using 130nm CMOS technology, targeting an IEEE 802.11 a/g WLAN standard with 2 frequency bands of 2.4GHz and 5GHz.
- Designed a CG-CS noise cancelling LNA to decouple noise design from the input matching design. Designed a double-balanced mixer (Gilbert Cell) driven by differential pair LO Buffer as the mixer stage.
- Tuned parameters of LNA and mixer to achieve low NF, high conversion gain, less non-linearity in accordance with low DC power budget.

Design of Two Stage Pipeline SAR ADC

- Implemented a 13-bit two stage pipeline SAR ADC (with 1 bit redundancy) by designing the SAR Logic, Comparators, Capacitor DAC, Residue Amplifier, Bootstrap/CMOS Switches using 45nm CMOS technology.
- Designed Comparator using the StrongArm Latch topology for low-power consumption.
- Designed a Folded-Cascode OTA for the residue amplifier block. Used g_m/I_D methodology to size the transistors achieving a DC Gain of 76.23dB, GBW of 900MHz and Phase Margin of 43.38°.

Design and Layout of 6T SRAM Cell

- Designed a SRAM Cell in Cadence Virtuoso using 45nm CMOS technology for read/write/hold operations. Designed required peripheral circuits to measure read margin, bit-differential and write margin. Tuned transistor widths to achieve read margin of 450mV.
- Drew the layout of this SRAM cell with the goal of minimizing the area of the cell and ensuring zero "DRC" and "LVS" errors in the circuit.

Design of RF Lowpass and Bandpass Filters

- Designed lumped element and Microstrip transmission line directional couplers on substrate having dielectric constant of 6.15 and loss tangent of 0.002 at a center frequency of 1GHz in ADS environment.
- Performed even/odd mode analysis to derive the S-parameters of the lumped-element coupler.

Design of Two Stage Miller Compensated Op Amp

- Designed a two stage op amp in Cadence Virtuoso using 45nm CMOS technology with Differential Pair with current mirror load as first stage.
- Tuned MOSFET parameters to achieve DC gain of 60.95 dB, phase margin of 45.38°, slew rate of 22.3 V/μS, power dissipation under 281.3μW. Redesigned the first stage as telescopic cascode structure to improve gain.

Design of Directional Couplers

- Designed lumped element and Microstrip transmission line directional couplers on substrate having dielectric constant of 6.15 and loss tangent of 0.002 at a center frequency of 1GHz in ADS environment.
- Performed even/odd mode analysis to derive the S-parameters of the lumped-element coupler.

Vertical Hydroponic Systems (Senior Design)

- Programmed Raspberry Pi to perform real time detection of hydroponically grown plants using OpenCV
- Collaborated with other team members to work on trajectory tracking control for the robot

Smart DE2 Bot (Digital Design Laboratory)

- Implemented the Simple Computer ISA on an Altera Cyclone II FPGA, interfacing with the Altera DE2 Development board peripherals
- Programmed the Simple Computer using VHDL to control a DE2 bot to perform automated detection using sonar sensors & odometry and implemented motion control algorithms to control robot for consistent motion

Jolly Jumper Problem (Controls and System Theory)

- Modelled the classic mass-spring problem on MATLAB Simulink Stateflow using state-space theory
- Simulated special cases such as state transition by impulsive energy input and energy loss in collision

LAME Attack Video Game (Software Design)

- Used C++ concepts of class hierarchy and polymorphic data structures to implement a game on Mbed Microcontroller and display it on LED screen

RELEVANT COURSEWORK

- ECE 6412: Analog IC Design
- ECE 6414: Analog Integrated System Design (Data Converters)
- ECE 6420: Wireless IC Design (RFIC)
- ECE 6360: Microwave Design
- ECE 6130: Advanced VLSI Systems
- ECE 6254: Statistical Machine Learning
- ECE 6445: Power IC Design
- ECE 4550: Control System Design