SUJAY PANDEY

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EDUCATION

Ph.D. in Electrical and Computer Engineering (GPA 3.66/4) *August 2015 - Present*
Thesis Advisor: Prof. Abhijit Chatterjee
Department of Electrical and Computer Engineering, Georgia Institute of Technology

M.Tech in Microelectronics and VLSI Design (GPA 9.46/10) *July 2011 - June 2013*
Department of Electronics and Electrical Communication Engineering
Indian Institute of Technology Kharagpur, Kharagpur, India

CURRENT RESEARCH

Ph.D. Thesis: Effective Scan Test Generation for Efficient Detection of Cell Internal Defects Fall 2015 - Present
Research Assistant

· Focused on development of a scan-compatible test generation approach for detecting open and short defects of variable size in standard cell designs.

Research Internship: Intel custom foundry ASIC graduate intern Fall 16, Summer 16,17

· Worked on various DFT Methodology aspects including the traditional DFT flows for the execution part of the team.
· Researched on the new fault model proposed by Mentor graphics called Cell aware methodology
· Worked on a newer fault model called DFM Aware fault model and published the work in ITC 2017
· Generated ATE patterns for Cell Aware methodology applied to a few standard cell libraries

Publications

· S. Pandey, S. Gupta, M. S. Lakshmipathy, S. Natarajan, A. Sinha, and A. Chatterjee, "Characterization of Library Cells for Open-circuit Defect Exposure: A Systematic Methodology" 2019 IEEE International Test Conference (ITC) (Accepted)
· A. Sinha, S. Pandey, A. Singhal, A. Sanyal and A. Schmaltz, "DFM-aware fault model and ATPG for intra-cell and inter-cell defects," 2017 IEEE International Test Conference (ITC), Fort Worth, TX, 2017, pp. 1-10.

PROJECTS AND TEACHING EXPERIENCE

Design of SRAM Memory System and Arithmetic Unit (Advanced VLSI Design course project)

- Designed an adder system interfaced with an SRAM array that can hold 64 8-bit words. The system key parameters(performance, power, read/write margins) were obtained.
- Achieved full functionality in post-layout simulation at nominal voltage, and compared its performance against pre-layout simulation.

Design of VLSI architecture for motion estimation using HAAR wavelet transform (M.Tech final year project)

- Designed an adder system interfaced with an SRAM array that can hold 64 8-bit words. The system key parameters(performance, power, read/write margins) were obtained.

- Achieved full functionality in post-layout simulation at nominal voltage, and compared its performance against pre-layout simulation.

Graduate Teaching Assistant (Digital systems test course: Fall 2017,2018)

- Worked on designing the exams related to DFT concepts
- Conducted labs related to PODEM algorithm development
- Gained teaching experience by covering lectures on behalf of Professor

TECHNICAL STRENGTHS

HDL and S/W Programming Languages	Verilog, Perl, Python
Engineering Tools	Cadence, MATLAB

COURSEWORK

Advanced VLSI Design, Architectural Design of ICs, VLSI CAD, Advanced Digital Design with Verilog, Digital System Test, Digital System Nanometer Nodes, Physical Design and Automation

HOBBIES

•Playing Badminton •Backpacking and Hiking •Playing Guitar and Drums

WORK EXPERIENCE

Broadcom Communication, Bangalore, India July 2013 May 2015

Engineer, Staff I- IC Design, Low Power Design Team

· Developed algorithm using ring oscillator IP to adapt voltage according to PVT variations.
· Verification of IPs used in the algorithm (in Simulation as well as hardware)
· Lab experiments and data analysis for development and optimization of algorithm
· Exhaustive Lab data collection for Temp. and Voltage sweep on real Silicon
· STA analysis for critical path structures and LAB experiment validation of the same
· Worked with DFT team for current intake measurements and AVS algorithm validation
· Power measurements using DFT and comparison with the specification values
· Bring up of the IPs used in the algorithm on manufactured Silicon

OTHER PUBLICATIONS

- S. Pandey, S. Deyati, A. Singh and A. Chatterjee, "Noise-Resilient SRAM Physically Unclonable Function Design for Security," 2016 IEEE 25th Asian Test Symposium (ATS), Hiroshima, 2016, pp. 55-60.
- S. Pandey, S. Banerjee and A. Chatterjee, "ReiNN: Efficient error resilience in artificial neural networks using encoded consistency checks," 2018 IEEE 23rd European Test Symposium (ETS), Bremen, 2018, pp. 1-2.
- S. Pandey, S. Banerjee and A. Chatterjee, "Error Resilient Neuromorphic Networks Using Checker Neurons," 2018 IEEE 24th International Symposium on On-Line Testing And Robust System Design (IOLTS), Platja d'Aro, 2018, pp. 135-138.
- S. Pandey, S. Banerjee and A. Chatterjee, "Concurrent error detection and tolerance in Kalman filters using encoded state and statistical covariance checks," 2016 IEEE 22nd International Symposium on On-Line Testing and Robust System Design (IOLTS), Sant Feliu de Guixols, 2016, pp. 161-166.

- M. I. Momtaz, S. Banerjee, S. Pandey, J. Abraham and A. Chatterjee, "Cross-Layer Control Adaptation for Autonomous System Resilience," 2018 IEEE 24th International Symposium on On-Line Testing And Robust System Design (IOLTS), Platja d'Aro, 2018, pp. 261-264.

REFERENCES

Ph.D. Thesis Advisor: Dr. Abhijit Chatterjee Fall 15 - Present
Professor, Georgia Institute of Technology

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M.Tech. Thesis Advisor: Dr. Anindya Sundar Dhar Fall 11 - Fall 13
Professor, Indian Institute of Technology Kharagpur

· Email: asd@ece.iitkgp.ac.in, Phone: +91-3222-283516