VINEET NADELLA

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EDUCATION

GEORGIA INSTITUTE OF TECHNOLOGY, College of Engineering **Atlanta, Georgia**
Master of Science in Electrical and Computer Engineering *May 2020*

- Thesis on Investigating Opportunities and Challenges in Modeling and Designing Scale-Out DNN Accelerators
- Relevant Coursework: Probabilistic Graphical Machine Learning | Statistical Machine Learning | Advanced Computer Architecture | Interconnection Networks | Embedded Systems | Robotics & Perception | Data Structures & Algorithms

Bachelor of Science in Computer Engineering *December 2019*

- Minor in Robotics from the College of Engineering
- Shenzhen University Study Abroad in Shenzhen, China & Hong Kong

WORK EXPERIENCE

GEORGIA INSTITUTE OF TECHNOLOGY **Atlanta, Georgia**
Researcher in Synergy Computer Architecture Lab *January 2019 – Present*

- Designing hardware accelerators akin to Google TPU using advanced data structures to improve deep learning processes
- Developed programs in Verilog, C (CUDA), & Python to model advanced hardware systems and analyze tradeoffs
- Synthesized RTL and created place & route in Cadence to model ASIC hardware and generate energy, chip area estimates

INTEL CORPORATION **Folsom, California**
Firmware Engineering Intern *May 2019 – August 2019*

- Implemented new logging mechanisms in C/C++ for firmware analysis and debugging during various drive states
- Developed firmware on a virtual emulation platform in a Linux environment using VSCode editor and real-time debugger
- Designed and implemented firmware that functions with an RTOS on an ARM processor system

INTEL CORPORATION **Folsom, California**
Firmware Validation Engineering Intern *May 2018 – December 2018*

- Managed FPGA platforms used for debugging firmware designed for future Intel Optane SSDs
- Gained a strong understanding of the architecture and firmware development in C/C++ of next generation SSDs
- Created validation scripts and templates using Python to test firmware functionality and place tests through integration
- Actively engaged in team communication and failure reporting utilizing Agile Software Development Tools

NORFOLK SOUTHERN (NS) CORPORATION **Atlanta, Georgia**
Software Engineering Intern *May 2017 – August 2017*
One of the nation's premier transportation companies, operating railways in 22 states and the District of Columbia.

- Developed and debugged web applications for track railroad maintenance in MVC ASP.NET
- Created Work Reports using SQL Server Reporting Services in a Microsoft VS environment
- Traveled to NS Train Yards to learn about daily inspections, engineering, and conductor duties

PROJECTS

GEORGIA INSTITUTE OF TECHNOLOGY **Atlanta, Georgia**
SCALE-Sim: Cycle Accurate Simulator for DNN Accelerators *August 2019 – May 2020*

- Key conclusion that bandwidth is limiting factor in accelerator design
- Tool redesign to modular, faster logic and features added to open-sourced GitHub repository

Atlanta, Georgia
SIGMA: GEMM Accelerator with Flexible Interconnects for DNN Training *January 2019 – May 2019*

- Best Paper Award at HPCA 2020
- Verilog implementation of Flex-DPE architecture fundamental building blocks

GEORGIA INSTITUTE OF TECHNOLOGY **Atlanta, Georgia**
Vie-Vu IoT Device: Cyber Security Project Member *August 2017 – December 2017*

- Examined cyber security vulnerabilities in a body worn camera IoT device
- Programmed scripts to parse signal data into readable text using Python
- Altered the device firmware using protocols on serial line communication using Linux kernel

SKILLS / INTERESTS

Programming: C++, C, Java, Python, C#, Verilog, VHDL, JavaScript, MATLAB, SQL, HTML, Linux Bash
Hardware: RTL Design, ECAD Tools (Cadence Place & Route, Synopsys Synthesis), Embedded Digital Design