

**PRAKSHI RASTOGI**

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**OBJECTIVE:**

Seeking full-time opportunities in Digital VLSI and Computer Architecture starting from Jan 2018

**EDUCATION:**

**MS in Electrical and Computer Engineering | GPA: 3.8/4.0**

Georgia Institute of Technology, Atlanta GA

Aug'16- Dec'17

*Relevant Courses: Advanced VLSI, Advanced Computer Architecture, Physical Design & Automation, Digital Systems Test Nanometer Nodes, Digital Design with Verilog, Gigascale Integration, Advanced Programming Techniques, IC Fabrication*

**B.Tech Electrical and Electronics | CGPA: 3.65/4(University Silver Medal)**

University of Petroleum and Energy Studies, India

Jun'11-May'15

**SKILLS:**

**Programming:** C++, Perl, Python, Verilog, Assembly language(x86/ MIPS), Shell scripting, VHDL

**Software:** Cadence Virtuoso, Cadence Encounter, Cadence Conformal LEC, HSpice, Modelsim-Altera, Xilinx, Keil, Suprem, Linux, Synopsys Primetime, Synopsys IC Compiler, Synopsys DC Compiler

**PROFESSIONAL EXPERIENCE:**

**Intel Corporation, Fort Collins, USA: Physical Design Intern, Hardware**

May' 17-Aug' 17

- Implemented Physical Design flow(Synthesis and apr) using Synopsys tools and automated the flow
- Single handedly implemented Formal Equivalence and Verification on an entire phase of project using Cadence Conformal LEC (**Got a rating of EE(Exceeding Expectation)** which only 5-10% of interns get)
- Worked on the Static Timing Analysis and devised solutions to meet timing criteria
- Built scripts in Perl and Shell to automate the flow and created a centralized webpage for automation

**Infosys Limited, India: Technical Intern**

Dec '15-Mar'16

- Worked as a Trainee and developed scripts in python, dotnet, sql and developed an online Graphic user interface for bus ticket login.

**Moser Baer Private Limited, India: Technical Intern**

May'14-Jul'14

- Worked for the establishment of solar charging stations in LWE areas by the Govt.
- Assisted the Technical Head, 'J.S. Dhaka' with the data analysis of the CD and the solar plant and manufactured CD's and DVD's in clean room.

**RoboSapiens Technology Private Limited, India: Technical Intern**

May '13-Jul'13

- Worked on the principles of Advance Robotics, embedded systems and developed an edge controlled Bot and coded in embedded C to achieve this.

**PROJECTS:**

**Reconfigurable Architecture for Machine Learning Acceleration**

Fall '17

- Increasing the performance of Deep Neural Networks/Convolutional Neural Networks by using VLSI architecture and performing the layouts of the architecture

**Design and Implementation of a 45nm 6-T SRAM and Arithmetic Unit: Advanced VLSI**

Fall '16

- Implemented a pipelined system of a 64 byte 6T SRAM, circuit to drive a 150fF capacitive interconnect in Cadence Virtuoso
- Designed an SRAM which takes an input and then adds it to the previous input sequentially which is Driven by long interconnect. Reduced the power consumption to 14%
- Designed row and column decoders, Sense Amplifier and implemented the layout of Sram and optimized Energy Delay product. Optimized the delay of the long Interconnects

**Implementation of Bounded PRIM and BRBC routing algorithms using C++: Physical Design & Automation**

Fall '16

- Implemented BPRIM and BRBC algorithms using C++
- Developing a model that efficiently routes the entire circuit by decreasing both its wirelength and cost at the same time. Developed a new Algorithm that reduced the radius upto 35.2%.

**Analysis of assist techniques and variability on different topologies of CMOS and FinFET SRAM** Spring '17

- Analyzed the Read, Write and Hold margin in 6T, 8T, 10T Sram cells for both Cmos and Finfet(Cadence).
- Developed Netlists(in Hspice) for Cmos and Finfet Sram and accounted the impact of process variation on read and write margin(Monte Carlo Simulation) and compared the two.
- Proposed new assist technique that increases the data retention voltage by 4% and decreases the Operating voltage by 10.3% thus decreasing the power consumption and operating at lower voltage

**Implementation of Mandelbrot Set using opengl: Advance Prog. Techniques** Spring'17

- Used OpenGL graphics API, C++ pthreads to compute and display a visual image (512x512) of Mandelbrot Set.
- Used the mouse to select a square region from the displayed set, and recomputed the set using only the selected region of the complex plane

**Parallel Programming Paradigms using PThreads and MPI Protocol** Spring'17

- Implemented 2D DFT Algorithm using Message Passing Interface (MPI) for inter process communication
- Implemented 2D FFT using pthreads employing conditional wait, mutexes and barriers

**Logic and Fault Simulator Circuit** Fall' 16

- Developed a logic simulator in python which detects the values of all the nodes and then formulating a fault simulator which detects the stuck at faults in the circuit covering 100% fault coverage.

**Image processing, conversion of Bitmap Image to VGA, transposing and Edge detection using Sobel Edge Detection using Verilog** Spring' 17

- Implemented the conversion of bitmap file to Vga in Verilog and transposed the image and implemented sobel edge detection in it by using Verilog

**Online Booking Portal (Infosys Limited)** Jan'16-Feb'16

- Developed a GUI for online booking portal in python
- Implemented various user profile features like data handling and entry constraints.

**CERTIFICATIONS:**

Adesh Kumar, Prakshi Rastogi, Pragyana Srivastava," Design and FPGA Implementation of DWT, Image Text Extraction Technique", Procedia Computer Science 57 (2015) 1015 – 1025

**LEADERSHIP/ACTIVITIES**

- Awarded with an EE (Exceeding Expectations) rating from Intel for my Summer 2017 Internship which about 5-10% of Interns get.
- University Silver Medal holder for being Ranked One in the Electronics branch among 60 students
- Awarded the 'Most Helping Student' in a class of 240 students.