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DEPARTMENT OF DEFENSE

Department of Army

Notice of Intent to seek Partners for a Cooperative Research and Development Agreement and Licensing Opportunity for Operating System (OS) Friendly Microprocessor Architecture invented and patent pending by U.S. Army Aviation and Missile Command

AGENCY: Department of Army, DoD.

ACTION: Notice of Intent Seeking Partners.

SUMMARY: The U.S. Army Aviation and Missile Command (AMRDEC) is seeking Cooperative Research and Development Agreement (CRADA) partners to collaborate in transitioning OS Friendly Microprocessor Architecture (OSFA) into commercial and/or government application(s). OSFA references approved for public release are provided [1-2]. Interested potential CRADA collaborators will receive detailed information on the current status of the project after signing a confidentiality disclosure agreement (CDA) with AMRDEC. Guidelines for the preparation of a full CRADA proposal will be communicated shortly thereafter to all respondents with whom initial confidential discussions will have established sufficient mutual interest. CRADA applications submitted after the due date may be considered if a suitable CRADA collaborator has not been identified by AMRDEC among the initial pool of respondents. Licensing of background

technology related to this CRADA opportunity is also available to potential collaborators.

DATES: Interested candidate partners must submit a statement of interest and capability to the AMRDEC point of contact before April 10, 2015 for consideration.

ADDRESSES: Comments and questions may be submitted to: Department of Army, US Army Research, Development and Engineering Command, Aviation and Missile Research, Development, and Engineering Center, ATTN: RDMR-CST, Office of Research and Technology Applications (Ms. Wallace), 5400 Fowler Road, Redstone Arsenal, AL 35898.

FOR FURTHER INFORMATION CONTACT: Questions about the proposed action can be directed to Ms. Cindy Wallace (256) 313-0895, Office of Research and Technology Applications, email: *cindy.s.wallace.civ@mail.mil*.

SUPPLEMENTARY INFORMATION:

1. **Project Description**. AMRDEC seeks to ensure that technologies developed by AMRDEC are expeditiously commercialized and brought to practical use. The purpose of a CRADA is to find partner(s) to facilitate the development and commercialization of a technology that is in an early phase of development. Respondents interested in submitting a CRADA proposal should be aware that it may be necessary for them to secure a patent license to the above-mentioned patent pending technology in order to be able to commercialize products arising from a CRADA. CRADA partners are afforded an option to

negotiate an exclusive license from the AMRDEC for inventions arising from the performance of the CRADA research plan.

2. Technology Overview: Conventional microprocessors have not tried to balance hardware performance and OS performance at the same time. The goal of the OS Friendly Architecture (OSFA) is to provide a high performance microprocessor and OS system. The architecture's cache memory banks provide for near instantaneous context switching and hardware based information assurance. The OS Friendly Microprocessor Architecture includes hardware permission bits for each cache bank and each memory address.

The OS Friendly Architecture is a switched set of cache memory banks in a pipeline configuration. For light-weight threads, the memory pipeline configuration provides near instantaneous context switching times. The pipelining and parallelism provided by the memory pipeline configuration provides for background cache read and write operations while the microprocessor's execution pipeline is running instructions. The cache bank selection controllers provide arbitration to prevent the memory pipeline and microprocessor's execution pipeline from accessing the same cache bank at the same time. This separation allows the cache memory pages to transfer to and from level 1 (L1) caching while the microprocessor pipeline is executing instructions.

OS information assurance is implemented in hardware. By extending Unix file permissions bits down to each cache memory bank and memory

address, the OSFA provides hardware level information assurance. OS level access to cache controller banks is divided into access layers. Only the OS has permission to access and modify permission bits. The OS access layers also support partitions for a high reliability microkernel, hypervisors and full featured OS.

For each software application, a table sets limits for all OS library function calls required by the application. Each library function call has a set of object limits. Exceeding the limits either requires higher than user level privileges or raises an exception.

The full CRADA proposal should include a capability statement with a detailed description of collaborators' expertise in the following and related technology areas: (1) microprocessor design; (2) computer security; (3) information assurance; (4) collaborators' expertise in successful technology transition; and (5) collaborator's ability to provide adequate funding to support some project studies is strongly encouraged. A preference will be given to collaborators who shall manufacture hardware in the United States.

Collaborators are encouraged to properly label any proprietary material in their CRADA proposal as PROPRIETARY. Do not use the phrase “company confidential.”

3. Publications. a. P. Jungwirth and P. LaFratta: "OS Friendly Microprocessor Architecture," US Patent Application 20140082298, March 2014. *http://www.google.com/patents/US20140082298.*

b. P. Jungwirth and P. LaFratta: "OS Friendly Microprocessor Architecture," white paper, US Army AMRDEC, March 2014. (email Ms. Wallace at cindy.s.wallace.civ@mail.mil to request a copy of this paper).

c. P. Jungwirth and P. LaFratta: "OS Friendly Microprocessor Architecture: Hardware Information Assurance," January 2014. (email Ms. Wallace at *cindy.s.wallace.civ@mail.mil* to request a copy of this paper, a CDA is required to receive a copy of this paper).

Brenda S. Bowen,
Army Federal Register Liaison Officer.

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