University of North Texas, College of Engineering

EENG 2710.005: Digital Logic Design

Spring 2026
Monday, Wednesday 10:00 – 11:20 AM
NTDP E266

Instructor

- Shahram Rohani, Email: shahram.rohani@unt.edu
  Office Hours (Room E245B): Mon/Wed 11:30 AM – 12:30 PM
- GA: Yoo Chul Park, Email: YooChulPark@my.unt.edu
  Office hours: (Room B250) Mon/Wed 1:00 – 2:30 PM

Check Canvas frequently for updated class information

Course Description

- Numbers and codes; switching theory; combinational logic circuits; modular design of combinational circuits; memory elements; sequential logic circuits; digital system design; fault models and testing.

Prerequisites

- Engineering or engineering technology majors

Corequisites

- EENG 2711 (which must be completed with a grade of C or better) for Electrical Engineering majors

Textbook and required material

- *Fundamentals of Logic Design*, Enhanced 7th Ed., C. H. Roth Jr., L. L. Kinney, and E. B. John, Cengage Learning, Inc., 2021. ISBN: 978-1-337-62035-2.

Additional material, as required, will be provided on Canvas.

Course Objectives

By the end of the course, you will

- **Know** *what* digital systems are, *how* they differ from analog systems and *why* it is advantageous to use the digital systems in *many applications*.
- **Comprehend** different number systems including the binary system and Boolean algebraic principles.
- **Apply** Boolean algebra to switching logic design and simplification.
- **Analyze** a given digital system and decompose it into logical blocks involving both *combinational* and *sequential circuit* elements.
- **Synthesize** a given system starting with problem requirements, identifying and designing the building blocks, and then integrating these blocks into a complete system.
- **Validate** the system functionality and evaluate the relative merits of different designs.

Course Topics:

- Number Systems and Digital Logic Gates
- Boolean Algebra, Switching Functions and Canonical Forms
- Combinational Circuit Minimization, Analysis, and Synthesis
- Sequential circuits elements and sequential logic circuits
- Modular Sequential Logic- Counters and shift registers
- Analysis and Design of synchronous sequential circuits

Course Requirements and General Policies

- The student is required to attend all scheduled lectures. Attendance will be taken for each class meeting. Lecture time will include vital activities such as taking quizzes and exams, problem solving, going over answers to questions in problem sets and quizzes, and reviews for exams. The student can be dropped from the course for three (3) unexcused absences in Lecture. An excused absence can only be guaranteed by obtaining, in advance, the instructor authorization. Please refer to https://policy.unt.edu/policy/06-039

- Please do not wait until the last minute. If you are having trouble with this class, please take advantage of the following support services:
  1. The Learning Center's Lead Tutors. You can access all of their services through their website: https://learningcenter.unt.edu/tutoring. They also have a video that overviews their services for the fall, including how to schedule an appointment! Here's the link: https://www.youtube.com/watch?v=HOggBsi3VME .
  2. The IEEE UNT Student Branch and IEEE-HKN Lambda Zeta Chapter will be hosting recitations for this course and a study hall. Details will be posted in the "Announcements" on Canvas.
  3. There will be a recitation host for this course who will be supporting students through homework review sessions held after each homework deadline. More detail will be posted in the "Announcements" on Canvas.
  4. Take advantage of the TA's office hours.

- The UNT Catalog procedures on cheating and plagiarism will be enforced. It is the duty of all students to protect their work so it is not available for others to represent as their own. This is especially true of files that are generated on the computer. Students who knowingly allow others to use their work are partners in this unethical behavior. For more details regarding the above policies and for your rights and responsibilities, please visit https://studentaffairs.unt.edu/dean-of-students/.

Assignments and Exams

- Homework will be assigned on a weekly basis and must be submitted by the due date and time and turned in at the beginning of the class period according to the instructions given each week. If you have an excused absence and are unable to come to class, you should email your assignment to me by the deadline. **Late homework will not be accepted.** Homework must follow the following guidelines; otherwise, it will be returned ungraded!

  1. Use standard 8 ½ x 11 paper (straight edge; no spiral)
  2. Number the pages and put them in order
  3. Staple the pages together
  4. Print your name, date, and the homework # on the top page
  5. Show your work clearly and highlight or circle your answers
  6. Place on the front desk as you enter the classroom before class begins

- There will be unannounced quizzes administered during the semester to evaluate understanding of relevant material. **No make-up quizzes will be given.**

- There will be **no extra credit**. There will be **no make-up quizzes or examinations** given unless prearranged with the instructor for a university approved excused absence. The final examination will be comprehensive over the entire semester's work.

- Exams will be based on text readings, handouts, class exercises, quizzes, class lectures and discussions. Students are responsible for all text material, regardless of whether we review the text material in class or not. **No make-up exams will be given.**

- Each student should retain graded lecture notes, quizzes, homework, tests, software-generated files, and laboratory reports to document errors in recorded grades.

- Requests for review of graded work must be emailed to the TA within a week of which such work is returned to the students. The instructor should be cc'd on this email. The request should be accompanied by a written justification of the request including any supporting data.

Disability Accommodation

UNT makes reasonable academic accommodation for students with disabilities. Students seeking accommodation must first register with the Office of Disability Accommodation (ODA) to verify their eligibility. If a disability is verified, the ODA will provide a student with an accommodation letter to be delivered to faculty to begin a private discussion regarding one's specific course needs. Students may request accommodations at any time, however, ODA notices of accommodation should be provided as early as possible in the semester to avoid any delay in implementation. Note that students must obtain a new letter of accommodation for every semester and must meet with each faculty member prior to implementation in each class. For additional information, please contact the Office of Disability Accommodation ODA website or at 940-565-4323.

Useful Links

- UNT Academic Calendar: https://registrar.unt.edu/registration/spring-registration-guide
- Office of the Registrar: http://essc.unt.edu/registrar (schedule of classes and exams, etc.)
- Eagle Student Services Center: https://studentaffairs.unt.edu/index.html

Grading Policies

- Homework 20%
- Quizzes 20%
- Midterm Exam 30%
- Final Exam 30%
- Final accumulated number score is on a 100-point scale.

Grade Distribution

90.0% - 100%	A
80.0% - 89.9%	B
70.0% - 79.9%	C
60.0% - 69.9%	D
59.9% & Below	F

Course Outline and Tentative Schedule

You can find the lectures slides and problem assignments in Canvas.

Week	Topic	Reading Assignment
1,2	Course Introduction – Number Systems and Conversion – Binary Arithmetic	1.1 – 1.3
2,3	Negative Numbers – Binary Codes – Boolean Algebra	1.4 – 1.5, 2.1 – 2.5
4	Laws of Boolean Algebra – SOP & POS Forms & Simplification	2.6 – 2.8, 3.1 – 3.5
5	Minterms/Maxterms & Applications of Boolean Algebra – Truth Tables and Incomplete Functions Two, Three, and Four-variable Karnaugh Maps	4.1 – 4.7, 5.1 – 5.3
5,6	Karnaugh Maps – Prime Implicants	5.1 – 5.7
7	Quine-McCluskey method	6.1 – 6.6
7,8	Multi-Level Gate Circuits – NAND and NOR Gates	7.1 – 7.7
8	Midterm Exam	
Mar 9&11	Spring Break – No Class	
9	Combinational Circuit Design, Gate Delays, Timing Diagrams, and Hazards	8.1 – 8.4
10	Multiplexers, Buffers, Decoders, Encoders, and ROMs	9.1 – 9.5
11	Latches and Flip-Flops – Registers and Counters (1)	11.1–11.10, 12.1 – 12.3
12	Registers and Counters (2) – Analysis of Clocked Sequential Circuits	12.4 – 12.6, 13.1 – 13.4
13	Derivation of State Graphs and Tables	14.1 – 14.6
14	Reduction of State Tables State Assignment (1)	15.1 – 15.6
15	Reduction of State Tables State Assignment (2) – Sequential Circuit Design; Final exam review	15.7 – 15.9, 16.1 – 16.3
16	Final Exam Saturday, May 2nd 7:30 – 9:30 AM https://registrar.unt.edu/exams/final-exam-schedule/spring	

Note: *This course outline is subject to change based on class progress.*

Reading Requirements:

The students are required to come prepared to every class with the material discussed in the previous class.

Class Evaluation by Students

The SPOT (Student Perceptions of Teaching) evaluation is a requirement for all organized classes at UNT and is available for your input at the end of the semester.

Course Learning Outcomes (CLOs)

Course Learning Outcomes (CLOs), that is, the areas for student learning in this course are:

[CLO-1] Digital and Analog Systems: Basic Concepts and Historical Perspective
[CLO-2] Number Systems and Digital Logic Gates
[CLO-3] Boolean Algebra, Switching Functions and Canonical Forms
[CLO-4] Combinational Circuit Minimization, Analysis, and Synthesis
[CLO-5] Sequential circuits elements and sequential logic circuits
[CLO-6] Modular Sequential Logic- Counters and shift registers
[CLO-7] Analysis and Design of asynchronous sequential circuits

Our EE Program Outcomes (POs)

Upon completion of our BSEE program, the students will be able to:

[PO-1] Apply knowledge of mathematics, engineering and science.

[PO-2] Design and conduct experiments to verify and validate the design projects developed by them and analyze and interpret data.

[PO-3] Develop project-based learning skills through design and implementation of a system, component, or process that meets the needs within realistic constraints.

[PO-4] Function on multidisciplinary teams.

[PO-5] Identify, formulate, and solve engineering problems.

[PO-6] Have an understanding of professional and ethical responsibility.

[PO-7] Communicate effectively.

[PO-8] Achieve broad education necessary to understand the impact of electrical engineering solutions in a global and societal context.

[PO-9] Understand learning processes, concepts of learning to learn, and engage in lifelong learning.

[PO-10] Achieve knowledge of contemporary issues.

[PO-11] Use techniques, skills, and computer-based tools for conducting experiments and carrying out designs.

[PO-12] Develop an appreciation for principles of business practices and entrepreneurship.

ABET Outcomes

3a- an ability to apply knowledge of mathematics, science, and engineering

3b- an ability to design and conduct experiments, as well as to analyze and interpret data

3c- an ability to design a system, component, or process to meet desired needs

3d- an ability to function on multi-disciplinary teams

3e- an ability to identify, formulate, and solve engineering problems

3f- an understanding of professional and ethical responsibility

3g- an ability to communicate effectively

3h- the broad education necessary to understand the impact of engineering solutions in a global and societal context

3i- a recognition of the need for, and an ability to engage in life-long learning

3j- a knowledge of contemporary issues

3k- an ability to use the techniques, skills, and modern engineering tools necessary for engineering practice

Relationship between the Course Learning Outcomes and Program/ABET Outcomes

The course learning outcomes map onto the program and ABET outcomes as depicted in the table below.

CLO	**Student/ABET Criterion 3 Outcomes**						
	SO-1/3 [1]	SO-2/3 [2]	SO-3/3 [3]	SO-4/3 [4]	SO-5/3 [5]	SO-6/3 [6]	SO-7/3 [7]
1	X						X
2	X						X
3	X						X
4	X						X
5	X						X
6	X						X
7	X						X