Syllabus

Course: EENG 2710 Digital Logic Design 3 Credits

Text: Fundamentals of Logic Design Seventh Edition by Charles H. Roth, Jr.

Hours: MW 1:50 – 3:10 PM K120

Instructor: John Polson, Ph.D. john.polson@unt.edu

Office Hours: Before and After class. Other times by zoom appointment (not on exam days)

Grades:				
	90	-	100	A
	80	-	89	B
	70	-	79	C
	60	-	69	D
	0	-	59	F

Your grade is based on 4 exams (20% each), homework and quizzes (20%). Any scaling or curving of grades is done at the end of the semester (unlikely). Instructor's assessment of professional conduct may move score +/- 5%. The schedule is on the back side of this syllabus and is subject to change. Watch Canvas AND e-mail.

If your Exam 4 score is higher than the lowest score from your first three exams, your Exam 4 score replaces the lowest score. However, if your Exam 4 is the lowest score, all count equally. Exam 4 replaces any missed exam; there are NO MAKEUP EXAMS. If you miss two exams, the second records as zero. Assigned seating for exams.

Homework: You should work and understand every assigned problem and more. Follow homework submission standards. Each problem (or section of a problem) has equal weight and is graded 10 points for correct answer, 5 points for incorrect answer, and 0 points for missing problem. Homework is not accepted late. Homework is due via Canvas midnight Thursdays.

Quizzes: Submit for 1 point (~0.05% of grade each) by 5:00 PM via Canvas. They are exam prep & attendance (name alone gets that point). See the HW schedule for when to submit the worked quizzes for points.

Academic Dishonesty: You are expected to follow the guidelines in the student handbook.

Submission Standards (5% penalty for not following standard)

1. ***PRINT*** your name and student number on every page (Last, First).
2. Start each problem on a new sheet of paper.
3. **Work in soft pencil and neatly erase any corrections.**
4. Work neatly down the paper in a single column.
5. Double underline your answer.
6. Number pages in the upper right hand corner A/B. Where: A is current out of total B (for this problem).
7. Upload a single file in the following format.

EENG2710	Due Date (A Thursday)	Last, First Student Number	Assignment #	A/B
	Problem Number. Given: (Single line drawn with a straight edge separates Given from Required).			
	Required: (Single line drawn with a straight edge separates Required from Solution).			
	Solution: Double Underline your Answer! Make it neat and easy to grade!!!			

Monday, August 17, 2026	Classes Begin	Event
Monday, August 17, 2026	Meet 1	Syllabus, Chapt 1: Base Conv.
Wednesday, August 19, 2026	Meet 2	Chapt 1: Arithmetic & Neg #s
Saturday, August 22, 2026	HW01	1.1a, 1.2a, 1.3, 1.5a (all bases valid on exam), Q01, Q02
Monday, August 24, 2026	Meet 3	Chapt 2: Def & Thms
Wednesday, August 26, 2026	Meet 4	Chapt 3: Use Thms
Saturday, August 29, 2026	HW02	2.3a-f, 2.7a, 2.9b, 3.25a, 3.35, Q03, Q04
Monday, August 31, 2026	Meet 5	Chapt 4: 6+1 Forms
Wednesday, September 2, 2026	Meet 6	Review
Monday, September 7, 2026		Labor Day - No Classes - University Closed
Wednesday, September 9, 2026	Meet 7	Exam 1
Monday, September 14, 2026	Meet 8	Ch 5: K-Map Pt 1
Wednesday, September 16, 2026	Meet 9	K-Map Pt 2: VEM, Quine McCluskey
Saturday, September 19, 2026	HW03	5.3a, 5.4a-b, 5.7a&c, Q05, Q06, Q07, Q08
Monday, September 21, 2026	Meet 10	Chapter 7 Parts, multi-level ckts
Wednesday, September 23, 2026	Meet 11	Chapter 7 Parts... (IEEE symbols)
Saturday, September 26, 2026	HW04	7.1a, 7.2a, 7.8a-b, Q09, Q10
Monday, September 28, 2026	Meet 12	Chapt. 8: delay, fan in/out, hazzards
Wednesday, September 30, 2026	Meet 13	Chapt. 9: MUX
Saturday, October 3, 2026	HW05	8.1, 8.3, 8.12, Q11, Q12
Monday, October 5, 2026	Meet 14	Review
Wednesday, October 7, 2026	Meet 15	Exam 2
Monday, October 12, 2026	Meet 16	FPGAs
Wednesday, October 14, 2026	Meet 17	Latches and Flip Flops
Saturday, October 17, 2026	HW06	11.2a-c, 11.3, Q13, Q14, Q15
Monday, October 19, 2026	Meet 18	SR, JK Latch, Flip Flops + debounce
Wednesday, October 21, 2026	Meet 19	Registers, Shift Reg, and Counters
Saturday, October 24, 2026	HW07	12.6, Q16, Q17
Monday, October 26, 2026	Meet 20	LFSR
Wednesday, October 28, 2026	Meet 21	Timing Diagrams, FPGA, MUX
Saturday, October 31, 2026	HW08	13.2, Q18, Q19
Monday, November 2, 2026	Meet 22	State Machines
Wednesday, November 4, 2026	Meet 23	Exam 3
Friday, November 6, 2026		Last day to drop with a grade of W
Monday, November 9, 2026	Meet 24	Regular Expressions
Wednesday, November 11, 2026	Meet 25	Next State Table, Output Tbl -> Ckt
Saturday, November 14, 2026	HW09	14.4, 14.5, Q20, Q21, Q22
Monday, November 16, 2026	Meet 26	Identical States
Wednesday, November 18, 2026	Meet 27	State Variable Assignments & Opts.
Saturday, November 21, 2026	HW10	15.1a-b, 15.3, 16.23a&c, Q23, Q24
Monday, November 23, 2026		Thanksgiving - No class November 23-29, 2026
Monday, November 30, 2026	Meet 28	Work last quiz in class summary
Wednesday, December 2, 2026	Meet 29	Exam 4
	Meet 30	Class Cancelled