Syllabus

Course: EENG 2710 Digital Logic Design 3 Credits

Text: Fundamentals of Logic Design Seventh Edition by Charles H. Roth, Jr.

Hours: MW 8:30 – 9:50 AM

Instructor: John Polson, Ph.D. john.polson@unt.edu

Office Hours: Before and After class. Other times by zoom appointment (not on exam days)

Grades:

90	-	100	A
80	-	89	B
70	-	79	C
60	-	69	D
0	-	59	F

Your grade is based on 4 exams (20% each), homework and quizzes (20%). Any scaling or curving of grades is done at the end of the semester (unlikely). Instructor's assessment of professional conduct may move score +/- 5%. The schedule is on the back side of this syllabus and is subject to change. Watch Canvas AND e-mail.

If your Exam 4 score is higher than the lowest score from your first three exams, your Exam 4 score replaces the lowest score. However, if your Exam 4 is the lowest score, all count equally. Exam 4 replaces any missed exam; there are NO MAKEUP EXAMS. If you miss two exams, the second records as zero. Assigned seating for exams.

Homework: You should work and understand every assigned problem and more. Follow homework submission standards. Each problem (or section of a problem) has equal weight and is graded 10 points for correct answer, 5 points for incorrect answer, and 0 points for missing problem. Homework is not accepted late. Homework is due via Canvas midnight Thursdays.

Quizzes: Submit for 1 point (~0.05% of grade each) by 10:00 AM via Canvas. They are exam prep & attendance.

Academic Dishonesty: You are expected to follow the guidelines in the student handbook.

Submission Standards (5% penalty for not following standard)

1. ***PRINT*** your name and student number on every page (Last, First).
2. Start each problem on a new sheet of paper.
3. **Work in soft pencil and neatly erase any corrections.**
4. Work neatly down the paper in a single column.
5. Double underline your answer.
6. Number pages in the upper right hand corner A/B. Where: A is current out of total B (for this problem).
7. Upload a single file in the following format.

EENG2710	Due Date (A Thursday)	Last, First Student Number	Assignment #	A/B
	Problem Number. Given: (Single line drawn with a straight edge separates Given from Required).			
	Required: (Single line drawn with a straight edge separates Required from Solution).			
	Solution: Double Underline your Answer! Make it neat and easy to grade!!!			

Class #	Date	Topic / Notes / Description	Nom. Part of Grade
1	Monday, January 12, 2026	Syllabus, Chapt 1: Base Conv.	0.05%
2	Wednesday, January 14, 2026	Class Cancelled	
	Friday, January 16, 2026	Drop / Add / Switch Day	
	Monday, January 19, 2026	Martin Luther King Jr. Holiday	
3	Wednesday, January 21, 2026	Chapt 1: Arithmetic & Neg #s	0.05%
	Thursday, January 22, 2026	**HW 1 Due (40 pts)** 1.1a, 1.2a, 1.3, 1.5a (all bases valid on exam)	1.98%
4	Monday, January 26, 2026	Chapt 2: Def & Thms	0.05%
5	Wednesday, January 28, 2026	Chapt 3: Use Thms	0.05%
	Thursday, January 29, 2026	**HW 2 Due (100 pts)** 2.3a-f, 2.7a, 2.9b, 3.25a, 3.35	4.95%
6	Monday, February 2, 2026	Chapt 4: 6+1 Forms	0.05%
7	***Wednesday, February 4, 2026***	***EXAM 1***	20.00%
8	Monday, February 9, 2026	Ch 5: K-Map Pt 1	0.05%
9	Wednesday, February 11, 2026	K-Map Pt 2: VEM, Quine McCluskey	0.05%
	Thursday, February 12, 2026	**HW 3 Due (50 pts)** 5.3a, 5.4a-b, 5.7a&c	2.48%
10	Monday, February 16, 2026	Chapter 7 Parts, multi-level ckts	0.05%
11	Wednesday, February 18, 2026	Chapter 7 Parts... (IEEE symbols)	0.05%
	Thursday, February 19, 2026	**HW 4 Due (40 pts)** 7.1a, 7.2a, 7.8a-b	1.98%
12	Monday, February 23, 2026	Chapt. 8: delay, fan in/out, hazzards	0.05%
13	Wednesday, February 25, 2026	Chapt. 9: MUX	0.05%
	Thursday, February 26, 2026	**HW 5 Due (30 pts)** 8.1, 8.3, 8.12	1.49%
14	Monday, March 2, 2026	Review	0.05%
15	***Wednesday, March 4, 2026***	***EXAM 2***	20.00%
	Monday, March 9, 2026	Spring Break	
	Wednesday, March 11, 2026	Spring Break	
16	Monday, March 16, 2026	FPGAs	0.05%
17	Wednesday, March 18, 2026	Latches and Flip Flops	0.05%
	Thursday, March 19, 2026	**HW 6 Due (40 pts)** 11.2a-c, 11.3	1.98%
18	Monday, March 23, 2026	SR, JK Latch, Flip Flops + debounce	0.05%
19	Wednesday, March 25, 2026	Registers, Shift Reg, and Counters	0.05%
	Thursday, March 26, 2026	**HW 7 Due (10 pts)** 12.6	0.50%
20	Monday, March 30, 2026	LFSR	0.05%
21	Wednesday, April 1, 2026	Timing Diagrams, FPGA, MUX	0.05%
	Thursday, April 2, 2026	**HW 8 Due (10 pts)** 13.2	0.50%
22	Monday, April 6, 2026	State Machines	0.05%
23	***Wednesday, April 8, 2026***	***EXAM 3***	20.00%
24	Monday, April 13, 2026	Regular Expressions	0.05%
25	Wednesday, April 15, 2026	Next State Table, Output Tbl -> Ckt	0.05%
	Thursday, April 16, 2026	**HW 9 Due (20 pts)** 14.4, 14.5	0.99%
26	Monday, April 20, 2026	Identical States	0.05%
27	Wednesday, April 22, 2026	State Variable Assignments & Opts.	0.05%
	Thursday, April 23, 2026	**HW 10 Due (40 pts)** 15.1a-b, 15.3, 16.23a&c	1.98%
28	Monday, April 27, 2026	Work last quiz in class summary	0.05%
29	***Wednesday, April 29, 2026***	***EXAM 4***	20.00%