University of North Texas
Department of Electrical Engineering
EENG 2910 Digital System Design
Spring 2014

Instructor: Ike Agbor
E-mail: ike.agbor@unt.edu
Class Hours: Wed. 2:30 PM - 5:20 PM
Office: NTDP B252
Office Hours: Tue. & Thurs. 2:30 PM – 4:30 PM or by appointment

Course Description:

Digital system design projects provide students substantial experience in logic analysis, design, logic synthesis in VHDL, and testing. Project documentation including all the phases of project cycle from requirement analysis to testing as well as a project presentation providing the students an opportunity to enhance their communication and presentation skills are essential components of this course.

Prerequisite: Digital Logic Design (EENG 2710)

Reference Textbooks:

- Fundamentals of Digital Logic with VHDL Design, 2nd Ed., Stephen Brown and Zvonko Vranesic, McGraw Hill Science/Engineering/Math, 2004, ISBN: 0072499389.
- FPGA Prototyping by VHDL Examples, 1st Ed., Pong P. Chu, John Wiley & Sons, ISBN: 9780470185315
- Logic and Computer Design Fundamentals, 4th Ed., Mano and Kime, Prentice Hall, ISBN-13: 9780131989269

Learning Outcomes:

Student will:

1. Demonstrate an understanding of project life-cycle through semester-long hands-on projects.
2. Design complex digital systems that comprises of combinational and sequential circuits starting from a word description that performs a set of specified tasks and functions.
3. Demonstrate project Planning and scheduling skills.
4. Develop skills, techniques and learn state-of-the-art engineering tools (such as Xilinx tools, VHDL) to design, implement and test modern-day digital systems on FPGAs.
5. Design control units as a state machine for complex systems.
6. Analyze the results of logic and timing simulations and to use these simulation results to debug digital systems.

7. Design, construct and test digital systems on breadboard.
8. Research design ideas and collect reference material that relates to their projects.
9. Defend their projects orally with good presentation skills.
10. Thoroughly document all phases of their project.
11. Understand engineering design and the steps involved and carry out engineering design principles in the design of a processor.
12. Demonstrate an understanding of ethical and professional issues as related to their projects.

General Policy:

- A perfect attendance is recommended for those aspiring to get good grades because there will be constant evaluation of skills.
- It is the responsibility of the students with certified disabilities to provide the instructor with appropriate documentation from the Dean of Students Office (see http://www.unt.edu/oda).
- Please visit http://www.unt.edu/csrr/ for your rights and responsibilities.

SETE Evaluations:

The Student Evaluation of Teaching Effectiveness (SETE) is a requirement for all organized classes at UNT. This short survey will be made available to you at the end of the semester, providing you a chance to comment on how this class is taught. I am very interested in the feedback I get from students, as I work to continually improve my teaching. I consider the SETE to be an important part of your participation in this class. Fall 2013 administration of the SETE will remain open through the week of finals.

Grading Policy:

Mid-term: 20,
Design Projects in VHDL: 80 (VHDL Skills: 15 + Design & Test Skills: 50 + Documentation & Defense: 15).

Topics (Tentative):

Week	Topic
1,2	Introduction to Digital system Design, VHDL and Nexys2 Board, Project
3	Combinational Logic Design
4	Sequential Logic Design
5	State Machine Design
6	Midterm

7	System design with emphasis on modularity
8	I/O Modules – UART, SRAM, VGA, Keyboard, and Mouse
9-13	Project
14	Project Presentation