Digital Logic Design (EENG 2710) Fall-2012

Instructor: Ikechukwu (Ike) Agbor
Faculty Office: **NTRP B-252**
Phone: **940-891-6874**
Email: **ike.agbor@unt.edu**

Class Hours: **T/TH 11:00 AM - 12:20 PM**
Class Room: **NTRP B-242.**
Office Hours: **M 11:0 0 PM-1:00 PM.** ***Students unable to see me during these times may request an appointment.***
Prerequisite: **Math 1720**

Text Book

1. Digital Logic Circuit Analysis & Design, 1st Ed. V. P. Nelson, H. T. Nagle, J. D. Irwin, and B. D. Carroll, Prentice Hall, 1995. ISBN: 0-13-463894-8.

Attendance Policy:

As a consequence of the continuous evaluation strategy adopted by the instructor, perfect attendance is recommended for those aspiring to get good grades.

Grading Policy:

Quizzes: 5%: Be aware that a quiz may be administered at the beginning, middle or end of a class session. It is your responsibility to be present during a quiz as there is no make-up for a missed quiz. The lowest score of the quiz may be dropped for the purposes of calculating your final grade.

Homework: 15%: Late homework is accepted, but with a 10% deduction per day until the solution is handed (usually one week after the due date of the homework). If you turn in your homework after the solution is distributed, you will not receive any credit. Your lowest homework score may also be dropped.

Two Middle Exams: 25% each: Make up exams will be possible only with a doctor's letter or letter of absence for a school-sponsored event. Were you to have a serious reason for missing an exam, you must contact me before the scheduled exam period to notify me that you cannot take the exam and provide accompanying documentation.

Final Exam: 30%: The final exam is comprehensive

• Final letter grade distribution: A=100-90, B=80-89, C=70-79, D=60-69, F=0-59

Academic Dishonesty:

Honesty is the best policy. Cheating will not be tolerated. Anyone found guilty of cheating on a test or assignment will be awarded an F grade for the course. Discussions of problems and assignment with your classmates is welcome and encouraged, however, sharing of solutions is not. If you need help, you should ask the instructor. Cheating includes, but is not limited to, all forms of plagiarism and misrepresentation. For your rights and responsibilities please refer to http://www.unt.edu/csrr

Statement regarding Disabled Students:

The Faculty of Electrical Engineering including this instructor cooperates with the Office of Disability Accommodation (ODA) to make reasonable accommodations for students with certified disabilities (cf. Americans with Disabilities Act and Section 504, Rehabilitation Act). If you have not registered with ODA, we encourage you to do so immediately and present a written accommodation request along with an appropriate documentation from the Dean of Students Office http://www.unt.edu/oda/, on or before the 2nd week of class.

Final Exam Date and Time: TBD.

Course Outline and Delivery Plan

Topic No.	Topic	Time Allocated
1.	Digital and analog systems- an introduction, historical perspective, importance of L2L and PBL	1 Week

2.	Number systems and codes	1 Week
3.	Boolean Algebra, Switching functions and canonical forms	2 Weeks
4.	Circuit minimization, Analysis of combinational circuits, and Timing issues	1.5 Weeks
5.	Top-down Modular Design of Combinational Logic	1.5 Weeks
6.	Sequential Circuit Elements- Latches and flip-flops	1 Week
7.	Modular Sequential Logic- Counters and shift registers	1 Week
8.	Analysis and Design of synchronous sequential circuits	1 Week
9.	Analysis and Design of asynchronous sequential circuits	3 Weeks
10.	Digital Logic Testing	1 Week

Note: The topics 1-10 listed above correspond to the chapters of the recommended reference book.

Reading Requirements

The students are required to come prepared to every class with the material discussed in the previous class.

Course Objectives

The main objectives of the course are to facilitate the students to achieve the highest levels in the Bloom's 6-level Learning Taxonomy so that they, at the end of the course, will be able to-

1. **Know** *what* the digital systems are, *how* they differ from analog systems and *why* it is advantageous to use the digital systems in *many applications*.
2. **Comprehend** different number systems including the binary system and Boolean algebraic principles
3. **Apply** Boolean algebra to switching logic design and simplification.
4. **Analyze** a given digital system and decompose it into logical blocks involving both *combinational* and *sequential circuit* elements.
5. **Synthesize** a given system starting with problem requirements, identifying and designing the building blocks, and then integrating blocks designed earlier

6. **Validate** the system functionality and evaluate the relative merits of different designs.

Course Learning Outcomes (CLOs)

Course Learning Outcomes (CLOs), that is, the areas for student learning in this course are:

[CLO-1] Digital and Analog Systems: Basic Concepts and Historical Perspective
[CLO-2] Importance of Learning to Learn (L2L) and Project-Based Learning (PBL) in learning Digital Logic Design.
[CLO-3] Number Systems and Digital Logic Gates
[CLO-4] Boolean Algebra, Switching Functions and Canonical Forms
[CLO-5] Combinational Circuit Minimization, Analysis, and Synthesis
[CLO-6] Sequential circuits elements and sequential logic circuits
[CLO-7] Modular Sequential Logic- Counters and shift registers
[CLO-8] Minimal Design of Synchronous Sequential Circuits
[CLO-9] Analysis and Design of asynchronous sequential circuits
[CLO-10] Digital Logic Testing
[CLO-11] Project-based Learning (PBL) - Digital Project execution from requirements through design and testing
[CLO-12] Project Report Writing

Our EE Program Outcomes (POs)

Upon completion of the BSEE program, the students will be able to:

[PO-1] Apply knowledge of mathematics, engineering and science.

[PO-2] Design and conduct experiments to verify and validate the design projects developed by them, and analyze and interpret data.

[PO-3] Develop project-based learning skills through design and implementation of a system, component, or process that meets the needs within realistic constraints.

[PO-4] Function on multidisciplinary teams.

[PO-5] Identify, formulate, and solve engineering problems.

[PO-6] Have an understanding of professional and ethical responsibility.

[PO-7] Communicate effectively.

[PO-8] Achieve broad education necessary to understand the impact of electrical engineering solutions in a global and societal context.

[PO-9] Understand learning processes, concepts of learning to learn, and engage in lifelong learning.

[PO-10] Achieve knowledge of contemporary issues.

[PO-11] Use techniques, skills, and computer-based tools for conducting experiments and carrying out designs.

[PO-12] Develop an appreciation for principles of business practices and entrepreneurship.

ABET Outcomes

3a- an ability to apply knowledge of mathematics, science, and engineering

3b- an ability to design and conduct experiments, as well as to analyze and interpret data

3c- an ability to design a system, component, or process to meet desired needs

3d- an ability to function on multi-disciplinary teams

3e- an ability to identify, formulate, and solve engineering problems

3f- an understanding of professional and ethical responsibility

3g- an ability to communicate effectively

3h- the broad education necessary to understand the impact of engineering solutions in a global and societal context

3i- a recognition of the need for, and an ability to engage in life-long learning

3j- a knowledge of contemporary issues

3k- an ability to use the techniques, skills, and modern engineering tools necessary for engineering practice

Relationship between the Course Learning Outcomes and Program/ABET Outcomes

The course learning outcomes map onto the program and ABET outcomes as depicted in the table below.

CLO	**Program Outcomes/ABET Outcomes**											
	PO-1/ 3(a)	PO-2/ 3(b)	PO-3/ 3(c)	PO-4/ 3(d)	PO-5/ 3(e)	PO-6/ 3(f)	PO-7/ 3(g)	PO-8/ 3(h)	PO-9/ 3(i)	PO-10/ 3(j)	PO-11/ 3(k)	P0-12
1								x				
2									x			
3	x											
4	x											
5	x											
6	x											
7	x											
8	x											
9	x											
10	x	x										
11		x	x								x	
12							x					