EENG 3520 Electronics II

Fall 2012
Tuesday & Thursday, 12:30 – 1:50 PM
Classroom: DP B227

Instructor: Ikechukwu (Ike) Agbor
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Office Hours: Monday & Wednesday from 11:00 to 1:00 pm or by appointment

Course Description

This course is a continuation of EENG 3510 (Electronics I). Topics will include single- and multi-stage amplifier, differential amplifier, feedback, and frequency response. The goals of this course are to expand the students' knowledge of basic electronics, to provide the students the design and analysis of advanced analog electronics circuits, and to expose the students to a variety of tradeoffs for practical electronics design.

Course Objectives

At the end of the class, the student should be able to:

- Describe the characteristics of single- and multi-stage amplifiers;
- Apply methods for the analysis of frequency response;
- Explain the advantage and disadvantage of feedback;
- Demonstrate the ability to design and implement a range of amplifiers;
- Simulate and analyze advance electronics circuits with PSPICE.

Textbooks

- *Required*: Adel S. Sedra and Kenneth C. Smith, Microelectronic Circuits, Sixth Edition, Oxford University Press, 2010, ISBN 978-0-19-532303-0.

Prerequisites

EENG 3510 Electronics I.

Grading Policies

In-class Quiz: 5%
Homework: 20% (Will NOT be accepted if late)
Project: 15% (Three Projects)
Exam #1: 10
Exam #2: 20%
Final Exam: 30%

Grade Distribution

90 - 100 = A
80 – 89 = B
70 – 79 = C
60 - 69 = D
Below 60 = F

General Comments

- In-class quizzes will be, given randomly throughout the semester, which serve the dual purpose of checking for attendance record and earning extra credit.
- You are expected to attend every lecture and responsible for announcements made during lecture, on the student access website, or via the class email list.
- Students are encouraged to discuss class material and homework in order to, better understand concepts. However, all the homework you submit must be of your own. Homework assignments are to be, turned in during class on the due date.
- The exams (two middle exams and final) are closed book with one page (8 ½ x 11) of notes allowed. Any request for "make-up" tests will be, subjected to university policy.
- All cell phones must be turned off during lecture. No food and drink are allowed in all classrooms and labs.

- It is the responsibility of students with certified disabilities to provide the instructor with appropriate documentation from the Dean of Students Office (see http://www.unt.edu/oda).
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Disabilities Accommodation:

The University of North Texas complies with Section 504 of the 1973 Rehabilitation Act and with the Americans with Disabilities Act of 1990. The University of North Texas provides academic adjustments and auxiliary aids to individuals with disabilities, as defined under the law. Among other things, this legislation requires that all students with disabilities be, guaranteed a learning environment that provides for reasonable accommodation of their disabilities. If you believe, you have a disability requiring accommodation, please see the instructor and/or contact the Office of Disability Accommodation at 940-565-4323 during the first week of class.

Course Topics (tentative)

- Building blocks of integrated-circuit amplifiers;
- Design and analysis of differential amplifiers;
- Design and analysis of multistage amplifiers;
- Feedback: analysis, design, and characteristics;
- Output stages and power amplifiers.
- CMOS digital logic circuits;
- Laboratory projects: design, analysis, and simulation using PSpice for typical single and multi-stage amplifiers, frequency response, and feedback.

Class Schedule (tentative)

Week	Date	Topics	Reading & Assignment	
1	Aug. 30	Review Ch. 1 and Ch. 2	Ch.1, Ch. 2	
2	Sep. 4	Review Ch. 3 and Ch. 6	Ch.3, Ch. 6	
	Sep. 6	Ch. 7 Building blocks of IC Amplifiers	7.1, 7.2 **HW1**	
3	Sep. 11	**Assign Project #1**	7.3	**HW1 due**
	Sep. 13		7.4	
4	Sep.18		7.5 **HW2**	
	Sep. 20		7.6	
5	Sep. 25	**Project #1**		**HW2 due**
	Sep. 27	Review		
6	Oct. 2	**Test #1**		
	Oct. 4	Ch. 8, Differential and Multistage Amps.	8.1, 8.2	
7	Oct. 9		8.3, 8.4	
	Oct. 11		8.5	
8	Oct. 16		8.6 **HW3**	
	Oct. 18	Ch. 10 Feedback	10.1, 10.2	
9	Oct. 23	**Assign Project #2**	10.3, 10.4	**HW3 due**
	Oct. 25	**Review**		
10	Oct. 30	**Test #2**		
	Nov. 1	Project#2		
11	Nov. 6		10.5, 10.6	
	Nov. 8		10.8, 10.9, 10.10	
12	Nov. 13		10.11 **HW4**	
	Nov. 15	Ch. 11, Output Stages and Power Amps.	11.1, 11.2	

13	Nov. 20	**Assign Project #3**	11.3, 11.4	**HW4 due**
	Nov. 22	Thanksgiving		
14	Nov. 27		11.5, 11.6	
	Nov. 29	Ch. 13, CMOS Digital Logic Circuits	13.1	
15	Dec. 4		13.2	**Project #3 due**
	Dec. 6	Review		
	Dec. 8 - 14	Final Exam Week		