EENG 5530- Analog Integrated Circuit Design (Spring 2022)

EENG 4010- Topics in EE (Spring 2022)

Mondays and Wednesdays 4 pm to 5:20 pm in B217

Description

Thoroughly investigates the fundamentals in design and analysis of analog and mixed-signal integrated circuits. Topics include analog MOS transistor models, current sources and sinks, circuit reference, amplifier, feedback amplifiers, differential amplifiers and operational amplifiers. Credit hours: 3 hrs.

Prerequisite(s): EENG 3520 or equivalent.

Instructor

Ifana Mahbub, Assistant Professor, Electrical Engineering Department Office B208, Email Ifana.Mahbub@unt.edu Phone: 940-369-7027 Office hours: Tuesdays and Thursdays 3 to 4 pm or by appointment.

Teaching Assistant

Karthik Kakaraparty, Ph.D. student, Office B250, Email karthikeyaanilkumarkakaraparty@my.unt.edu, Office hours: Monday and Wednesday 3 – 4 pm or by appointment.

Format

- Lectures, notes would be provided (See suggested reference textbooks)
- Online: announcements, grades via Canvas https://unt.instructure.com

Grade

Homeworks/Mini Assignments: 50%

Mid-term: 25%

Final Assignment: 25% (Report: 15%, Presentation: 10%)

Grade distribution

A=90-100, B=80-89, C=70-79, D=60-69, F=0-59

Schedules of exams

- Final Assignment Presentation days: April 27, May 2, and May 4, 2022
- Final Report Submission Deadline: May 11, 2022

Textbooks

Required: R Jacob Baker, *CMOS- Circuit Design, Layout, Simulation*, John Wiley and Sons, 4th edition, 2019, ISBN 9781119481515.

Optional: Behzad Razavi, *Design of Analog CMOS Integrated Circuits*, McGraw-Hill, 2001, ISBN 0-07-238032-2.

Class Evaluation by Students

SPOT is a requirement for all organized classes at UNT and is available for your input at the end of the semester.

Course Learning Outcomes (CLO):

Upon successful completion of this course, the students will be able to:

- 1. Discuss the operation of a field-effect transistor in weak, moderate, and strong inversion and how it relates to SPICE parameters.
- 2. Describe the gain, speed, and matching trade-offs when setting the width, length, and overdrive of transistors.
- 3. Analyze and design transistor current mirrors, amplifiers, and differential amplifiers.
- 4. Design and analyze voltage and current references.
- 5. Design op-amps for specific gain, speed, or switching performance.
- 6. Analyze the frequency response of amplifier and operational amplifier circuits.
- 7. Compensate operational amplifiers for stability.

ABET Student Learning Outcomes (SO)

- 1. an ability to identify, formulate, and solve complex engineering problems by applying principles of engineering, science, and mathematics
- 2. an ability to apply engineering design to produce solutions that meet specified needs with consideration of public health, safety, and welfare, as well as global, cultural, social, environmental, and economic factors
- 3. an ability to communicate effectively with a range of audiences
- 4. an ability to recognize ethical and professional responsibilities in engineering situations and make informed judgments, which must consider the impact of engineering solutions in global, economic, environmental, and societal contexts
- 5. an ability to function effectively on a team whose members together provide leadership, create a collaborative and inclusive environment, establish goals, plan tasks, and meet objectives
- 6. an ability to develop and conduct appropriate experimentation, analyze and interpret data, and use engineering judgment to draw conclusions
- 7. an ability to acquire and apply new knowledge as needed, using appropriate learning strategies

	LO Student/ABET Criterion 3 Outcomes						
CLO							
	SO-1/	SO-2/	SO-3/	SO-4/	SO-5/	SO-6/	SO-7/
	3[1]	3 [2]	3 [3]	3 [4]	3 [5]	3 [6]	3 [7]
1	X						
2	X						
3	X						
4	X					X	
5	X					X	

6	x			
7	X			

Policies

- A. Academic Integrity Standards and Consequences. According to UNT Policy 06.003, Student Academic Integrity, academic dishonesty occurs when students engage in behaviors including, but not limited to cheating, fabrication, facilitating academic dishonesty, forgery, plagiarism, and sabotage. A finding of academic dishonesty may result in a range of academic penalties or sanctions ranging from admonition to expulsion from the University. See full policy at https://policy.unt.edu/sites/default/files/06.003.pdf.
- B. ADA Accommodation Statement. UNT makes reasonable academic accommodation for students with disabilities. Students seeking accommodation must first register with the Office of Disability Accommodation (ODA) to verify their eligibility. If a disability is verified, the ODA will provide a student with an accommodation letter to be delivered to faculty to begin a private discussion regarding one's specific course needs. Students may request accommodations at any time, however, ODA notices of accommodation should be provided as early as possible in the semester to avoid any delay in implementation. Note that students must obtain a new letter of accommodation for every semester and must meet with each faculty member prior to implementation in each class. For additional information see the ODA website at disability.unt.edu.
- C. **Emergency Notification & Procedures.** UNT uses a system called Eagle Alert to quickly notify students with critical information in the event of an emergency (i.e., severe weather, campus closing, and health and public safety emergencies like chemical spills, fires, or violence). In the event of a university closure, please refer to Blackboard for contingency plans for covering course materials.
- E. Student Evaluation Administration Dates. Student feedback is important and an essential part of participation in this course. The student evaluation of instruction is a requirement for all organized classes at UNT. The survey will be made available during weeks 13, 14 and 15 of the long semesters to provide students with an opportunity to evaluate how this course is taught. Students will receive an email from "UNT SPOT Course Evaluations via IASystem Notification" (no-reply@iasystem.org) with the survey link. Students should look for the email in their UNT email inbox. Simply click on the link and complete the survey. Once students complete the survey they will receive a confirmation email that the survey has been submitted. For additional information, please visit the SPOT website at www.spot.unt.edu or email spot@unt.edu.

Tentative Course Calendar

Week	Date	Topics	Homework/Mini Assignment
1	01/19	Introduction (Recorded lecture)	

2	01/24	MOS small-signal analysis, Norton drain, Thevenin source models, etc.	
	01/26	MOS modeling from weak through strong inversion	1 (Due Date: 02/07)
3	01/31	MOS modeling from weak through strong inversion	
	02/02	MOS modeling from weak through strong inversion	
4	02/07	MOS resistors, switches and transmission gates	2 (Due Date: 02/16)
	02/09	MOS resistors, switches and transmission gates (Will be taught by the TA)	
5	02/14	MOS Current mirrors-simple,cascode, LV cascode, regulated cascode	
	02/16	MOS Current mirrors-simple,cascode, LV cascode, regulated cascode	3 (Due Date: 02/28)
6	02/21	Band-gap reference and LDO	
	02/23	Band-gap reference and LDO	
7	02/28	MOS single-stage amplifier using Thevenin and Norton model	4 and 5 (Due Date: 03/09)
	03/02	MOS single-stage amplifier using Thevenin and Norton model	
8	03/07	Mid-term Exam review	
	03/09	Mid-term Exam	
9	03/14	Spring break	
	03/18	Spring break	
10	03/21	MOS single-stage amplifier frequency response	Final project post
	03/23	MOS differential amplifiers – differential, CM, PS "half circuits"	
11	03/28	MOS differential amplifiers – differential, CM, PS "half circuits"	
	03/30	MOS single stage, dominant pole op amps (OTA) two-stage op amps	

12	04/04	MOS single stage, dominant pole op amps (OTA) two-stage op amps	
	04/06	MOS single stage, dominant pole op amps (OTA), two-stage op amps	
13	04/11	MOS fully differential Op amps (Common mode feedback)	
	04/13	MOS fully differential Op amps (Common mode feedback)	
14	04/18	MOS single-stage amplifier frequency response	
	04/20	Design review for final assignment design projects (with the TA)	
15	04/25	MOS single-stage amplifier frequency response	
	04/27, 05/02 & 05/04	Final Assignment Presentation 04/27 – Group 1 -8 05/02 - Group 9 -16 05/04 – 17 - 24	Final report due on Canvas by May 11 th , 2022

Cadence Software Access:

The undergraduate and graduate students will be using the 0.5 micron CMOS process.

Lab computers where you can access Cadence:

You should be able to remotely log in to the Cadence server following the remote access tutorial posted on Canvas.