

CSCE 4610: Computer Systems Architecture

Instructor: Hui Zhao
My Office: F278 Discovery Park
My Phone: 940-369-8189
My Email: hui.zhao@unt.edu
My Web: <http://www.cse.unt.edu/~huizhao/>
My Office Hours: Tuesdays /Thursdays
11:00am-12:00pm

TA: Yuwen Cui
(cuiyuwen@my.unt.edu)
TA Office Hours: TBA

Tentative Breakdown Of Course Grades

2 Mid Semester Exams	40%
Final	20%
Homework Assignments	20%
Term Project	15%
Discretion	5%

Prerequisites: CSCE 2610, CSCE 3612 or CSCE 3600

Primarily, you should know how a basic CPU works, assembly language programming in MIPS (or ARM) instruction, memory organization, ALU (including multiplication, division and floating point algorithms), and some understanding of compilers and runtime support, Operating system concepts like process scheduling, virtual memory, protection domains, etc.

Exams and Grading Policies: All exams (mid-semester and final) are "open-book" format. The final exam is not comprehensive. Every exam will be graded using a "relative point" system. For each problem, the best among all the solutions presented by the students (which gets the highest grade) will be selected and all the others will be graded relative to the best solution.

ABET Course Outcomes for CSCE 4610

1. Apply metrics to evaluate performance and power requirements of modern computer systems. Represent performance using arithmetic, harmonic and geometric means.
2. Understand Amdahl's law as applied to a single core and multicore systems.
3. Design a pipelined processor to meet design specifications.
4. Design an out-of-order and speculative processor to improve performance.
5. Understand cache memory performance issues.
6. Understand cache memory issues in multicore systems include cache coherency management.
7. Understand hardware support for concurrency including multithreading, locks and barriers.

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Course Outline

Course materials are on Canvas

	Hours
1. Introduction and Background	6
What is computer architecture	
Instruction sets, control unit	
Performance evaluation	
2. Memory Systems	10
Memory hierarchy	
Cache memory designs	
Improving cache performance	
Main memory and Virtual memory	
DRAM and SSD technologies	
3. Pipeline and out of order execution	10
Basic design of pipelines	
Data and control hazards	
Branch prediction and dynamic scheduling	
Superscalar and multiple issue processors	
VLIW or EPIC	
4. Shared Memory Multiprocessors	8
Mutual Exclusion and Synchronization	
Cache Coherency Problem and Solutions	
Distributed Shared Memory Systems	
5. Dataflow and multithreaded architectures	6
Dataflow model of computation	
What is multithreading Scheduled Dataflow	
SMT and Hyper Threading	
6. Low Power Issues	4

Textbook: J. Hennessy and D. Patterson. “Computer Architecture: A Quantitative Approach”, 5th Edition (Materials from older editions will also be used)

Other Useful Books:

1. J.P. Shen and M.H. Lipasti. “Modern Processor Design”, McGraw Hill, 2005
2. D.E. Culler and J.P. Singh. “Parallel Computer Architecture”, Morgan Kaufman, 1999