EENG 5530: Analog Integrated Circuit Design

Fall 2026 | 3 Credit Hours | Graduate Course

Section	1	**Meeting**	Moy/Wed, 1:50-3:10 PM
Location	NTDP B142	**Instructor**	Dr. Hyusim Park
Office Hours	Mo/Wed 12:30-1:30 PM	**Office**	Discovery Park E255
Email	Hyusim.Park@unt.edu	**Prerequisite**	EENG 3520 or equivalent

1. Course Description

Catalog-aligned description. This course develops the analysis and design methods used in analog and mixed-signal integrated circuits. Topics include MOS transistor models, biasing networks, current sources and mirrors, voltage and current references, single-stage and differential amplifiers, feedback, frequency response, operational-amplifier architectures, noise, mismatch, and computer-aided IC design.

Combined-Course Structure

EENG 4530 and EENG 5530 share lectures, textbook coverage, and core course topics. Students enrolled in EENG 5530 are expected to demonstrate greater depth in analysis, more independent design decisions, and more rigorous verification and technical communication.

2. Learning Outcomes

By the end of the semester, a successful student will be able to:

1. Use appropriate long-channel and short-channel MOS models to estimate operating points, transconductance, output resistance, intrinsic gain, capacitances, and frequency response.
2. Design and evaluate current mirrors, bias networks, cascodes, references, and startup circuits under headroom and power constraints.
3. Analyze and design common-source, common-gate, source-follower, cascode, and differential amplifier stages with active loads.
4. Relate topology and sizing choices to gain, bandwidth, slew rate, output swing, common-mode range, noise, power, and area.
5. Apply feedback theory and loop-gain concepts to analyze closed-loop analog circuits and amplifier performance.
6. Design an operational transconductance amplifier or analog front-end from a written specification and justify major tradeoffs.
7. Use OrCAD Capture and PSpice to perform operating-point, DC sweep, AC, transient, noise, parametric, temperature, sensitivity, and device-parameter variation analyses.
8. Interpret hand-analysis-versus-simulation and nominal-versus-variation discrepancies and recommend corrective design changes.
9. Communicate an analog IC design through calculations, schematics, simulation evidence, concise technical writing, and oral presentation.

3. Required Background

Students are expected to be comfortable with:

- KCL/KVL, node-voltage analysis, Thevenin/Norton equivalents, and first-order RC behavior;
- MOSFET operating regions, biasing, and small-signal models;
- single-transistor amplifier analysis and basic differential-pair concepts;
- complex impedance, transfer functions, Bode plots, poles, and zeros;
- prior experience using OrCAD Capture and PSpice for schematic entry and basic operating-point, DC, AC, and transient simulation. Prior PSpice experience is required. PSpice operation will not be taught as a regular lecture topic; **students are expected to use PSpice independently for project**;

Readiness responsibility. A short review module will be provided, but students are responsible for closing prerequisite gaps early.

4. Course Materials and Software

Required Textbook and Software

- Required textbook: Behzad Razavi, Design of Analog CMOS Integrated Circuits, 2nd ed., McGraw-Hill.
- Access to a computer capable of connecting to UNT engineering computing resources.
- OrCAD Capture and PSpice through UNT or student-accessible computing resources. **Prior experience with SPICE-based circuit simulation is required. PSpice will be used for course assignments and projects. Students are expected to be familiar with PSpice or to independently acquire the necessary PSpice skills. PSpice instruction is not part of the regular lecture.** Course-provided MOSFET model files will be used for transistor-level simulations. Students must retain organized, backed-up copies of all schematics, model files, simulation profiles, plots, and reports.

Supplementary References

- Occasional instructor-provided handouts, selected papers, problem statements, and design files posted in Canvas are supplementary and will not replace the textbook as the primary lecture source.
- Paul R. Gray, Paul J. Hurst, Stephen H. Lewis, and Robert G. Meyer, Analysis and Design of Analog Integrated Circuits, 5th ed.
- R. Jacob Baker, CMOS: Circuit Design, Layout, and Simulation, 4th ed.
- Phillip E. Allen and Douglas R. Holberg, CMOS Analog Circuit Design, 3rd ed.

Model files and course libraries. Any MOSFET model, component library, example circuit, or licensed software resource provided for the course may be used only under the applicable UNT and vendor access terms. Students may not redistribute proprietary files.

5. Course Organization and Major Requirements

Component	Weight	Description	Typical Format
Homework	20%	Textbook-based analytical problems and short design exercises. Some problems include a graduate extension.	4 Homework
Exam 1	20%	In-class assessment covering Chapters 1-6	In class
Exam 2	20%	In-class assessment covering Chapters 7-9.	In class
Graduate Design Project	40%	Open-ended analog IC design with specifications, variation-aware PSpice verification, technical report, and oral defense.	Individual (EENG5530) Team (EENG4530)

Textbook-led pacing. Regular lectures will follow the assigned Razavi chapters and emphasize derivations, worked examples, and design reasoning. PSpice operation is not a regular lecture topic.

**Team projects require clearly documented individual contributions. The instructor may require an individual oral check or design-defense question for each team member.*

Homework and PSpice Design Assignments

Software-learning expectation. PSpice procedures are not taught during regular lecture meetings. Students are expected to enter the course with basic PSpice experience and to complete software setup and troubleshooting independently, with brief reference materials and office-hour assistance available as needed.

Homework will be based primarily on the assigned textbook chapters and instructor-selected design problems. PSpice assignments are completed independently outside regular lecture meetings. Assignments are intended to connect textbook analysis, simulation, and engineering interpretation. A complete technical submission normally includes:

- the governing assumptions and equations, not only final numerical answers;
- clearly labeled schematics and device sizes;
- plots with readable axes, units, legends, and operating conditions;
- a concise comparison between prediction and simulation;
- the design files or netlists requested in the assignment; and
- a brief explanation of any discrepancy, failed specification, or corrective iteration.

Design Project

Each EENG 5530 student will design and verify a transistor-level analog block or front-end under realistic constraints using PSpice. Typical project options include a two-stage OTA, folded-cascode OTA, telescopic amplifier, low-power sensor interface, transimpedance amplifier, or another approved analog block.

Deliverable	Target Date	Minimum Content
Project proposal	Sept. 16	Architecture, specifications, technology assumptions, first-order feasibility, and work plan.
Design checkpoint	Oct. 21	Biasing, operating points, hand estimates, nominal simulation, and unresolved risks.
Design review	Nov. 11	Updated design, nominal DC/AC/transient verification, loop or frequency analysis as appropriate, a supply/temperature and device-parameter variation plan, and preliminary comparison with a published design or established reference.
Presentation / defense	Nov. 30 or Dec. 2	Approximately 12 minutes plus questions; every student must defend design choices and verification results.
Final package	Dec. 4	8-10 page report, complete simulation evidence, supply-voltage, temperature, and device-parameter variation results, PSpice project files, and a reproducibility note.

Minimum graduate verification. The final design must include nominal performance, at least three meaningful supply-voltage and temperature conditions, parameter sensitivity analysis, and device-parameter variation analysis. Merely reproducing a tutorial circuit does not satisfy the project requirement.

6. Graduate-Level Differentiation from EENG 4530

Area	EENG 4530 Baseline	EENG 5530 Graduate Expectation
Analytical work	Core calculations and guided design steps.	Additional derivations, tradeoff analysis, and justification of assumptions.
Simulation	Nominal operating-point, AC, and transient verification.	Nominal plus supply-voltage, temperature, and device-parameter variation, sensitivity, and failure analysis.
Design project	More structured specifications and architecture.	Open-ended architecture selection with literature-supported decisions.
Physical effects	Introductory awareness of device parasitics and model limitations.	Advanced variation, sensitivity, and model-based parasitic verification.
Communication	Concise report and presentation.	8-10 page technical report and oral defense with reproducibility evidence.

7. Grading

A	B	C	D	F
90-100	80-89.99	70-79.99	60-69.99	Below 60

Evaluation Standards

- Correctness: analysis, models, calculations, and interpretation are technically sound.
- Completeness: all required operating conditions, plots, files, and explanations are included.
- Design quality: the solution meets specifications or clearly identifies and explains remaining limitations.
- Verification quality: simulation settings are appropriate, reproducible, and sufficient to support the claims.
- Communication: figures, tables, units, captions, and prose are clear and professional.
- Engineering judgment: tradeoffs and design decisions are justified rather than presented as unexplained trial-and-error.

Regrade Requests

A regrade request must be submitted in writing within seven calendar days after the graded work is returned. The request must identify the specific item, the suspected grading error, and the technical basis for the request. The entire submission may be reviewed for consistency.

8. Course Policies

Attendance and Participation

Regular attendance is expected because design methods and project guidance build cumulatively. Attendance is not assigned a separate point value, but missed in-class work, announcements, design reviews, or assessments remain the student's responsibility. The course includes two in-class examinations. During each scheduled examination week, no regular lecture will be held; only the announced examination session will occur. Authorized absences will be handled in accordance with UNT Policy 06.039. Students should notify the instructor as early as practical and provide required documentation.

Late Work and Missed Assessments

- Homework and design assignments may be submitted up to 24 hours after the deadline with a 20% deduction**. Work more than 24 hours late is not accepted** unless an extension was approved before the deadline or an authorized/exceptional circumstance applies.
- Make-up examinations are provided only for authorized absences or circumstances approved by the instructor. The format may differ from the original assessment.
- **Technical problems are not automatically grounds for an extension. Students should back up PSpice projects, model files, simulation profiles, reports, and plots throughout the semester.**

Communication and Canvas

Canvas and the student's UNT email account are the official channels for course announcements, assignment updates, and emergency continuity plans. Students should check both regularly.

9. Academic Integrity

Academic dishonesty includes cheating, plagiarism, fabrication, facilitating another student's dishonesty, forgery, sabotage, unauthorized collaboration, falsified simulation results, and misrepresentation of AI-generated work. These behaviors are governed by UNT Policy 06.003.

Course-specific consequences. A confirmed violation may result in a zero on the affected work, a reduced or failing course grade, and referral through the university academic-integrity process. Copying or sharing examination answers, complete assignment solutions, design libraries, netlists, reports, or fabricated plots is considered a serious violation. The instructor will determine the academic penalty based on the nature and severity of the incident while following university procedures.

Citation expectation. Published circuits, equations, figures, code, scripts, measurement data, and design ideas that are not the student's own must be cited. Reusing one's own previously submitted work also requires permission and disclosure when the new assignment expects original work.

10. Accessibility and Student Support

Disability Accommodations

UNT provides reasonable academic accommodations for students with disabilities. Students seeking accommodations must first register with the Office of Disability Access (ODA) and obtain an accommodation letter for the current semester. After receiving the letter, the student should contact the instructor promptly for a private discussion so approved accommodations can be implemented without avoidable delay. Additional information is available through the ODA website.

Emergency Notification and Course Continuity

UNT uses Eagle Alert to communicate critical information involving severe weather, campus closures, public-safety incidents, and other emergencies. During a university closure or interruption, students should consult Canvas and UNT email for adjusted meetings, deadlines, or alternative activities. Students should follow all campus and building instructions.

Student Support

- Students experiencing academic difficulty should contact the instructor early; waiting until the final weeks greatly limits available options.
- UNT provides tutoring, writing support, counseling, health services, technology assistance, and other student services. Current service information is available through UNT student-support websites.
- Students affected by sexual misconduct, relationship violence, stalking, or sexual assault may contact UNT Survivor Advocates or the Dean of Students for support. Reports to the Title IX Coordinator are handled under current university policy.

11. Safety and Data Practices

This course primarily uses computer-based design tools rather than a physical electronics laboratory. Students working in any instructional or research laboratory must follow posted safety rules, complete required training, and use equipment only as authorized. Do not connect personal hardware to laboratory systems or probe powered circuits without instructor approval. Protect proprietary model files, licensed software, and unpublished project data; do not upload restricted design content to public repositories or external AI services.

12. Tentative Course Schedule

Wk	Topics	Reading
1	Chapters 1-2: analog IC design perspective and specifications; MOS device operation, large-signal models, small-signal parameters, and a focused review of the transistor concepts needed for analog IC design.	Razavi Chs. 1-2
2	Chapter 3: single-stage amplifiers, including common-source, common-gate, source-follower, and cascode stages; gain, output resistance, headroom, and worked design examples.	Razavi Ch. 3
3	Differential amplifiers: large-signal and small-signal behavior, active loads, common-mode response, CMRR, input common-mode range, and practical design tradeoffs.	Razavi Ch. 4
4	Labor Day on Sept. 7 (no class). Biasing and current mirrors on Sept. 9: basic and cascode mirrors, output resistance, headroom, bias networks, and current-reference design.	Razavi Ch. 5

Wk	Topics	Reading
5, 6, 7	Frequency response I: device capacitances, Miller effect, dominant poles, zeros, and first-order high-frequency analysis of common amplifier stages. Frequency response II: pole/zero estimation, bandwidth limitations, gain-bandwidth tradeoffs, and worked frequency-response examples.	Razavi Ch. 6
8	**Exam 1 week**; no regular lecture.	Review Chs. 1-6
9	Noise: thermal and flicker noise, resistor and MOS noise models, input-referred noise, noise propagation, device sizing and bias-current tradeoffs, and integrated noise.	Razavi Ch. 7
10, 11	Feedback I: feedback concepts, loop gain, closed-loop gain, desensitization, accuracy, and the major feedback topologies. Feedback II: loading, input/output impedance modification, loop-gain interpretation, nonidealities, and worked feedback-amplifier examples.	Razavi Ch. 8
12, 13	Operational amplifiers I: architecture choices, gain stages, biasing, output swing, input common-mode range, and first-order design from specifications. Operational amplifiers II: two-stage and higher-gain structures, output stages, slew-rate considerations, and worked op-amp design examples. Operational amplifiers III: design tradeoffs, specification-driven sizing, gain/bandwidth/power/headroom tradeoffs, and integrated design examples.	Razavi Ch. 9
14	**Exam 2 week**; no regular lecture.	Review Chs. 7-9
15	Thanksgiving Break - no classes.	-
16	Project presentations and oral design defense; course wrap-up. No new course content on Dec. 2 (Pre-Finals Day).	Review Chs. 1-9