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EDUCATION

1991 - 1997	LOUISIANA STATE UNIVERSITY Ph.D. in Electrical Engineering	BATON ROUGE, LA
1987 - 1988	LOUISIANA STATE UNIVERSITY MS in Physics	BATON ROUGE, LA
1985 - 1987	LOUISIANA STATE UNIVERSITY MS in Electrical Engineering	BATON ROUGE, LA
1980 - 1985	UNIVERSITY OF PATRAS Diploma in Electrical Engineering	PATRAS, GREECE

INDUSTRIAL AND ACADEMIC EMPLOYMENT

DEPT. OF ELECTRICAL ENGINEERING UNIVERSITY OF NORTH TEXAS	DENTON, TX
9/2019 – Present: Professor	
DEPT. OF ENGINEERING TECHNOLOGY UNIVERSITY OF NORTH TEXAS	DENTON, TX
9/2016 – 8/2019: Professor	
9/2010 – 8/2016: Associate Professor (Tenured)	
1/2004 – 8/2010: Assistant Professor (Tenure Track)	
Specific duties include:	
<ul style="list-style-type: none">I perform research in Internet of Things applications for smart healthcare, blockchain and physical cybersecurity.Other areas of my research are: Analog/Mixed-Signal and RF IC design and design automation.I maintain an active search for external funding sources in support of my research.I am co-founder of the Smart Electronic Systems Laboratory (SESL, https://www.smohanty.org/SESL/index.html)I teach and develop undergraduate and graduate courses. Also create and maintain laboratories pertinent to these courses.I supervise undergraduate students in senior project work (40+ to date).I supervise graduate students in thesis and dissertation work (15 PhD and 25 MS graduated to date).I perform service at the Department, College, University, and Professional Society level.	DENTON, TX

2000 – 2004	CADENCE DESIGN SYSTEMS, INC.	DALLAS, TX
Technical Leader, Custom Analog/Mixed Signal Integrated Circuits		
I worked with enterprise accounts, Texas Instruments, Intel and Motorola in particular. Approx. 90% of the time I was on-site at customer design centers. My main responsibilities were to facilitate design		

of large Mixed Signal, Analog and RF ICs by developing methodologies, flows and providing design expertise and, concurrently, establishing the adoption of Cadence's mixed-signal framework (AMS Designer) and analog simulation tools (Spectre/SpectreRF) by design groups in the High Performance Analog, Mixed Signal (BigA/BigD) and Wireless areas.

Specific duties included:

- Consultation with design groups with regards to their internal IC design tool flows and design practices, in particular Analog, Mixed-Signal and RF designs and methodologies.
- Design architecting
- Analog/MS and RF simulation
- I developed and maintained libraries of behavioral models (in Verilog/Verilog-A, Verilog-AMS and VHDL-AMS) of analog and digital IC building blocks (PLLs, VCOs, Comparators, OpAmps, Bandgap References, Mixers, ROM/RAMs etc.)
- Participated in the development of complete Layout-vs-Schematic (LVS), R, C and L extraction (RCLX) and parasitic resimulation support for CMOS, BiCMOS and RF SiGe processes.
- Recognized as Cadence's foremost field expert in parasitic resimulation with the latest generation physical verification tools.
- Expert or advanced user of tools such as Analog Artist, Virtuoso, Verilog, Verilog-A, Verilog-AMS, AMS Designer, Signal Processing Workbench, Spectre and SpectreRF. Main emphasis was towards analog, mixed-signal and RF circuit and system simulation tools and methodologies.
- Expert-level knowledge of Unix/Linux, C/C++ programming and Perl and Tcl/Tk scripting.

1999 – 2000 AVANT! CORPORATION (NOW [SYNOPSYS](#))

PHOENIX, AZ AND DALLAS, TX

Sr. Applications Engineer

As a member of Avant!'s technical support organization, my duties concentrated on providing technical assistance to our major accounts (such as Intel, Motorola, Texas Instruments, Qualcomm, Conexant etc.)

Specific duties included:

- I supported Avant!'s Device-level parasitic extraction (Raphael/Raphael NES), Lithography (Taurus OPC/PSM) and Technology CAD (TSUPREM4, MEDICI, Taurus Process/Device) software in TX, AZ and Southern CA.
- I was the primary world-wide contact for Avant!'s device-level field-solver products.
- I interfaced with the software development groups to ensure alignment with customer requirements and industry trends.
- I assisted customers with the installation and configuration of our EDA software as well as its integration with simulation flows that include competitor's products.

1999 [DEVRY UNIVERSITY](#)

IRVING, TX

Assistant Professor

- Taught C/C++ Programming, Digital Signal Processing (with lab), Unix & NT Networking and Advanced Telecommunications at the junior and senior level.
- Recipient of the 1999 Ron Taylor award for excellence in teaching.
- Founding member of the Computer Engineering Technology program (deployed across 17 North America DeVry campuses).
- Developed and authored curriculum and lab guides for new courses (CET-421: Advanced Operating Systems, EET 475: Advanced Unix Networking.)
- Supervised 4 senior projects.
- Chaired the Communications Faculty Committee and participated in the Programming Faculty Committee.
- Member of the Technology in Engineering DeVry corporate Committee.

1989 – 1998 [TEXAS INSTRUMENTS, INC.](#)

HOUSTON, LUBBOCK AND DALLAS, TX

Member Technical Staff - Research

I was a member of TI's prestigious Silicon Technology Development (SiTD) R&D center in Dallas, TX. My tenure with TI lasted almost 10 years and is divided in 3 distinct phases. For the time period Aug. 97 – Dec. 98 I was a full-time employee in Dallas, TX. During the time period Aug. 91 – Dec. 97 I was employed part time while also pursuing my Ph.D. at Louisiana State University. Finally, from Apr. 89 to Aug. 91 I was a full-time Design Engineer employed in TI's Application-Specific Memory Products (ASMP) division in Houston, TX. Specific duties and accomplishments included:

- Provided corporate-wide development and strategic evaluation of custom and commercial EDA and Technology CAD software.
- Responsible for understanding the basic physics of new devices under development (particularly EEPROMs and Flash memories), improving device performance, developing new designs and technologies and performing process and electrical simulations.
- Interfaced with university EDA groups (Stanford, University of Florida, University of Texas, Purdue and Boston University) to obtain and evaluate TCAD software and provide suggestions for further research. Also made recommendations on R & D fund allocation to various research institutions.
- Developed novel simulation tools to characterize circuit behavior of floating gate structures and performed design and process optimization to maximize device endurance and reliability.
- Provided extensive process and electrical characterization of pre-production devices at wafer level. Interfaced semiconductor characterization equipment to a central data acquisition system and wrote all controlling software.
- Developed, configured and maintained Linux Beowulf clusters for TCAD applications. Also ported internally developed TCAD and EDA tools to various platforms.

1991 – 1997 [LOUISIANA STATE UNIVERSITY](#)

BATON ROUGE, LA

Research and Teaching Assistant (Part Time)

- Developed Poisson and Laplace field solvers using stochastic (Monte Carlo) as well as traditional (finite elements, finite differences & boundary elements) techniques.
- Performed research on modeling and simulation of Heterojunction Bipolar Transistors, Solar Cells, Resonant Tunneling Devices and novel Quantum Heterostructure Devices.
- Performed large-scale numerical simulation of physical processes in electronic devices and electron lenses utilizing both deterministic and Monte Carlo methods.
- Taught over 40 sections of Circuits, Electronics I & II, Analog and Digital Electronics labs at the sophomore, junior and senior level.
- Twice on the Dean's list of outstanding teachers.

1988 – 1989 [COMPUTER VENTURES, INC.](#)

BATON ROUGE, LA

Applications Development Engineer

- Wrote and used modular code for User Interface, Graphics, Database, Communications and Statistical Process Control applications in C, Pascal, FORTRAN, 80x86 Assembly, Basic and HP Basic under UNIX, X11, MS-DOS and MS Windows operating systems.
- Developed software and provided hardware interfaces for data-acquisition systems.

BOOKS

S. P. Mohanty, N. Ranganathan, **E. Kougianos** and P. Patra, [Low-Power High-Level Synthesis for Nanoscale CMOS Circuits](#), Springer, 2008. ISBN: 978-0-387-76473-3

BOOK CHAPTERS

L. Rachakonda*, Sarma, A., S. P. Mohanty, and E. Kougianos, "Good-Eye: A Combined Computer-Vision and Physiological Sensor Based Device for Full-Proof Prediction and Detection of Fall of Adults", [Internet of Things. A Confluence of Many Disciplines](#), Casaca, A., Katkoori, S., Ray, S., and Strous, L. (Editors), Springer International Publishing, 2020, ISBN: 978-3-030-43605-6 (http://dx.doi.org/10.1007/978-3-030-43605-6_16)

S. P. Mohanty, and E. Kougianos, "SPICEless RTL Design Optimization of Nanoelectronic Digital Integrated Circuits", in [Nano-CMOS and Post-CMOS Electronics: Circuits and Design](#), A. Srivastava and S. P. Mohanty (Editors), Institution of Engineering and Technology (IET), 2016, ISBN: 978-1-84919-999-5

V. P. Yanambaka*, S. P. Mohanty, E. Kougianos and D. Ghai, "Nanoscale high-k/metal gate CMOS and FinFET based logic libraries", in [Nano-CMOS and Post-CMOS Electronics: Devices and Modelling](#), S. P. Mohanty and A. Srivastava (Editors), Institution of Engineering and Technology (IET), 2016, ISBN: 978-1-84919-997-1

S. P. Mohanty and E. Kougianos, "Polynomial Metamodel-Based Fast Optimization of Nanoscale PLL Components", in [Models, Methods, and Tools for Complex Chip Design: Selected Contributions from FDL 2012](#), Jan Haase (Editor), Springer, 2014, pp. 179-200. ISBN: 978-3-319-01417-3

BOOK REVIEWS

E. Kougianos, "Nanoelectronic Mixed-Signal System Design", IEEE Consumer Electronics Magazine, Vol. 6, No. 1, pp. 147-148, Jan. 2017. DOI: [10.1109/MCE.2016.2614559](https://doi.org/10.1109/MCE.2016.2614559)

PATENTS (AWARDED)

2. E. Kougianos, and S. P. Mohanty, "[Methodology for Nanoscale Technology based Mixed-Signal System Design](#)", US Patent 9,053,276 issued on June 9, 2015.

1. E. Kougianos, S. P. Mohanty, and G. Zheng*, "[An Intelligent Metamodel Integrated Verilog-AMS for Fast and Accurate Analog Block Design Exploration](#)", US Patent 9,026,964 issued on May 5, 2015.

PATENTS (PENDING)

4. E. Kougianos, S. P. Mohanty and A. Mitra "Method for Synthetic Video/Image Detection", USA Provisional Patent Application: 18/485,285. Filed on: 11 Oct. 2023.

3. E. Kougianos, S. P. Mohanty and A. Mitra "MyAgroPal: Systems of Systems to Assist Farmers", USA Provisional Patent Application: 63/510,881. Filed on: 28 June 2023.

2. E. Kougianos, S. P. Mohanty and L. Rachakonda "System and Method For Monitoring A State of A Driver", USA Provisional Patent Application: 18/185,717. Filed on: 17 Mar. 2023.

1. E. Kougianos, S. P. Mohanty and L. Rachakonda "Intelligent Diet, Sleep and Stress Management", USA Provisional Patent Application: 17/540,076. Filed on: 01 Dec. 2021.

PROFILE: (current as of Jan. 26, 2024)

	All	Since 2018
Citations	6985	4977
h-index	34	27
i10-index	110	67

AD SCIENTIFIC INDEX: #1 RANKED IN ELECTRICAL ENGINEERING AT UNT

REFEREED JOURNAL PAPERS PUBLISHED OR ACCEPTED FOR PUBLICATION (* INDICATES A STUDENT AUTHOR, ITALICS INDICATE A UNT COLLABORATOR)

74. M. A Sayeed, *S. P. Mohanty*, and **E. Kougianos**, "rSeiz 2.0: A Low Latency and Energy Efficient Seizure Detector in the IoMT", *Springer Nature Computer Science (SN-CS)*, Vol. 4, No. 5, Article: 532, Sep. 2023, 15 pages. DOI: DOI: <https://doi.org/10.1007/s42979-023-02051-1>.
73. A. Mitra, *S. P. Mohanty*, and **E. Kougianos**, "aGROdet 2.0: An Automated Real Time Approach for Multiclass Plant Disease Detection", *Springer Nature Computer Science (SN-CS)*, Vol. 4, No. 5, Article: 657, Sep. 2023, 20 pages. DOI: <https://doi.org/10.1007/s42979-023-02076-6>.
72. A. K. Bapatla*, D. Puthal, *S. P. Mohanty*, V. P. Yanambaka, and **E. Kougianos**, "EasyChain: An I-T-Friendly Blockchain for Robust and Energy-Efficient Authentication", *Frontiers in Blockchain*, Vol. 6, No. 1194883, pp. 1-19, Aug. 2023. DOI: <https://doi.org/10.3389/fbloc.2023.1194883>.
71. A. J. Alkhodair*, *S. P. Mohanty*, and **E. Kougianos**, "FlexiChain 3.0: Distributed Ledger technology Based Intelligent Transportation for Vehicular Digital Asset Exchange in Smart Cities", *MDPI Sensors*, Vol. 23, No. 8, 27 pages, Apr. 2023. DOI: <https://doi.org/10.3390/s23084114>.
70. A. K. Bapatla*, *S. P. Mohanty*, **E. Kougianos**, and D. Puthal, "PharmaChain: A Blockchain to Ensure Counterfeit-Free Pharmaceutical Supply Chain", *IET Networks*, Vol. 12, No. 2, pp. 53-76, Mar. 2023. DOI: <https://doi.org/10.1049/ntw2.12041>
69. S. L. T. Vangipuram*, *S. P. Mohanty*, **E. Kougianos**, and C. Ray, "G-DaM: A Distributed Data Storage with Blockchain Framework for Management of Groundwater Quality Data", *MDPI Sensors*, Vol. 22, No. 22, Nov. 2022. DOI: <https://doi.org/10.3390/s22228725>
68. S. L. T. Vangipuram*, *S. P. Mohanty*, **E. Kougianos**, and C. Ray, "agroString: Visibility and Provenance through a Private Blockchain Platform for Agricultural Dispense Towards Consumers", *MDPI Sensors*, Vol. 22, No. 21, Oct. 2022. DOI: <https://doi.org/10.3390/s22218227>
67. A. Mitra*, D. Bigioi, *S. P. Mohanty*, P. Corcoran, and **E. Kougianos**, "iFace 1.1: A Proof-of-Concept of a Facial Authentication Based Digital ID for Smart Cities", *IEEE Access Journal*, Vol. 10, pp. 71791-71804, July 2022. DOI: <https://doi.org/10.1109/ACCESS.2022.3187686>
66. V. K. V. V. Bathalapalli*, *S. P. Mohanty*, **E. Kougianos**, B. K. Baniya, and B. Rout, "PUFchain 2.0: Hardware-Assisted Robust Blockchain for Sustainable Simultaneous Device and Data Security in Smart Healthcare", *Springer Nature Computer Science (SN-CS)*, Vol. 3, No. 5, Sep. 2022 Article: 344, 19 pages. DOI: <https://doi.org/10.1007/s42979-022-01238-2>.

65. A. Mitra*, A. Singhal, S. P. Mohanty, E. Kougianos, and C. Ray "eCrop: A Novel Framework for Automatic Crop Damage Estimation in Smart Agriculture", *Springer Nature Computer Science (SN-CS)*, Vol. 3, No. 4, Jul. 2022 Article: 319, 16 pages. DOI: <https://doi.org/10.1007/s42979-022-01216-8>.
64. A. J. Alkhodair*, S. P. Mohanty, and E. Kougianos, "FlexiChain: A Minerless Scalable Next Generation Blockchain for Rapid Data and Device Security in Large Scale Complex Cyber-Physical Systems", *Springer Nature Computer Science (SN-CS)*, Vol. 3, No. 3, May 2022 Article: 235, 13 pages. DOI: <https://doi.org/10.1007/s42979-022-01139-4>.
63. L. Rachakonda, A. K. Bapatla*, S. P. Mohanty, and E. Kougianos, "BACTmobile: A Smart Blood Alcohol Concentration Tracking Mechanism for Smart Vehicles in Healthcare CPS Framework", *Springer Nature Computer Science (SN-CS)*, Vol. 3, No. 3, May 2022 Article: 236, 24 pages. DOI: <https://doi.org/10.1007/s42979-022-01142-9>.
62. Z. Huang, E. Kougianos, X. Ge, S. Wang, P. Daniel Chen, and L. Cai, "A Systematic Interdisciplinary Engineering and Technology Model Using Cutting-Edge Technologies for STEM Education", *IEEE Transactions on Education*, Vol. 64, No. 4, Nov. 2021, pp. 390-397. DOI: [10.1109/TE.2021.3062153](https://doi.org/10.1109/TE.2021.3062153)
61. S. L. T. Vangipuram*, S. P. Mohanty, and E. Kougianos, "CoviChain: A Blockchain based Framework for Nonrepudiable Contact Tracing in Healthcare Cyber-Physical Systems during Pandemic Outbreaks", *Springer Nature Computer Science (SN-CS)*, Vol. 2, No. 2, Jun. 2021 Article: 346, 16 pages. DOI: [10.1007/s42979-021-00746-x](https://doi.org/10.1007/s42979-021-00746-x).
60. I. L. Olokodana*, S. P. Mohanty, E. Kougianos, and R. S. Sherratt, "EZcap: A Novel Wearable for Real-Time Automated Seizure Detection from EEG Signals", *IEEE Transactions on Consumer Electronics*, Vol. 62, No. 2, pp. 166-175, May 2021 DOI: [10.1109/TCE.2021.3079399](https://doi.org/10.1109/TCE.2021.3079399)
59. D. Puthal, S. P. Mohanty, E. Kougianos, and G. Das, "When Do We Need the Blockchain?", *IEEE Consumer Electronics Magazine*, Vol 10, Issue 2, pp. 53-56, Mar. 2021 DOI: [10.1109/MCE.2020.3015606](https://doi.org/10.1109/MCE.2020.3015606)
58. A. Mitra*, S. P. Mohanty, P. Corcoran, and E. Kougianos, "A Machine Learning based Approach for DeepFake Detection in Social Media through Key Video Frame Extraction", *Springer Nature Computer Science (SN-CS)*, Vol. 2, No. 2, Feb. 2021 Article: 99, 18 pages. DOI: [10.1007/s42979-021-00495-x](https://doi.org/10.1007/s42979-021-00495-x).
57. L. Rachakonda*, A. K. Bapatla*, S. P. Mohanty, and E. Kougianos, "SaYoPillow: Blockchain-Integrated Privacy-Assured IoMT Framework for Stress Management Considering Sleeping Habits", *IEEE Transactions on Consumer Electronics*, Vol. 67, No. 1, Feb. 2021, pp. 20-29. DOI: [10.1109/TCE.2020.3043683](https://doi.org/10.1109/TCE.2020.3043683)
56. I. L. Olokodana*, S. P. Mohanty, E. Kougianos, and O. O. Olokodana, "Real-Time Automatic Seizure Detection using Ordinary Kriging Method in an Edge-IoT Computing Paradigm", *Springer Nature Computer Science (SN-CS)*, Vol. 1, No. 5, Sep. 2020 DOI: [10.1007/s42979-020-00272-2](https://doi.org/10.1007/s42979-020-00272-2)
55. A. K. Tripathy, A. G. Mohapatra, S. P. Mohanty, E. Kougianos, A. M. Joshi, and G. Das, "EasyBand: A Wearable for Safety-Aware Mobility During Pandemic Outbreak", *IEEE Consumer Electronics Magazine*, Vol. 9, Issue 5, pp. 57-61, Sep. 2020. DOI: [10.1109/MCE.2020.2992034](https://doi.org/10.1109/MCE.2020.2992034)
54. S. P. Mohanty, V. P. Yanambaka, E. Kougianos, and D. Puthal, "PUFChain: Hardware-Assisted Blockchain for Sustainable Simultaneous Device and Data Security in Internet of Everything (IoE)",

53. L. Rachakonda*, S. P. Mohanty, and E. Kougianos: "iLog: An Intelligent Device for Automatic Food Intake Monitoring and Stress Detection in the IoMT", *IEEE Transactions on Consumer Electronics*, Vol. 66, No. 2, pp. 115-124, May 2020. DOI: [10.1109/TCE.2020.2976006](https://doi.org/10.1109/TCE.2020.2976006)
52. L. Rachakonda*, S. P. Mohanty, E. Kougianos, and P. Sundaravadivel: "Stress-Lysis: A DNN-Integrated Edge Device for Stress Level Detection in the IoMT", *IEEE Transactions on Consumer Electronics*, Vol. 65, No. 4, pp. 474-483, November 2019. DOI: [10.1109/TCE.2019.2940472](https://doi.org/10.1109/TCE.2019.2940472)
51. V. P. Yanambaka*, S. P. Mohanty, E. Kougianos, and D. Puthal: "PMsec: Physical Unclonable Function-Based Robust and Lightweight Authentication in the Internet of Medical Things", *IEEE Transactions on Consumer Electronics*, Vol. 65, No. 3, pp. 388–397, August 2019. DOI: [10.1109/TCE.2019.2926192](https://doi.org/10.1109/TCE.2019.2926192)
50. Md. Abu Sayeed*, S. P. Mohanty, E. Kougianos, and H. P. Zaveri: "eSeiz: An Edge-Device for Accurate Seizure Detection for Smart Healthcare", *IEEE Transactions on Consumer Electronics*, Vol. 65, No. 3, pp. 379–387, August 2019. DOI: [10.1109/TCE.2019.2920068](https://doi.org/10.1109/TCE.2019.2920068)
49. Md. Abu Sayeed*, S. P. Mohanty, E. Kougianos, and H. P. Zaveri: "Neuro-Detect: A Machine Learning-Based Fast and Accurate Seizure Detection System in the IoMT", *IEEE Transactions on Consumer Electronics*, Vol. 65, No. 3, pp. 359–368, August 2019. DOI: [10.1109/TCE.2019.2917895](https://doi.org/10.1109/TCE.2019.2917895)
48. P. Sundaravadivel*, K. Kesavan, L. Kesavan, S. P. Mohanty, and E. Kougianos, "Smart-Log: A Deep-Learning based Automated Nutrition Monitoring System in the IoT", *IEEE Transactions on Consumer Electronics*, Vol. 64, Issue 3, pp. 390-398, August 2018. DOI: [10.1109/TCE.2018.2867802](https://doi.org/10.1109/TCE.2018.2867802)
47. D. Puthal, N. Malik, S. P. Mohanty, E. Kougianos, and G. Das, "Everything You Wanted to Know About the Blockchain", *IEEE Consumer Electronics Magazine*, Vol. 7, Issue 4, pp. 6-14, July 2018. DOI: [10.1109/MCE.2018.2816299](https://doi.org/10.1109/MCE.2018.2816299)
46. V. P. Yanambaka*, S. P. Mohanty, and E. Kougianos, "Making Use of Semiconductor Manufacturing Process Variations: A Dopingless Transistor Based-PUF for Hardware-Assisted Security", *IEEE Transactions on Semiconductor Manufacturing*, Vol. 31, No. 2, pp. 285–294, May 2018. DOI: [10.1109/TSM.2018.2818180](https://doi.org/10.1109/TSM.2018.2818180)
45. D. Puthal, N. Malik, S. P. Mohanty, E. Kougianos, and C. Yang, "The Blockchain as a Decentralized Security Framework", *IEEE Consumer Electronics Magazine*, Vol. 7, Issue 2, pp. 18-21, March 2018. DOI: [10.1109/MCE.2017.2776459](https://doi.org/10.1109/MCE.2017.2776459)
44. S. P. Mohanty, E. Kougianos, and P. Guturu, "SBPG: Secure Better Portable Graphics for Trustworthy Media Communications in the IoT (Invited Paper)", *IEEE Access Journal*, Vol. 6, pp. 5939-5953, January 2018. DOI: [10.1109/ACCESS.2018.2795478](https://doi.org/10.1109/ACCESS.2018.2795478)
43. P. Sundaravadivel*, E. Kougianos, S. P. Mohanty, and M. Ganapathiraju, "Everything You Wanted to Know about Smart Healthcare: Evaluating the Different Technologies and Components of the Internet of Things for Better Health", *IEEE Consumer Electronics Magazine*, Vol. 7, Issue 1, pp. 18-28, January 2018. DOI: [10.1109/MCE.2017.2755378](https://doi.org/10.1109/MCE.2017.2755378)

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41. S. Joshi*, S. P. Mohanty and E. Kougianos, "Everything You Wanted to Know about PUFs", *IEEE Potentials*, Vol. 36, No. 6, pp. 38-46, November-December, 2017. DOI: [10.1109/MPOT.2015.2490261](https://doi.org/10.1109/MPOT.2015.2490261)
40. C. Yang, D. Puthal, S. P. Mohanty and E. Kougianos, "Big-Sensing-Data Curation for the Cloud is Coming: A Promise of Scalable Cloud-Data-Center Mitigation for Next-Generation IoT and Wireless Sensor Networks", *IEEE Consumer Electronics Magazine*, Vol. 7, No. 4, pp. 48-56, October 2017. DOI: [10.1109/MCE.2017.2714695](https://doi.org/10.1109/MCE.2017.2714695)
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37. V. P. Yanambaka*, S. P. Mohanty, E. Kougianos, D. Ghai, and G. Ghai, "Process Variation Analysis and Optimization of a FinFET based VCO", *IEEE Transactions on Semiconductor Manufacturing*, Vol. 30, No. 2, pp. 126-134, May 2017. DOI: [10.1109/TSM.2017.2669314](https://doi.org/10.1109/TSM.2017.2669314)
36. S. P. Mohanty, U. Choppali and E. Kougianos, "Everything You Wanted to Know about Smart Cities", *IEEE Consumer Electronics Magazine*, Vol. 6, No. 3, pp. 60-70, July 2016. DOI: [10.1109/MCE.2016.2556879](https://doi.org/10.1109/MCE.2016.2556879)
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34. E. Kougianos, S. P. Mohanty, G. Coelho*, U. Albalawi* and P. Sundaravadivel*, "Design of a High Performance System for Secure Image Communication in the Internet of Things" (Invited Paper), *IEEE Access*, Vol. 4, pp. 1222 - 1242, 2016. DOI: [10.1109/ACCESS.2016.2542800](https://doi.org/10.1109/ACCESS.2016.2542800)
33. M. L. Rajaram*, E. Kougianos, S. P. Mohanty and U. Choppali, "Wireless Sensor Network Simulation Frameworks: A Tutorial Review", *IEEE Consumer Electronics Magazine*, Vol. 5, No. 2, pp. 63 - 69, April 2016. DOI: [10.1109/MCE.2016.2519051](https://doi.org/10.1109/MCE.2016.2519051)
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40. O. Garitselov*, S. P. Mohanty, and E. Kougianos, "Fast Optimization of Nano-CMOS Mixed-Signal Circuits Through Accurate Metamodelling", *12th IEEE International Symposium on Quality Electronic Design (ISQED) 2011*, pp. 1-6 , 2011. (**blind review**, 92 regular papers and 34 poster papers accepted out of 290 submissions, **acceptance rate - 43.4%**) DOI: [10.1109/ISQED.2011.5770758](https://doi.org/10.1109/ISQED.2011.5770758)
39. E. Kougianos, S. P. Mohanty and P. Patra "Digital Nano-CMOS VLSI Design Courses in Electrical and Computer Engineering through Open-Source/Free Tools", *IEEE International Symposium on Electronic System Design (ISED) 2010*, pp. 265-270, 2010 (**blind review**, 41 regular papers accepted out of 120 submissions, acceptance rate **34.1%**). DOI: [10.1109/ISED.2010.57](https://doi.org/10.1109/ISED.2010.57)
38. R. S. Bani*, S. P. Mohanty, E. Kougianos, and G. Thakral*, "Design of a Reconfigurable Embedded Data Cache", *IEEE International Symposium on Electronic System Design (ISED) 2010*, pp. 163-168, 2010. (**blind review**, 41 papers accepted out of 120 submissions, **acceptance rate - 34.1%**) DOI: [10.1109/ISED.2010.39](https://doi.org/10.1109/ISED.2010.39)
37. O. Garitselov*, S. P. Mohanty, E. Kougianos and P. Patra, "Nano-CMOS Mixed-Signal Circuit Metamodelling Techniques: A Comparative Study", *IEEE International Symposium on Electronic System Design (ISED) 2010*, pp. 169-174, 2010. (**blind review**, 41 papers accepted out of 120 submissions, **acceptance rate - 34.1%**) DOI: [10.1109/ISED.2010.57](https://doi.org/10.1109/ISED.2010.57)

Design (ISED) 2010, pp. 191-196, 2010. (**blind review**, 41 papers accepted out of 120 submissions, **acceptance rate - 34.1%**) DOI: [10.1109/ISED.2010.44](https://doi.org/10.1109/ISED.2010.44)

36. S. P. Mohanty, D. Ghai*, and E. Kougianos, "A P4VT (Power-Performance-Process-Parasitic-Voltage-Temperature) Aware Dual- V_{Th} Nano-CMOS VCO", in *Proceedings of the 23rd IEEE International Conference on VLSI Design (ICVD) 2010*, pp. 99-104, 2010. (**blind review**, 70 papers accepted out of 320 submissions, **acceptance rate - 21.8%**) DOI: [10.1109/VLSI.Design.2010.15](https://doi.org/10.1109/VLSI.Design.2010.15)

35. E. Kougianos, S. P. Mohanty, and D. K. Pradhan, "SIMULINK Based Architecture Prototyping of Compressed Domain MPEG-4 Watermarking", in *Proceedings of the 12th International Conference on Information Technology (ICIT) 2009*, pp. 10-16, 2009. (**blind review**, 60 papers accepted out of 146 submissions, **acceptance rate - 41.0%**).

34. D. Ghai*, S. P. Mohanty, and E. Kougianos, "Unified P4 (Power-Performance-Process-Parasitic) Fast Optimization of a Nano-CMOS VCO", in proceedings of the *19th ACM/IEEE Great Lakes Symposium on VLSI (GLSVLSI) 2009*, pp. 303-308, 2009 (**blind review**, 34 full papers and 28 short papers accepted out of 215 submissions, **acceptance rate - 29%**). DOI: [10.1145/1531542.1531612](https://doi.org/10.1145/1531542.1531612)

33. D. Ghai*, S. P. Mohanty, E. Kougianos and B. Joshi, "A Universal Level Converter Towards the Realization of Energy Efficient Implantable Drug Delivery Nano-Electro-Mechanical-Systems", *10th IEEE International Symposium on Quality Electronic Design (ISQED) 2009*, pp. 673-679, 2009 (**blind review**, 87 regular papers accepted out of 300 submissions, **acceptance rate - 29%**) DOI: [10.1109/ISQED.2009.4810374](https://doi.org/10.1109/ISQED.2009.4810374)

32. D. Ghai*, S. P. Mohanty, E. Kougianos and P. Patra, "A PVT Aware Accurate Statistical Logic Library for High-k Metal-Gate Nano-CMOS", *10th IEEE International Symposium on Quality Electronic Design (ISQED) 2009*, pp. 47-54, 2009 (**blind review**, 87 regular papers accepted out of 300 submissions, **acceptance rate - 29%**) DOI: [10.1109/ISQED.2009.4810268](https://doi.org/10.1109/ISQED.2009.4810268)

31. S. P. Mohanty, E. Kougianos, W. Cai* and M. Ratnani*, "VLSI Architectures of Perceptual Based Video Watermarking for Real-Time Copyright Protection", *10th IEEE International Symposium on Quality Electronic Design (ISQED) 2009*, pp. 527-534, 2009 (**blind review**, 87 regular papers and 50 poster papers accepted out of 300 submissions, **acceptance rate - 45.7%**) DOI: [10.1109/ISQED.2009.4810350](https://doi.org/10.1109/ISQED.2009.4810350)

30. D. Ghai*, S. P. Mohanty and E. Kougianos, "Variability-Aware Optimization of Nano-CMOS Active Pixel Sensors using Design and Analysis of Monte Carlo Experiments", *10th IEEE International Symposium on Quality Electronic Design (ISQED) 2009*, pp. 172-178, 2009 (**blind review**, 87 regular papers and 50 poster papers accepted out of 300 submissions, **acceptance rate - 45.7%**) DOI: [10.1109/ISQED.2009.4810289](https://doi.org/10.1109/ISQED.2009.4810289)

29. S. P. Mohanty, D. Ghai*, E. Kougianos and P. Patra, "A Combined Packet Classifier and Scheduler Towards Net-Centric Multimedia Processor Design", *27th IEEE International Conference on Consumer Electronics (ICEE) 2009*, pp. 1-2 DOI: [10.1109/ICCE.2009.5012155](https://doi.org/10.1109/ICCE.2009.5012155)

28. Y. -T. Pai, L. -T. Lee, S. -J. Ruan, Y. -H. Chen, S. P. Mohanty, and E. Kougianos, "Honeycomb Model Based Skin Color Detector for Face Detection", in *Proceedings of the 15th International Conference on Mechatronics and Machine Vision in Practice (M2VIP) 2008*, pp. 11-16, 2008 DOI: [10.1109/MMVIP.2008.4749499](https://doi.org/10.1109/MMVIP.2008.4749499)

27. D. Ghai*, S. P. Mohanty and E. Kougianos, "A Process and Supply Variation Tolerant Nano-CMOS Low Voltage, High Speed, A/D Converter for System-on-Chip", in *Proceedings of the 18th ACM/IEEE Great Lakes Symposium on VLSI (GLSVLSI) 2008*, pp. 47-52, 2008 (**blind review**, 40 regular papers accepted out of 220 submissions, **acceptance rate - 18%**). DOI: [10.1145/1366110.1366124](https://doi.org/10.1145/1366110.1366124)
26. D. Ghai*, S. P. Mohanty and E. Kougianos, "Parasitic Aware Process Variation Tolerant Voltage Controlled Oscillator (VCO) Design", in *Proceedings of the 9th IEEE International Symposium on Quality Electronic Design (ISQED) 2008*, pp. 330-333, 2008 (**blind review**, 90 regular papers accepted out of 300 submissions, **acceptance rate - 30%**) DOI: [10.1109/ISQED.2008.4479750](https://doi.org/10.1109/ISQED.2008.4479750)
25. D. Ghai*, S. P. Mohanty and E. Kougianos, "A Dual Oxide CMOS Universal Voltage Converter for Power Management in Multi-V_{DD} SoCs", in *Proceedings of the 9th IEEE International Symposium on Quality Electronic Design (ISQED) 2008*, pp. 257-260, 2008 (**blind review**, 90 regular papers accepted out of 300 submissions, **acceptance rate - 30%**) DOI: [10.1109/ISQED.2008.4479735](https://doi.org/10.1109/ISQED.2008.4479735)
24. E. Kougianos and S. P. Mohanty, "Metrics to Quantify Steady and Transient Gate Leakage in Nanoscale Transistors: NMOS Vs PMOS Perspective", in *Proceedings of the 20th IEEE International Conference on VLSI Design (VLSID) 2007*, pp. 195-200, 2007 (**blind review**, 141 papers accepted out of 444 submissions, **acceptance rate - 31.7%**) DOI: [10.1109/VLSID.2007.107](https://doi.org/10.1109/VLSID.2007.107)
23. S. P. Mohanty and E. Kougianos, "Simultaneous Power Fluctuation and Average Power Minimization during Nano-CMOS Behavioral Synthesis", in *Proceedings of the 20th IEEE International Conference on VLSI Design (VLSID) 2007*, pp. 577-582, 2007 (**blind review**, 141 papers accepted out of 444 submissions, **acceptance rate - 31.7%**) DOI: [10.1109/VLSID.2007.142](https://doi.org/10.1109/VLSID.2007.142)
22. S. P. Mohanty, N. Pati*, and E. Kougianos, "A Watermarking Co-Processor for New Generation Graphics Processing Units", in *Proceedings of the 25th IEEE International Conference on Consumer Electronics (ICCE) 2007*, pp. 303-304, 2007 DOI: [10.1109/ICCE.2007.341552](https://doi.org/10.1109/ICCE.2007.341552)
21. S. P. Mohanty, O. B. Adamo*, and E. Kougianos, "VLSI Architecture of an Invisible Watermarking Unit for a Biometric-Based Security System in a Digital Camera", in *Proceedings of the 25th IEEE International Conference on Consumer Electronics (ICCE) 2007*, pp. 485-486, 2007 DOI: [10.1109/ICCE.2007.341340](https://doi.org/10.1109/ICCE.2007.341340)
20. S. P. Mohanty, E. Kougianos and R. N. Mahapatra, "[A Comparative Analysis of Gate Leakage and Performance of High-K Nanoscale CMOS Logic Gates](#)", in *Proceedings of the 16th ACM/IEEE International Workshop on Logic and Synthesis (IWLS) 2007*, pp. 31-38, 2007.
19. S. P. Mohanty, E. Kougianos, D. Ghai* and P. Patra, "[Interdependency Study of Process and Design Parameter Scaling for Power Optimization of Nano-CMOS Circuits under Process Variation](#)", in *Proceedings of the 16th ACM/IEEE International Workshop on Logic and Synthesis (IWLS) 2007*, pp. 207-213, 2007.
18. S. P. Mohanty, S. T. Vadlamudi* and E. Kougianos, "A Universal Voltage Level Converter for Multi-V_{DD} Based Low-Power Nano-CMOS Systems-on-Chips (SoCs)", *Proceedings of the 13th NASA Symposium on VLSI Design 2007*, CD-ROM Electronic Proceedings paper # 2.2 (7 pages).
17. S. P. Mohanty and E. Kougianos, "Impact of Gate Leakage on Mixed Signal Design and Simulation of Nano-CMOS Circuits", *Proceedings of the 13th NASA Symposium on VLSI Design 2007*, CD-ROM Electronic Proceedings paper # 2.4 (6 pages).

16. D. Ghai*, S. P. Mohanty and E. Kougianos, "A 45nm Flash Analog to Digital Converter for Low Voltage High Speed System on Chips", *Proceedings of the 13th NASA Symposium on VLSI Design 2007*, CD-ROM Electronic Proceedings paper # 3.1 (10 pages).
15. Hai Deng, Murali Varanasi, Kathleen Swigger, Oscar Garcia, Ron Ogan and Elias Kougianos, "Design of Sensor-Embedded Radio Frequency Identification (SE-RFID) Systems", in *Proceedings of the IEEE International Conference on Mechatronics and Automation (ICMA) 2006*, pp. 792-796, 2006 DOI: [10.1109/ICMA.2006.257710](https://doi.org/10.1109/ICMA.2006.257710)
14. S. P. Mohanty, R. Velagapudi*, and E. Kougianos, "Physical-Aware Simulated Annealing Optimization of Gate Leakage in Nanoscale Datapath Circuits", in *Proceedings of the 9th IEEE International Conference on Design Automation and Test in Europe (DATE) 2006*, pp. 1191-1196, 2006 (**blind review**, 233 papers accepted out of 834 submissions, **acceptance rate - 27.9%**) DOI: [10.1109/DAT.2006.244046](https://doi.org/10.1109/DAT.2006.244046)
13. S. P. Mohanty and E. Kougianos, "Steady and Transient State Analysis of Gate Leakage Current in Nanoscale CMOS Logic Gates", in *Proceedings of the 24th IEEE International Conference on Computer Design (ICCD) 2006*, pp. 210-215, 2006 (**blind review**, 72 papers accepted out of 231 submissions, **acceptance rate - 31%**) DOI: [10.1109/ICCD.2006.4380819](https://doi.org/10.1109/ICCD.2006.4380819)
12. S. P. Mohanty and E. Kougianos, "Modeling and Reduction of Gate Leakage during Behavioral Synthesis of NanoCMOS Circuits", in *Proceedings of the 19th IEEE International Conference on VLSI Design (VLSID) 2006*, pp. 83-88, 2006 (**blind review**, 88 regular papers accepted out of 328 submissions, **acceptance rate - 26.8%**) DOI: [10.1109/VLSID.2006.118](https://doi.org/10.1109/VLSID.2006.118)
11. S. P. Mohanty, R. Velagapudi*, and E. Kougianos, "Dual-K Versus Dual-T Technique for Gate Leakage Reduction: A Comparative Perspective", in *Proceedings of the 7th IEEE International Symposium on Quality Electronic Design (ISQED) 2006*, pp. 564-569, 2006 (**blind review**, 93 regular papers accepted out of 256 submissions, **acceptance rate - 36.3%**) DOI: [10.1109/ISQED.2006.52](https://doi.org/10.1109/ISQED.2006.52)
10. O. B. Adamo*, S. P. Mohanty, E. Kougianos, and M. Varanasi, "VLSI Architecture for Encryption and Watermarking Units Towards the Making of a Secure Digital Camera", in *Proceedings of the IEEE International SOC Conference (SOCC) 2006*, pp. 141-144, 2006 (**blind review**, 53 regular papers accepted out of 169 submissions, **acceptance rate - 31.3%**) DOI: [10.1109/SOCC.2006.283868](https://doi.org/10.1109/SOCC.2006.283868)
9. S. P. Mohanty, P. Guturu, E. Kougianos, and N. Pati*, "A Novel Invisible Color Image Watermarking Scheme using Image Adaptive Watermark Creation and Robust Insertion-Extraction", in *Proceedings of the IEEE International Symposium on Multimedia (ISM) 2006*, pp. 153-160, 2006 (**acceptance rate - 35%**) DOI: [10.1109/ISM.2006.7](https://doi.org/10.1109/ISM.2006.7)
8. S. P. Mohanty, E. Kougianos, R. Velagapudi*, and V. Mukherjee*, "Scheduling and Binding for Low Gate Leakage NanoCMOS Datapath Circuit Synthesis", in *Proceedings of the 38th IEEE International Symposium on Circuits and Systems (ISCAS) 2006*, pp. 5291-5294, 2006 (1439 papers accepted out of 2429 submissions, **acceptance rate - 59%**). DOI: [10.1109/ISCAS.2006.1693827](https://doi.org/10.1109/ISCAS.2006.1693827)
7. E. Kougianos and S. P. Mohanty, "Effective Tunneling Capacitance: A New Metric to Quantify Transient Gate Leakage Current", in *Proceedings of the 38th IEEE International Symposium on Circuits and Systems (ISCAS) 2006*, pp. 2937-2940 , 2006 (1439 papers accepted out of 2429 submissions, **acceptance rate - 59%**) DOI: [10.1109/ISCAS.2006.1693240](https://doi.org/10.1109/ISCAS.2006.1693240)

6. V. Mukherjee*, S. P. Mohanty, **E. Kougianos**, R. Allawadhi*, and R. Velagapudi*, "Gate Leakage Current Analysis in READ/WRITE/IDLE States of a SRAM Cell", in *Proceedings of the IEEE Region 5 Technology and Science Conference 2006*, pp. 196-200, 2006 DOI: [10.1109/TPSD.2006.5507432](https://doi.org/10.1109/TPSD.2006.5507432)
5. O. B. Adamo*, S. P. Mohanty, **E. Kougianos**, M. Varanasi, and W. Cai*, "VLSI Architecture and FPGA Prototyping of a Digital Camera for Image Security and Authentication", in *Proceedings of the IEEE Region 5 Technology and Science Conference 2006*, pp. 154-158, 2006 DOI: [10.1109/TPSD.2006.5507440](https://doi.org/10.1109/TPSD.2006.5507440)
4. G. Sarivisetti*, **E. Kougianos**, S. P. Mohanty, A. Palakodety*, and A. K. Ale*, "Optimization of a 45nm CMOS Voltage Controlled Oscillator using Design of Experiments", in *Proceedings of the IEEE Region 5 Technology and Science Conference 2006*, pp. 87-90, 2006 DOI: [10.1109/TPSD.2006.5507456](https://doi.org/10.1109/TPSD.2006.5507456)
3. C. A. Kincaid*, S. P. Mohanty, A. R. Mikler, **E. Kougianos**, and B. Parker*, "A High Performance ASIC for Cellular Automata Applications", in *Proceedings of the 9th IEEE International Conference on Information Technology (ICIT) 2006*, pp. 289-290, 2006 (**blind review**, 96 papers accepted out of 231 submissions, **acceptance rate - 41.5%**) DOI: [10.1109/ICIT.2006.9](https://doi.org/10.1109/ICIT.2006.9)
2. V. Mukherjee*, S. P. Mohanty, and **E. Kougianos**, "A Dual Dielectric Approach for Performance Aware Gate Tunneling Reduction in Combinational Circuits", in *Proceedings of the 23rd IEEE International Conference on Computer Design (ICCD) 2005*, pp. 431-436, 2005 (**blind review**, 101 papers accepted out of 313 submissions, **acceptance rate - 32%**) DOI: [10.1109/ICCD.2005.5](https://doi.org/10.1109/ICCD.2005.5)
1. M. Gill, R. Cleavelin, S. Lin, M. Middendorf, A. Nguyen, J. Wong, B. Huber, S. D'Arrigo, P. Shah, **E. Kougianos**, P. Hefley, G. Santin and G. Naso, "A Novel Sublithographic Tunnel-Diode-Based 5V-Only Flash Memory", *IEDM Digest of Technical Papers*, pp. 119-122, 1990 DOI: [10.1109/IEDM.1990.237212](https://doi.org/10.1109/IEDM.1990.237212)

RESEARCH FUNDING

Award amounts and PI/co-PI recognition are available from the Office of Research and Economic development (ORED) [web site](#).

AWARDED

AGENCY	AMOUNT	PIs	TITLE	DURATION
NSF #1924112	\$247K (Total) (Kougianos, 30%)	S. Mohanty E. Kougianos, and E. Mpfou	Easy-Med: Interdisciplinary Training in Security, Privacy-Assured Internet of Medical Things	09/01/2020-08/31/2023
NSF #1244129	\$199K (Total) \$199K (UNT) \$66.4K (Kougianos, 33%)	Z. Huang, E. Kougianos, and S. Wang	A New Interdisciplinary Technology Education Strategy Using State-of-art Wireless Sensor Network	10/15/2013 - 09/30/2016
Air Force STTR Phase I F15A-T13-0209	\$45K (Total) \$45K (UNT) \$22.5K (Kougianos, 50%)	S. Mohanty and E. Kougianos	Low-Latency Embedded Vision Processor (LLEVS)	08/03/2015 - 04/29/2016
NSF #0942629	\$180K (Total) \$90K (UNT) \$45K (Kougianos, 50%)	E. Kougianos and S. P. Mohanty (UNT), R. Mahapatra (TAMU)	Introduction of Nanoelectronics Courses in Undergraduate Computer Science and Computer Engineering Curricula	5/1/10 - 4/30/13
NSF #0854182	\$250K (Total) \$250K (UNT) \$125K (Kougianos, 50%)	E. Kougianos and S. P. Mohanty	Infrastructure Acquisition for Statistical Power, Leakage, and Timing Modeling Towards Realization of Robust Complex Nanoelectronic Circuits	8/1/09 - 7/31/12
SRC/TxACE #P10883	\$105K (UNT) \$52.5K (Kougianos, 50%)	E. Kougianos and S. P. Mohanty	Fast PVT Tolerant Physical Design of RF IC Components	9/1/09 - 8/31/12
NSF #0702361	\$200K (Total) \$100K UNT \$50K (Kougianos, 50%)	E. Kougianos and S. P. Mohanty (UNT), R. Mahapatra (TAMU)	A Comprehensive Methodology for Early Power-Performance Estimation of Nano-CMOS Digital Systems	9/1/07 - 8/31/10
UNT	\$24K \$6K (Kougianos, 25%)	E. Kougianos, S. P. Mohanty, B. Rout and F. McDaniel	Nanoelectronics Unified Fault Modeling and Experimentation - From Devices to Systems	9/1/08 - 8/31/09
UNT	\$5K	E. Kougianos	Behavioral Tools and Methodologies for Nanotechnology Design Automation	9/1/06 - 8/31/07
UNT	\$5K	E. Kougianos	Stochastic Techniques for the Characterization of VLSI Interconnects	6/1/06 - 8/31/06
IEEE/ACM	\$24K	E. Kougianos	The SPICE Modernization Project	9/1/05 - 8/31/06
Cadence	\$50K	E. Kougianos	Development of Efficient Methodologies and Tools for Analog, Mixed-Signal and RF IC Design	9/1/04 - 8/31/05

COURSES DEVELOPED AND TAUGHT

COURSE	LEVEL	WHERE	TITLE
ENGR 2720	Sophomore	UNT	Digital Logic (+ Lab)
ENGR 2750	Sophomore	UNT	Introduction to Microcontrollers (+ Lab)
ECET 350	Junior	DeVry	Digital Signal Processing (+ Lab)
ECET 360	Junior	DeVry	Operating Systems and Interfacing (+ Lab)

ELET 3750	Junior	UNT	Embedded C Programming (+ Lab)
ELET 3760	Junior	UNT	Design of DSP Systems (+ Lab)
ELET 3970	Junior	UNT	Electronic Devices and Controls (for non-majors, + Lab)
ELET 4300	Senior	UNT	Embedded Systems Organization
ELET 4340	Senior	UNT	Logic Design
ECET 425	Senior	DeVry	Broadband Communications (+ Lab)
ECET 430	Senior	DeVry	Advanced Digital Signal Processing (+ Lab)
ELET 4730	Senior	UNT	Analog/Mixed Signal Electronics (+ Lab)
ELET 4780/4790	Senior	UNT	Senior Design I & II
ELET 4720	Senior	UNT	Control Systems
MSET 5020	Graduate	UNT	Design of Experiments
MSET 5130	Graduate	UNT	Quality Control
MSET 5020	Graduate	UNT	Analog/Mixed-Signal Design (+ Lab)
MSET 5300	Graduate	UNT	Embedded Systems
MSET 5340	Graduate	UNT	Advanced Logic Design with Verilog
EENG 5940	Graduate	UNT	Mixed-Signal Circuit Design
EENG 5940	Graduate	UNT	Embedded Controller Organization
EENG 5940	Graduate	UNT	Digital Logic Circuit Design Techniques

GRADUATE STUDENT DISSERTATION AND THESIS SUPERVISION [Graduated 12 PhDs & 25 MS] - STUDENT LINKEDIN PROFILE HYPERLINKED WHEN AVAILABLE

NAME	DEGREE	ROLE	TITLE	STATUS
M. Shamsa	PhD CE	Co-Major Advisor	TBD	
A. Alkinani	MS CE	Co-Major Advisor	FruitPAL: An IoT-Enabled Framework for Automatic Monitoring of Fruit Consumption in Smart Healthcare	Grad. 12/25 (Exp.)
K. K. Kethineni	PhD CE	Co-Major Advisor	AI for Smart Agriculture	Grad. 12/25 (Exp.)
F. J. Alwuaili	PhD CE	Co-Major Advisor	Cybersecurity in AI-Enabled Smart Systems	Grad. 12/25 (Exp.)
M. Alruwaill	PhD CE	Co-Major Advisor	Blockchain Applications on Smart Cities	Grad. 05/25 (Exp.)
V. K. Bathalapalli	PhD CE	Co-Major Advisor	Hardware-Assisted Sustainable Cybersecurity for Smart Healthcare and Agriculture	Grad. 12/24 (Exp.)
L. S. Vangipuram	PhD CE	Co-Major Advisor	Blockchain Applications for Smart Agriculture	Grad. 05/24 (Exp.)
S. Aarella	PhD CE	Co-Major Advisor	Collaborative Edge Computing for Smart Villages	Grad. 05/24 (Exp.)
A. K. Bapatla	PhD CE	Co-Major Advisor	Blockchain based Solutions for Verifiable Pharmaceuticals	Grad. 05/24 (Exp.)
A. Mitra ¹⁴	PhD CE	Co-Major Advisor	Machine Learning Methods for Data Quality Aspects in Edge Computing Platforms	Grad. 12/23
A. Alkhodair ¹²	PhD CE	Co-Major Advisor	Scalable Next Generation Blockchains For Large Scale Complex Cyber-Physical Systems in Smart Cities	Grad. 08/23
L. Rachakonda ¹¹	PhD CE	Co-Major Advisor	IoMT-Based Accurate Stress Monitoring for Smart Healthcare	Grad. 05/21
I. L. Olokodana	PhD CE	Co-Major Advisor	Kriging Methods to Exploit Spatial Correlations of EEG Signals for Fast and Accurate Seizure Detection in the IoMT	Grad. 08/20
Md. A. Sayeed ¹⁰	PhD CE	Co-Major Advisor	Epileptic Seizure Detection and Control in the Internet of Medical Things (IoMT) Framework	Grad. 05/20
P. V. Yanambaka ⁹	PhD CE	Co-Major Advisor	Exploring Physical Unclonable Functions for Efficient Hardware Assisted Security in the IoT	Grad. 05/19

P. Sundaravadivel ⁸	PhD CE	Co-Major Advisor	Application-Specific Things Architectures for IoT-Based Smart Healthcare Solutions	Grad. 05/18
V. Dhayal	MS CE	Co-Major Advisor	Exploring Simscape Modeling for Piezoelectric Sensor Based Energy Harvester	Grad. 05/17
N. Mukka ⁶	MS CE	Co-Major Advisor	Simulink Based Modeling of a Multi Global Navigation Satellite System	Grad. 08/16
U. A. S. Albalawi ¹³	PhD CE	Co-Major Advisor	New Frameworks for Secure Image Communication in the Internet of Things (IoT)	Grad. 08/16
G. Aluru	MS CE	Co-Major Advisor	Exploring Analog and Digital Design Using the Open-Source Electric VLSI System	Grad. 05/16
S. Joshi ⁵	PhD CE	Co-Major Advisor	Analysis and Optimization of Graphene FET Based Nanoelectronic Integrated Circuits	Grad. 05/16
M. K. Mukka	MS CE	Co-Major Advisor	Simulink based Design and Implementation of a Solar Power Based Mobile Charger	Grad. 05/16
L. Lrmadhu	MS ET	Major Advisor	Comparative Analysis and Implementation of High Data Rate Wireless Sensor Network Simulation Frameworks	Grad. 12/15
A. Hanson	MS CE	Co-Major Advisor	General Purpose Computing in GPU – A Watermarking Case Study	Grad. 08/14
Dr. O. Okobiah ⁷	PhD CE	Co-Major Advisor	Geostatistical Inspired Metamodeling and Optimization of Nanoscale Analog Circuits	Grad. 05/14
Dr. G. Zheng	PhD CE	Co-Major Advisor	Layout-Accurate Ultra-fast System-Level Design Exploration Through Verilog-AMS	Grad. 05/13
M. Gautam	MS CE	Co-Major Advisor	Exploring Memristor Based Analog Design in Simscape	Grad. 05/13
G. Coelho	MS ES	Major Advisor	Qta-Quadrotor: An Object-Tracking Autonomous Quadrotor for Real-time Detection and Recognition	Grad. 05/12
Dr. O. Gariltselov ¹	PhD CE	Co-Major Advisor	Metamodeling-Based Fast Optimization of Nanoscale AMA-SoCs	Grad. 05/12
J. Franco	MS CE	Co-Major Advisor	Rapid Prototyping and Design of a Fast Random Number Generator	Grad. 05/12
Dr. G. Thakral ²	PhD CE	Co-Major Advisor	Process-Voltage-Temperature Aware Nanoscale Circuit Optimization	Grad. 12/10
O. Okobiah	MS CE	Co-Major Advisor	Exploring Process-Variation Tolerant Design of Nanoscale Sense Amplifier Circuits	Grad. 12/10
I. Zarate	MS ES	Major Advisor	Software and Hardware-in-the-Loop Modeling of an Audio Watermarking Algorithm	Grad. 12/10
R. Rastogi ³	MS CE	Co-Major Advisor	A New N-way Reconfigurable Data Cache Architecture for Embedded Systems	Grad. 5/10
S. Rangoonwala	MS ES	Major Advisor	A Verilog 8051 Soft Core for FPGA Applications	Grad. 8/09
Dr. D. V. Ghai ⁴	PhD CE	Co-Major Advisor	Variability-Aware Low-Power Techniques for Nanoscale Mixed-Signal Circuits	Grad. 5/09
J. A. Mendoza	MS ES	Major Advisor	Hardware and Software Codesign of a JPEG2000 Watermarking Encoder	Grad. 12/08
S. Naraharisetti	MS CE	Co-Major Advisor	Region-Aware DCT Domain Invisible Robust Blind Watermarking for Color Images	Grad. 12/08

S. Tarigopula	MS CE	Minor Professor	A CAM Based, High-Performance Classifier-Scheduler for a Video Network Processor	Grad. 5/08
W. Cai	MS ETEC	Major Advisor	FPGA Prototyping of a Watermarking Algorithm for MPEG-4	Grad. 8/07
T. Vadlamudi	MS CE	Co-Major Advisor	A nano-CMOS Based Universal Voltage Level Converter for Multi-V_{DD} SoC	Grad. 8/07
A. Palakodety	MS CE	Co-Major Advisor	CMOS Active Pixel Sensors for Digital Cameras: Current State-of-the-Art	Grad. 5/07
G. Sarivisetti	MS CE	Co-Major Advisor	Design and Optimization of Components in a 45 nm Phase Locked Loop	Grad. 12/06
A. K. Ale	MS CE	Co-Major Advisor	Comparison and Evaluation of Existing Analog Circuit Simulators Using a Sigma-Delta Modulator	Grad. 8/06
O. B. Adamo	MS CE	Minor Professor	VLSI Architecture and FPGA Prototyping of a Secure Digital Camera for Biometric Applications	Grad. 8/06
V. Mukherjee	MS CE	Co-Major Advisor	A Dual Dielectric Approach for Performance Aware Reduction of Gate Leakage in Combinational Circuits	Grad. 5/06
R. Velagapudi	MS CE	Co-Major Advisor	Modeling and Reduction of Gate Leakage During Behavioral Synthesis of Nanoscale CMOS Circuits	Grad. 5/06
H. Liddar	MS ETEC	Major Advisor	Photocurrent Spectroscopy and Photoluminescence of Hybrid Molecular Based Optoelectronic Devices	Grad. 12/05

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² Partially supported by NSF grants #0854182 and #0942629.

³ Recipient of the Outstanding Master's Student in Computer Engineering Award, AY 2009-2010.

⁴ Partially supported by NSF grant #0702361.

⁵ Partially supported by Air Force STTR Phase I Grant # F15A-T13-0209

⁶ Received Outstanding Master's Student in Computer Engineering Award for 2015-2016

⁷ Received Outstanding Ph.D. Student in Computer Science and Engineering Award for 2013-2014. Received scholarship for ACM A.M. Turing Centenary Celebration 2012. Received Scholarship for ACM SIGDA Design Automation Summer School 2011. First Employment: Samsung Semiconductor

⁸ Assistant Professor (tenure-track) in Electrical Engineering, University of Texas at Tyler, Tyler, TX.

⁹ Assistant Professor (tenure-track) in Computer Engineering, Central Michigan University, Mt. Pleasant, MI.

¹⁰ Assistant Professor (tenure-track) in Engineering Technology, Eastern New Mexico University, Portales, NM.

¹¹ Assistant Professor (tenure-track) in Computer Science, University of North Carolina, Wilmington, NC.

¹² Assistant Professor (tenure-track) in Computer Science, University of Tabuk, Saudi Arabia.

¹³ Associate Professor (tenure-track) in Computer Science, University of Tabuk, Saudi Arabia.

¹⁴ Research Assistant Professor in Computer Science, University of Nebraska, Lincoln.

HONORS & AWARDS

- UNT Decker Scholar Award 2017-2019
- *Thank a Teacher* (UNT Provost's Office) recognition in 2012, 2013, 2014, 2015 and 2016.
- 42nd Design Automation Conference (DAC) Fellowship Award, 2005.
- Ron Taylor Award for excellence in teaching, DeVry University, 1999.

PROFESSIONAL ACTIVITIES

- Senior Member IEEE.
- Reviewer for the following journals:
Circuits, Devices and Systems (IET) - Circuits, Systems & Signal Processing (Springer) - Computers and Electrical Engineering (Elsevier) - Defence Technology - Expert Systems with

Applications (Elsevier) - International Journal of Electronics (Taylor & Francis) - International Journal of Numerical Modeling (John Wiley) - Microelectronics Journal (Elsevier) - IEEE Access - IEEE Consumer Electronics Magazine - IEEE Potentials - IEEE Transactions on Circuits and Systems for Video Technology - IEEE Transactions on Computer-Aided Design - IEEE Transactions on Information Forensics and Security - IEEE Transactions on Nanotechnology - IEEE Transactions on VLSI Design - Journal of Emerging Technologies in Computing Systems (ACM) - Journal of Low Power Electronics (ASP) - Semiconductor Science and Technology (IoP) - VLSI Journal (Elsevier)

- Program committee member of the 1st IEEE International Symposium on Nanoelectronics and Information Systems (iNIS) 2015.
- Steering committee member for the 2010, 2011 and 2012 International Symposia on Electronic System Design (ISED).
- Track Chair for the 2010 International Symposium on Electronic System Design (ISED) track on "Analog/Mixed-Signal System Design".
- Web Chair for the 2010 International Symposium on Electronic System Design (ISED).
- Publicity Chair for the 12th International Conference on Information Technology (ICIT) 2009.
- Program committee chair for the "Application-Specific Hardware and Software Systems" track, IEEE International Conference on Information Technology (ICIT) 2006.
- Search chair for a Systems Engineering faculty position (Spring 2009).
- Chair of the committee for the evaluation of a BS in Information Technology program at UNT (Fall 2005 and Spring 2006).
- Graduate coordinator of the Master's in Engineering Systems, Electronics concentration program (2009 – 2018).
- Chair of the Personnel Affairs Committee (PAC) of the Engineering Technology Department (AY 2012-2013).
- Member of the Personnel Affairs Committee (PAC) of the Engineering College (Fall 2013 -Fall Spring 2016).
- Member of the Faculty Council of the Engineering College (Fall 2010 - Spring 2013).
- Member of the Personnel Affairs Committee (PAC) of the Mechanical and Energy Engineering Department (Fall 2010 - Spring 2012).
- Member of the development committee for a Mechatronics program at UNT (2006 – 2007).