CSCE 5610 Computer Systems Architecture
Course Syllabus

Class Meetings: Monday/Wednesday 8:30 am – 9:50 am, NTDP B190
Instructor: Dr. Beilei Jiang
Office: E245J
Office Hours: Tuesday/Thursday 10:00 am – 11:30 am, or by appointment
Email/Phone: beilei.jiang@unt.edu,

TA: Paulson, Elsa
TA Office: Help Lab – F232
TA Office hours: Tuesday/Thursday 12:30pm – 2:30pm
Email: elsapaulson@my.unt.edu

☐ Please include the Class number and Section number in the subject line of emails to me:

CSCE5610-001-YOURNAME

☐ Please give me or TAs a minimum of 24 hours after sending me an email before expecting a response. Please refrain from sending me duplicate emails. Email again if you haven't heard back after 24 hours (weekdays).

Course Objectives

The focus of this course is to improve your understanding of the technology factors, design techniques, architectural innovations and evaluation methods that will determine the form of today's computers. Given that you have basic knowledge of computer system design, this course will introduce more advanced design technologies and will help you build solid foundations in systems/hardware design through programming and simulations.

Prerequisites

CSCE 4610 or equivalent knowledge is required. Fundamental concepts of computer architecture and organization will be necessary for the course. It is helpful to have basic understanding of “Computer Organization and Design” by Hennessy and Patterson. Programming experience in C/C++ will be necessary for the course in order to finish the programming assignments.

Textbook

**Tentative Class Schedule** *(subject to change):*

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<thead>
<tr>
<th>Week</th>
<th>Lecture</th>
<th>Assignments Due</th>
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<tr>
<td>8/29 - 8/31</td>
<td>Fundamentals of Quantitative Design and Analysis</td>
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<td><strong>9/5</strong> - 9/7</td>
<td>Fundamentals of Quantitative Design and Analysis</td>
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<td>9/12 - 9/14</td>
<td>Fundamentals of Quantitative Design and Analysis</td>
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<td>9/19 - 9/21</td>
<td>Fundamentals of Quantitative Design and Analysis</td>
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<tr>
<td>9/26 – 9/28</td>
<td>Memory Hierarchy Design</td>
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<td>10/3 – 10/5</td>
<td>Memory Hierarchy Design</td>
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<td>10/10 – 10/12</td>
<td>Paper presentation</td>
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<td>10/17 – 10/19</td>
<td>Paper presentation</td>
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<tr>
<td>10/24 – 10/26</td>
<td>Instruction-Level Parallelism and Its Exploration</td>
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<tr>
<td>10/31 – 11/2</td>
<td>Instruction-Level Parallelism and Its Exploration</td>
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<td>11/7 – 11/9</td>
<td>Data-Level Parallelism in Vector, SIMD, and GPU Architectures</td>
<td>Final Exam (8:00am-10:00pm)</td>
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<td>11/14 – 11/16</td>
<td>Thread-Level Parallelism</td>
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<td>11/21 – <strong>11/23</strong></td>
<td>Thread-Level Parallelism</td>
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<td>11/28 – 11/30</td>
<td>Project Presentation</td>
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<td>12/5 – 12/7</td>
<td>Project Presentation</td>
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<tr>
<td>12/12 – 12/14</td>
<td>Review, final exam</td>
<td>Final Exam (8:00am-10:00pm)</td>
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**Grading Policy**

Homework/Simulation assignments: 25%

Pop Quizzes (20min): 10%

Exam: 25%

- The exam will be held in class and will be closed book. The exams will test your understanding of the basic ideas and objectives of the class as covered in the course book and the lectures.

Paper Presentation: 10%

Research project: 30%
• Group projects on modern computer architecture
• Several stages to demonstrate progress
• Expected results and performance evaluation
• Topic options will be made available

**Term Project**

There is a three-phase project to be performed by students (organized into teams of two or three members). The goal of this project is for students to gain in-depth knowledge and hands-on experiences on modern computer/AI architecture design. Teams will make presentations of their methods and results in class.

Presentations and Review

• Proposal (~2 pages) – whitepaper with initial references
• Mid-point Progress Report (3 pages) – abstract, list of sub-tasks completed and pending, additional references, plan of experiments
• Final Report (8 including ref pages) – IEEE conference paper format
• Project Presentations

**Late Policy**

Students are strongly encouraged to turn in any assignments on-time. Unless otherwise noted for a particular assignment, the following late policy holds. Late assignments will be penalized by subtracting 15% of the total achievable points of that deliverable, if turned in within the first 24 hours after the due date. Between 24 to 48 hours late turn in will result in a reduction of 30% of the total achievable points.

Certain deliverables may not have ANY LATE day, as announced. Late point reductions cannot be made up by later improvements.

**Academic Integrity**

Unless explicitly noted, all work is to be done on an individual basis. Any violation of the university's guidelines for academic integrity will result in no credit for the course and further disciplinary action.