# A 10 Gbps SerDes For Wireless Chip-to-chip Communication

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***Abstract*— This paper presents a 10 Gbps serializer/deserializer (SerDes) with a phase interpolator (PI) based clock and data recovery (CDR) circuit for high-speed and short-range wireless chip-to-chip communication. The SerDes performs 4:1 muxing and 1:4 demuxing functions. The PI-based CDR uses an 8-phase delay-locked loop (DLL) to produce a set of evenly spaced reference clock phases. The phase vernier, then transforms the 8-phases to sampling clocks for the sampler, which performs 2× oversampling to recover the data from the input signal. Implemented in a 65 nm CMOS process, the proposed SerDes achieves a data rate of 10 Gbps and a recovered peak-to-peak clock jitter of 36.25 ps. The 10 Gbps SerDes occupies an active area of 0.095mm$^2$ and dissipates 88 mW.**

## I. INTRODUCTION

Recently, the Wireless Gigabit Alliance (WiGig) adopted the unlicensed 60 GHz wireless communication as the short distance, high speed wireless communication standard and IEEE announced the IEEE 802.11ad specification for 60 GHz [1]. The 60 GHz wireless communication system is capable of data rates of up to 6–10 Gbps and can satisfy bandwidth demands in portable and consumer applications. The unprecedented access to the unlicensed spectrum and the small size of the transceiver chipset make 60 GHz very attractive for many potential applications requiring ultra low power and low latency. The block diagram of a 60 GHz transceiver chipset is shown in Fig. 1. One of the challenges in the design of energy-efficient 60 GHz chipset is the implementation of a serializer and deserializer (SerDes) that can provide robust performance with low power dissipation, while maintaining a small area, low complexity, and low bit-error-rates. The power and performance of a SerDes are dependent on the clock and data recovery (CDR) circuit [2-6]. In this paper, a low-power and low-jitter SerDes for wireless chip-to-chip communication that uses a phase interpolator (PI) based digital CDR is presented.

## II. PROPOSED SERDES ARCHITECTURE WITH A PI-BASED CDR

Fig. 2 shows the block diagram of the proposed SerDes. Fig. 2(a) shows the serializer that consists of a 4-to-2 MUX and a 2-to-1 MUX. The serializer converts the 4-bit 2.5 Gbps/pin parallel data into a single 10 Gbps/pin serial data stream and send it to the RF transmitter.

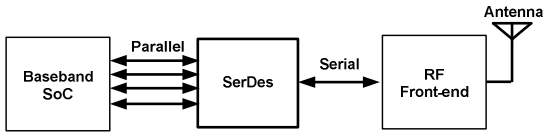
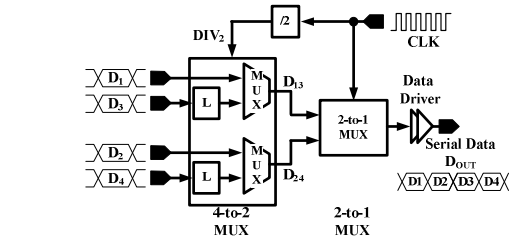
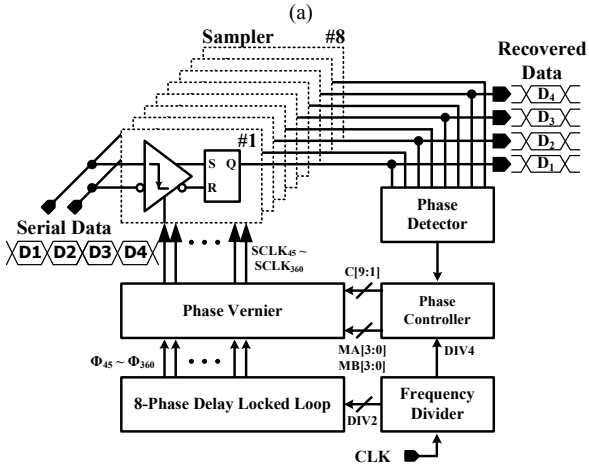



Fig. 1 Wireless chip-to-chip communication chipset with a SerDes




(a)




(b)

Fig. 2. Block diagram of the proposed SerDes (a) Serializer (b) Deserializer (= digital CDR with 4-bit demultiplexed parallel output data)

Fig. 2(b) shows the block diagram of the proposed deserializer, which is actually a digital CDR with 4-bit

demultiplexed parallel output data. This PI-based CDR consists of eight data receiving samplers, a phase detector, a phase controller, a frequency divider, a phase vernier, and a 8-phase DLL. The DLL generates four differential (8 phases, Φ45~Φ360) 2.5Ghz clock signals and there are four phase verniers. Each vernier select two adjacent clock signals (out of 8 phase clocks) depending on the control codes (MA[3:0], MB[3:0], C[9:1]) of the phase controller. The phase vernier consists of two multiplexers and a phase interpolator for providing infinite phase rotation. Consequentially, the phase vernier provide 8-phase sampling clocks (SCLK45 ~ SCLK360) for the eight samplers to recover the data from the input signal using 2× oversampling.

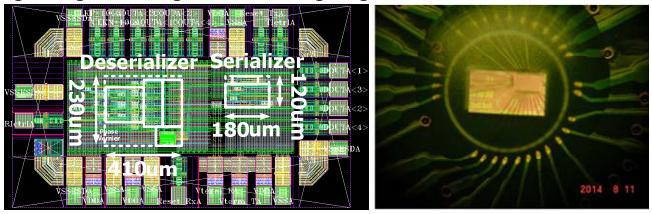



Fig. 3. Layout and chip microphotograph of the proposed SerDes

## III. Experimental Results

The proposed SerDes was implemented in a 65 nm CMOS process and tested in a chip-on-board assembly. Fig. 3 shows the chip layout and the microphotograph of the proposed SerDes which occupies an active area of 0.095mm$^2$. Fig. 4 shows the measured 4-bit data recovered with a PRBS-7 pattern.

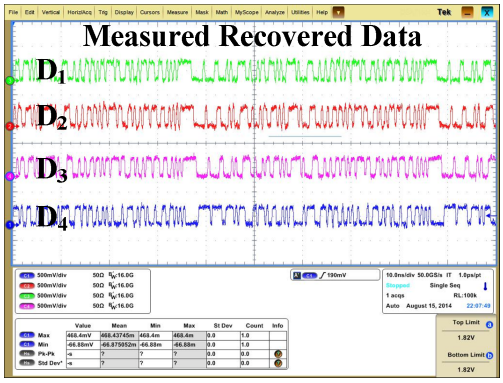
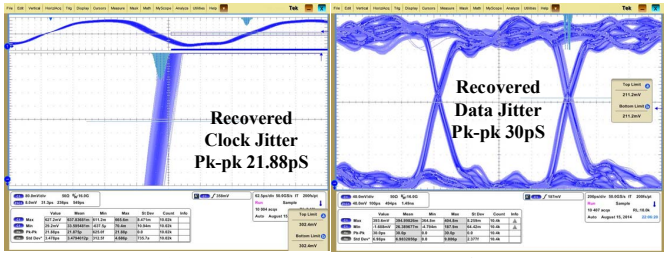



Fig. 4. Measured recovered data (2.5 Gbps × 4)




(a) (b)

Fig.5. Measured peak-to-peak jitter (a) Recovered clock (b) Recovered data

Fig. 5 displays the measured jitter of the recovered clock and the eye diagram of the recovered data, respectively. The peak-to-peak jitter of the clock is 21.88 ps and the peak-to-peak jitter of the data signal is 30 ps. The estimated BER is 1e-28 at 10 Gbps. Compared with previous CDRs shown in Table I, the proposed PI-based digital CDR achieves highest figure-of-merit (FOM) in terms of power dissipation, die area and data rate. The FOM is defined as follows.

FOM = power dissipation(mW)×area(mm$^2$) / data rate(Gbps)

## IV. Conclusion

A low-power 10 Gbps SerDes is presented that uses a PI-based digital CDR for energy-efficient short-range wireless chip-to-chip communication. The DLL-based phase-interpolating CDR performs 2× oversampling to recover the data from the input signal. Implemented in a 65 nm CMOS process, the proposed SerDes achieves a measured data rate of 10 Gbps and a recovered peak-to-peak clock jitter of 21.88 ps. The SerDes occupies an active area of only 0.095mm$^2$ and the CDR dissipates 6.8 mW/Gbps.

## Acknowledgment

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TABLE I. Performance Comparison Table

| | TCASII 2013 [3] | VLSI 2013 [4] | JSSC 2007 [5] | JSSC 2011 [6] | This work |
|---|---|---|---|---|---|
| Tech | 90nm | 90nm | 0.11µm | 0.13µm | 65nm |
| Supply | 1.2v | 1v | 1.2v | 1.2v | 1.2v |
| CDR Architecture | PLL-based | PLL-based | Oversampling | PI-based | PI-based |
| CDR DEMUX | 1:1 | 1:1 | 1:1 | 1:4 | 1:4 |
| Data Rate (Gbps) | 12.5 | 5 | 3.2 | 5 | 10 |
| Power Consumption (mW) | 84 | 13.1 | 115 | 18.2 | Ser : 20<br>Des : 68 |
| CDR Bit energy (mW/Gbps) | 6.72 | 2.62 | 35.9 | 3.64 | 6.8 |
| Recovered Clock Jitter (Pk-pk) | - | 44pS | - | 52.22pS | 21.88pS |
| Chip Area (mm$^2$) | 0.823 | 0.62 | 0.15 | 0.4 | 0.095 |
| FOM | 5.531 | 1.625 | 5.385 | 1.456 | 0.646 |

## References

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