Development of undervoltage lockout (UVLO) circuit configured Schmitt trigger

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Abstract—CMOS under-voltage lockout (UVLO) circuit configured Schmitt trigger was fabricated and tested. The UVLO circuit consists of current source inverter, Schmitt trigger, delay circuit, and waveform shaper of the output. The tested result shows that the UVLO has size of die was 136 µm x 85 µm, turn on and off voltage was at 1.85V and 1.70V, respectively. The fabrication process was Magna/Hynix CMOS 0.35 µm process and supply voltage was 3.3V. Power dissipation of the UVLO was 0.18mW.

Keywords- UVLO, schmitt trigger, currentsource inverter

I. INTRODUCTION

Many systems may employ an under-voltage lockout (UVLO) circuit to prevent operation of system circuits during under-voltage condition. Many circuits are sensitive to fluctuations in supply voltage. More particularly, when the supply voltage decrease below a minimum specified operating voltage, an under-voltage condition may occur. Some circuits may either be damaged or they may exhibit unpredictable operation when operation may be especially such as microprocessors, microcontrollers, and digital signal processors, for example [1].

Figure 1 shows one of the conventional UVLO circuit with bandgap structure. For the bandgap structure using NPN transistors, the circuit can’t be used in standard CMOS processes.

Resistors R₁, R₂ and diode-connected M₁ form a V₁, threshold reference, generating a reference voltage Vᵣ. N-channel transistors M₄ and M₅ have same W/L ratio, forming a current mirror. Transistors M₂ and M₃ make up an inverter with current source load. Transistors M₆~M₉ form a Schmitt trigger. M₁₀~M₁₂ form a delay circuit to prevent the UVLO circuit enable from an acceptable ripple in supply voltage. M₁₀ was designed to have large L/W ratio to get large R_DSON. When UVLO occurs, the gate of M₁₂ is getting high slowly for the large R_DSON of M₁₀. The delay circuit acts as a low-pass filter. BUFI and BUF2 shape the waveform of the output enable signal UVLO. M₁₃ acts as a switch to alter the resistance load of reference generator so as to realize hysteretic threshold[5].

Unfortunately, these conventional implementations of UVLO circuits may utilize a relatively large amount of circuitry and thus layout area. This also may consume a relatively large amount of power during operation.

In this paper, we had fabricated and tested UVLO circuit using CMOS standard process for small chip size and low power systems.

II. CIRCUIT DESCRIPTION

Figure 2 shows the fabrication and verification of UVLO circuit. The UVLO circuit consists of current source inverter, Schmitt trigger, delay circuit, and waveform shaper of the output.
Hysteretic threshold is realized by changing the load resistance of the reference generator. When \( V_{DD} \) is above \( V_{TH} \) the gate of control transistor \( M_{13} \) is high, \( M_{13} \) is cutoff.

\[
V_{RH} = V_{TN2} - \frac{1}{K_{X2}R_2} + \frac{2(V_{DD} - V_{TN2})}{K_{X2}(R_1 + R_2)} + \frac{1}{K_{X2}^2(R_1 + R_2)^2} \tag{1}
\]

When supply voltage \( V_{DD} \) is below \( V_{TH} \) the gate of control transistor \( M_{13} \) is low, \( M_{13} \) is turned on. Neglecting the \( R_{DS(ON)} \).

\[
V_{BH} = V_{TN2} - \frac{1}{K_{X2}R_2} + \frac{2(V_{DD} - V_{TN2})}{K_{X2}(R_1 + R_2)} + \frac{1}{K_{X2}^2R_2^2} \tag{2}
\]

The hysteretic threshold is realized as shown in Equation (4). It can be concluded that hysteresis range is determined by \( R_1 \).

\[
\Delta V_{TH} = V_{THH} - V_{THL} = (1 + \sqrt{\frac{K_{X2}}{K_{P3}}})(V_{RH} - V_{RL}) \tag{3}
\]

III. SIMULATIONS AND MEASUREMENTS RESULTS

The developed UVLO circuits shown in Fig 2 simulated with Cadence the full parameters of Magna/Hynix CMOS 0.35 \( \mu m \). The value of the device are set by \( V_{DD} = 3.3V \), \( R_1 = 50k\Omega \), \( R_2 = 50k\Omega \).

Figure 3 was simulation result of the UVLO circuit. The change in the output voltage of supply voltage. The simulation result shows that the UVLO turn on at 1.84V and turn off at 1.65V. The hysteresis range was 190mV.

IV. CONCLUSION AND FUTURE SUBJECT

UVLO circuit configured Schmitt trigger was development. The simulation result shows that the UVLO turn on at 1.84V and turn off at 1.65V. The measuring result shows that the UVLO turn on at 1.85V and turn off at 1.70V. The designed UVLO circuit simulation and layout was used as the Magna/Hynix 0.35 \( \mu m \) process and supply voltage was 3.3V. Hysteresis threshold range is 150mV. In the future, we will register the IP.

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REFERENCES