# GS1011M

## LOW-POWER WIRELESS SYSTEM-ON-CHIP WI-FI MODULE

## *DATA SHEET*

**PRELIMINARY RELEASE**



***GainSpan Confidential Information***

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|---|---|---|
| 0.7 | | Initial release. |

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# 1 Overview

## 1.1 Document Overview

THIS DOCUMENT describes the GS1011Mxx Low Power module hardware specification. The GS1011 based module provides a cost effective, low power, and flexible platform to add Wi-Fi® connectivity for embedded devices for a variety of applications, such as wireless sensors and thermostats. It combines ARM7-based processors with an RF transceiver, 802.11 MAC, security, & PHY functions, FLASH and SRAM, onboard and off module certified antenna options, and various RF front end options for end customer range needs in order to provide a WiFi and regulatory certified IEEE 802.11 radio with concurrent application processing services for variety of applications, while leverage existing 802.11 [1] wireless network infrastructures.

## 1.2 Product Overview

- Family of modules with different antenna and output power options:
  - GS1011MIx 1.280 inches by 0.900 inches by 0.143 inches (Length * Width * Height) 48-pin Dual Flat pack PCB Surface Mount Package.
  - GS1011MEx 1.450 inches by 0.900 inches by 0.143 inches (Length * Width * Height) 48-pin Dual Flat pack PCB Surface Mount Package.
  - Single hardware covers low power and extended range options (see section 6 Ordering Information
  - Simple API for embedded markets covering large areas of applications
- Compliant with IEEE 802.11and regulatory domains:
  - DSSS modulation for data rate of 1 Mb/s and 2 Mb/s; CCK modulation rates of 5.5 and 11 Mb/s.
  - Compatible with IEEE 802.11b/g/n.
  - Supports short preamble and short slot times.
  - WiFi Certified Solution (WFA ID=TBD)
    - Supports 802.11i security
      - WPA™ - Enterprise, Personal
      - WPA2™ - Enterprise, Personal
      - Vendor EAP Type(s)
        - EAP-TTLS/MSCHAPv2, PEAPv0/EAP-MSCHAPv2, PEAPv1/EAP-GTC, EAP-FAST, EAP-TLS
  - High-throughput hardware AES and RC4 encryption/decryption engines.
  - RoHS and CE compliant
  - FCC Certified (USA, FCC ID: TBD)
  - IC Certified (IC: TBD)
  - Fully compliant with EU & meets the R&TTE Directive for Radio Spectrum
  - Japan Radio Type Approval pre-scan compliant
- Dual ARM7 Processor Platform:
  - 1st ARM7 processor (WLAN CPU) for WLAN software

- 2nd ARM7 (APP CPU) for networking software
- Based on Advanced Microprocessor Bus Architecture (AMBA) system:
  - AMBA High-Speed Bus (AHB).
  - AMBA Peripheral Bus (APB).
- On-chip WLAN boot code located in dedicated boot ROM.

► Interfaces:
- PCB or external antenna options.
- Two general-purpose SPI interfaces (each configurable as master or slave) for external sensors, memory, or external CPU interface; one interface may be configured as a high-speed Slave-only.
- Two multi-purpose UART interfaces.
- Up to 23 configure able general purpose I/Os.
- Single 3.3V supply option
  - I/O supply voltage 1.8 ~ 3.3V option
- One PWM output
- $I^2C$ master/slave interface.
- Two 10-bit ADC channels, aggregate sample rate 32 kS/s.
- Two alarm inputs to asynchronously awaken the chip.
- Support of up to two control outputs for power supply and sensors.

► Embedded RTC (Real Time Clock) can run directly from battery.

► Power supply monitoring capability.

► Low-power mode operations

► Sleep, Deep Sleep, and Standby

# 2 Architecture

## 2.1 G1011Mxx Block Diagram

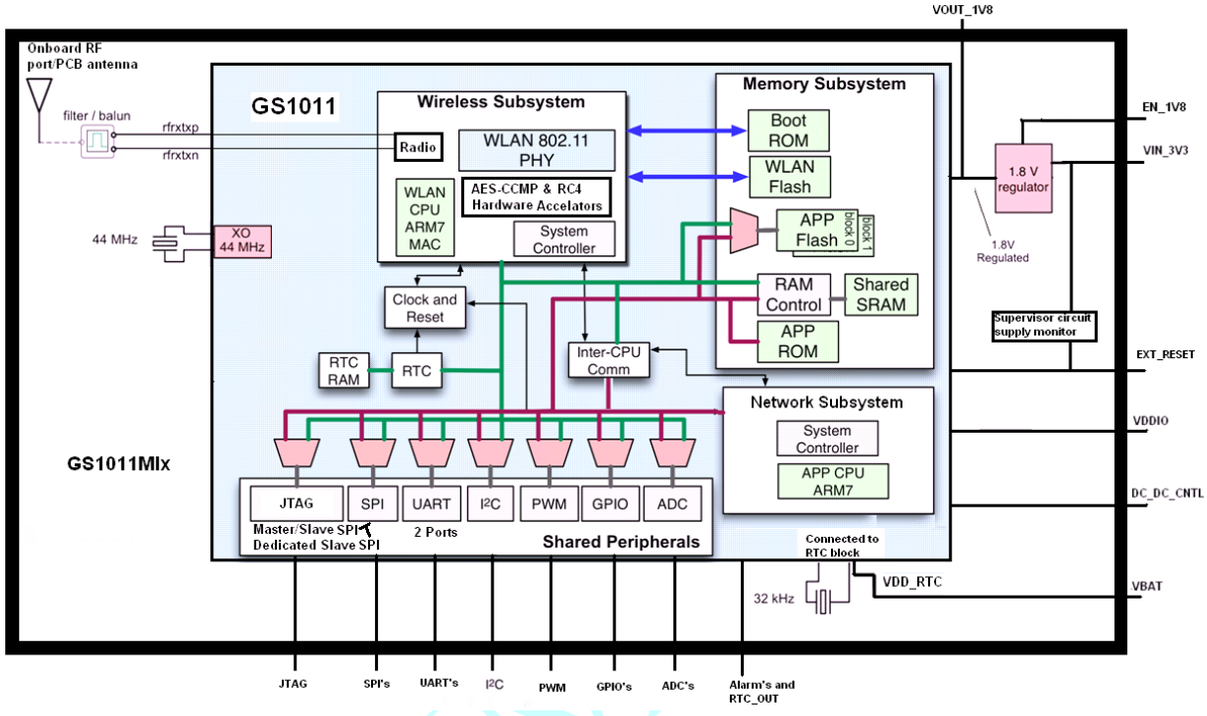


**Figure 2-1: GS1011MIx Block Diagram**

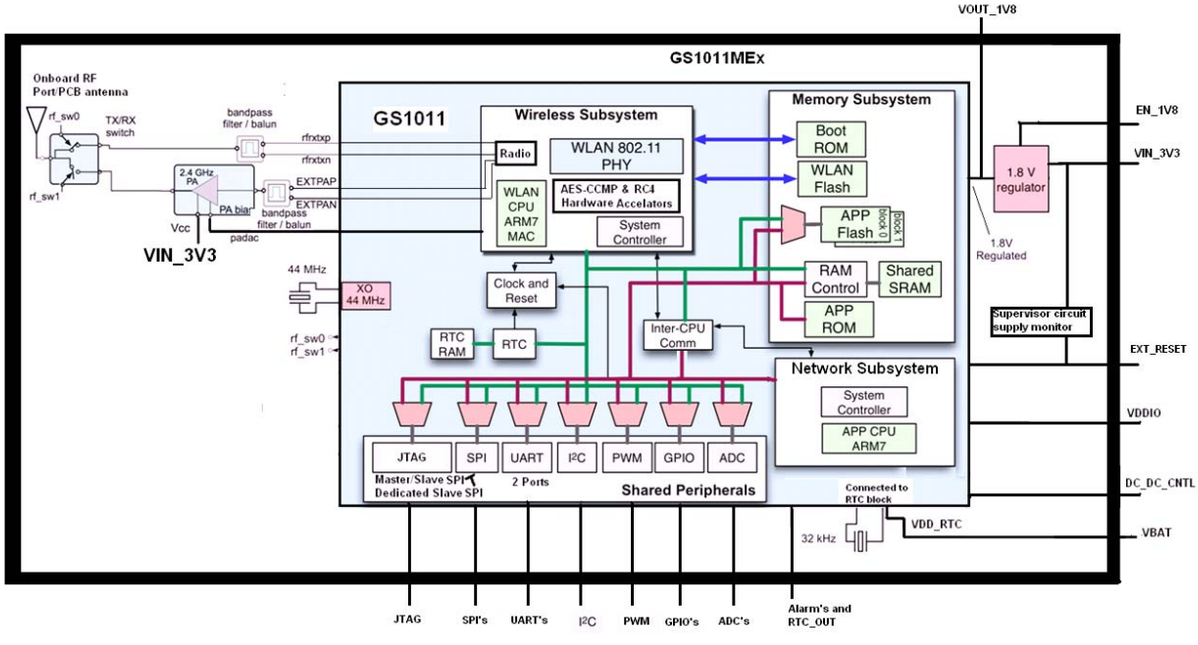


**Figure 2-2: GS1011MEx Block Diagram**

## 2.2 Block Diagram Description

### 2.2.1 Overview

GS1011Mxx module is a highly integrated ultra low power Wi-Fi system-on-chip (SOC) that contains the following:

- The module includes GS1011 SoC, which contains media access controller (MAC), baseband processor, security, on-chip flash memory and SRAM, and an applications processor in a single package.
- The module contains two ARM7-based processors, one dedicated to Networking Subsystems, and the other dedicated to Wireless Subsystems.
- The module carries an 802.11 radio with onboard 32 KHz & 44 MHz crystal circuitries, RF, and certified PCB antenna or external antenna options.
    - The low power module option has a capability of +9dBm output power at the antenna (see Figure 2-1).
    - The extended range module option has a capability of +17dBm output power at the antenna (see Figure 2-2).
- Variety of interfaces are available such as two UART blocks using only two data lines per port with optional hardware flow controls, two SPI block (one dedicated as a serial slave with configurable hardware interrupt to the HOST), $I^2C$ with Master or slave operation, JTAG port, low-power 10-bit ADC capable of running at up to 32 Ksamples/Sec., GPIO's, and LED Drivers/GPIO with 20mA capabilities.
- GS1011Mxx contains single power supply (VIN_3V3) with optional module controlled external regulator enable control pin (DC_DC_CNTL), a separate I/O supply (VDDIO) that can be tied to the HOST supply rail without the use of external voltage translators, Real Time Clock (RTC) with battery supply monitor option (VBAT), and two external alarm inputs enable wake-up of the system on external events & outputs (ALARM and RTC_OUT) to enable periodic wake-up of the remainder of the system.
    - The Module carries onboard single supply monitor for under voltage supply and onboard 1.8V regulator with enable/disable capabilities for power critical applications.

### 2.2.2 Wireless Subsystem

The Wireless subsystem provides the WLAN PHY, MAC and baseband functionality. It contains the WLAN CPU, a 32-bit ARM7 TDMI-S core running at up to 44 MHz. It includes an IEEE 802.11b/g -compatible RF transceiver, which supports Direct Sequence Spread Spectrum (DSSS) 1 Mb/s and 2 Mb/s data rates, and Complementary Code Keyed (CCK) 5.5 Mb/s and 11 Mb/s data rates. The WLAN subsystem includes an integrated power amplifier, and provides management capabilities for an optional external power amplifier. In addition, it contains hardware support for AES-CCMP encryption (for WPA2) and RC4 encryption (for WEP & WPA/WPA2 TKIP) encryption/decryption.

The WLAN subsystem contains the control logic and state machines required to drive the low power DSSS modem, and perform pre-processing (in transmit mode) or post-processing (in receive mode) of the data stream. The WLAN subsystem manages DMA accesses, data encryption/decryption using the AES algorithm, and CRC computation.

#### 2.2.2.1 Onboard antenna / RF port / Radio

The GS1011Mxx modules have fully integrated RF frequency synthesizer, reference clock, low power PA, and high power PA for extended range applications. Both TX and RX chain in the module incorporate internal power control loops. The GS1011Mxx modules also incorporate onboard printed antenna option plus a variety of regulatory certified antenna options for various application needs.

### 2.2.3 Network Subsystem

#### 2.2.3.1 APP CPU

The APP CPU is an ARM7 TDMI-S. It incorporates an AHB interface and a JTAG debug interface. The network RTOS, network stack, and customer application code can reside on this CPU. For more information, consult the GS1011 Peripheral and Register Description [2] and GS1011 IC data sheet [3] for detailed descriptions.

### 2.2.4 Memory Subsystem

#### 2.2.4.1 Overview

The GS1011 Chip contains several memory blocks:

- Boot ROM blocks.
  - The software contained in this ROM provides the capability to download new firmware via the SPI Slave or UART interfaces and to control the update of WLAN and APP Flash Memory.
- 384 KBytes of Embedded Flash to store program code.
  - Three embedded Flash blocks of 128K bytes each
    - WLAN Flash (contains the WLAN Software)
    - APP Flash 0 and 1 (contain the Network/Application Software)
- 128 KBytes of RAM shared between the two integrated CPU's.
- 512 bytes of RTC memory ((retains data in all states including Standby, as long as the battery or other voltage supply is present)

For more information, consult the GS1011 Peripheral and Register Description [2] and GS1011 IC data sheet [3] for detailed descriptions.

### 2.2.5 Clock Circuitries

The GS1011MXX architecture uses a low-power oscillator (i.e. 32 kHz) to provide a minimal subset of functions when the chip is in its low-power Standby mode, and a high-speed 44 MHz oscillator to provide clock signals for the processors, bus, and interfaces during active operation. Intermediate modes of operation, in which the 44 MHz oscillator is active but some modules are inactive, are obtained by gating the clock signal to different subsystems. The Clock & Reset Controller, within the device, is responsible for generation, selection and gating of the clocks used in the module to reduce power consumption in various power states.

### 2.2.5.1 Real Time Clock (RTC)

### 2.2.5.2 Overview

To provide global time (and date) to the system, the GS1011MXX Chip is equipped with a low-power Real Time Clock (RTC).

RTC key features include:

- 32.768 kHz crystal support.
- Two external alarm inputs to wake up the device.
- Two programmable periodic outputs (one for a DC/DC regulator and one for a sensor).
- Embedded 128x32 non-volatile (battery-powered) RAM.
- Embedded Power On Reset.
- Real Time Counter (48 bits; 46 bits effective).

An overview of RTC block diagram is shown in Figure 2-3. The RTC contains a low-power oscillator that can use 32.768 kHz crystals. In normal operation the RTC is always powered up, even in the Stand-by state (see Figure 2-8).

Two programmable embedded alarm counters (wrap-around) are provided to enable periodic wake-up of the remainder of the system, and one independent external component (typically a sensor). Two external alarm inputs enable wake-up of the system on external events. The global times are recorded on each external event and if the system is in the Power-ON state (see Figure 2-8), an interrupt is provided. The RTC includes a Power-On Reset (POR) circuit, to eliminate the need for an external component. The RTC contains low-leakage non-volatile (battery-powered) RAM, to enable storage of data that needs to be preserved while in Standby.

Total current consumption of the RTC in the worst case is typically less than 5 µA without data storage, using the 32.768 kHz oscillator.

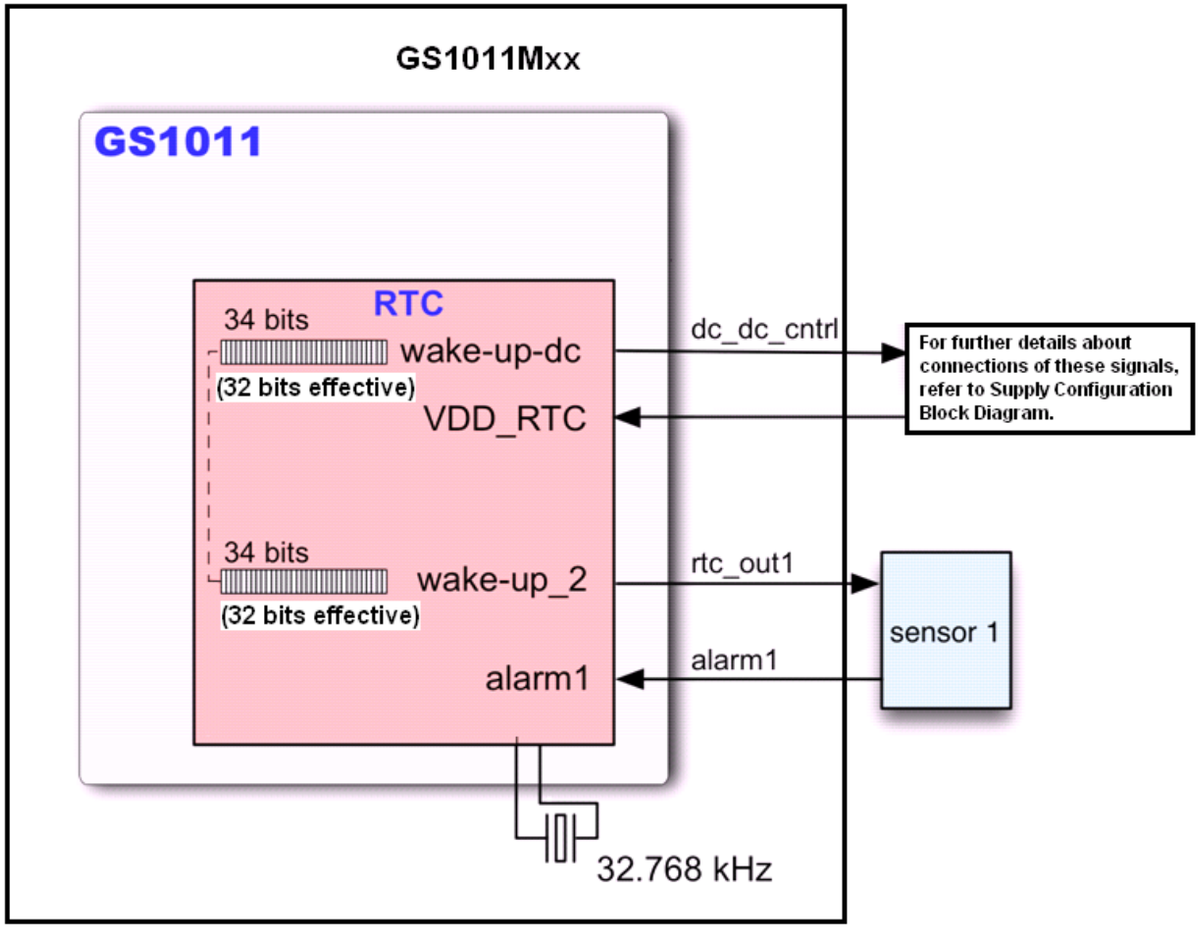


**Figure 2-3: RTC Interface Diagram**

Resolution of the wake-up timer is one clock cycle, and, with onboard 32KHz. CLK, each 32bit effective register can provide up to 1.5 days worth of standby duration as the longest standby period. Polarity of the rtc_out1 pin is programmable.

### 2.2.5.3 Real Time Counter

The Real Time Counter features:

- 48-bit length (with absolute duration dependent on the crystal frequency used).
- Low-power design.

This counter is automatically reset by power-on-reset.

This counter wraps around (returns to “all-0” once it has reached the highest possible “all-1” value).

### 2.2.5.4 RTC Outputs

There are two RTC outputs (dc_dc_cntl and rtc_out1) that can be used to control external devices, such as sensors or voltage regulators. For more information, consult the GS1011 Peripheral and Register Description [2] and GS1011 IC data sheet [3] for detailed descriptions.

#### 2.2.5.4.1 DC_DC_CNTL

During Power-on-Reset (e.g. when the battery is connected), the dc_dc_cntl pin is held low; it goes high to indicate completion of RTC power-on-reset. This pin can be used as an enable into an external device such as voltage regulator. For more information, consult the GS1011 Peripheral and Register Description [2] and GS1011 IC data sheet [3] for detailed descriptions.

#### 2.2.5.4.2 RTC_OUT1

The rtc_out1 signal can be disabled or driven by the Wake-up Counter 2. This counter is 34 bits long, and operates in the same fashion as Wake-up Counter 1. The rtc_out1 signal can be configured to output the low-power crystal oscillator clock (i.e. the 32 kHz clock) instead of a simple state transition. Wake-up Counter 2 is automatically reset at Power-on-Reset. For more information, consult the GS1011 Peripheral and Register Description [2] and GS1011 IC data sheet [3] for detailed descriptions.

### 2.2.5.5 RTC Alarm Inputs 1 and 2

The RTC inputs alarm1 and alarm2 operate as follows:

- dc_dc_cntl is set to "1" (typically enabling the power supply to the rest of the GS1011) whenever either of these inputs changes state.
- The RTC counter value is stored each time either of these inputs changes state.

The inputs alarm1 and alarm2 have programmable polarity. Their task is to wake up the system (by setting dc_dc_cntl output pin to "1") when an external event occurs. For more information, consult the GS1011 Peripheral and Register Description [2] and GS1011 IC data sheet [3] for detailed descriptions.

## 2.3 Peripherals

Note: For register identification and additional details on the use of shared peripherals, refer to the GS1011MXX Peripheral and Register Description [3].

### 2.3.1 SPI

There are two general-purpose SPI interfaces (each configurable as master or slave) for external sensors, memory, or external CPU interface; one interface may be configured as a high-speed Slave-only. The master SPI block provides dual synchronous serial communication interfaces. The Master SPI block can be used in one of two modes of operations: as a serial master or a serial slave. Each block provides synchronous serial communication with slave or master devices, using one of the following protocols:

- Motorola Serial Peripheral Interface (SPI).
- Texas Instruments Synchronous Serial Protocol (SSP).
- National Semiconductor Microwire Protocol.

Only Motorola Serial Peripheral Interface (SPI) timing is shown in this data sheet; however, National Semiconductor Microwire Protocol or Texas Instruments Synchronous Serial Protocol (SSP) modes are certainly supported. The SPI interface can also be used to access non-volatile external memory, such as an EEPROM block. The interface uses the SPI master mode to allow easy connection to industry-standard EEPROMs.

The shared SPI blocks provide the following general features:

- 32-bit AMBA APB interface to allow access to data, control, and status information by the host processor.
- Full-duplex serial-master or serial-slave operation.

- Two clock design:
  - APB bus clock for bus interface and registers.
  - Serial input clock for core logic.
- Support of external EEPROM or other non-volatile memory.
- Programmable choice of Motorola SPI, Texas Instruments Synchronous Serial Protocol or National Semiconductor Microwire.
- Programmable control of the serial bit rate of the data transfer in serial-master mode of operation.
- Programmable phase and polarity of the bit rate clock.
- Programmable transfer modes to perform transmit and receive, transmit only, receive only and EEPROM read transfers.
- Programmable data word size (8, 16, 24 & 32 bits) for each data transfer.
- Transmit and receive FIFO buffer depth 8 words (of the selected size).
- Configurable number of slave select outputs in serial-master mode of operation: 1 to 4 serial slave-select output signals can be generated.
- Combined interrupt line with independent masking of interrupts.
- Transmit FIFO overflow, transmit FIFO empty, transmit FIFO underflow, receive FIFO full, receive FIFO underflow, receive FIFO overflow, and receive FIFO timeout interrupts.
- Transmit FIFO empty and receive FIFO full interrupts provide programmable threshold values.

Both SPI blocks are configured to provide a FIFO depth of four entries.

The SPI master interface can be used to access external sensor devices, and EEPROM containing system parameters, under software control. The main purpose of the SPI slave interface is to provide control of the GS1011MXX from an external CPU.

SPI chip select (MPSISI_CS0 or MPSI_CS1) signals frame each data word. If the chip select is required to remain asserted for multiple data words, then a GPIO pin should be used for the chip select instead of the SPI chip select signals. For clock architecture and rates, please refer to section 7.1 Clock Architecture of GS1011 Peripheral and Register Description [2]. For other SPI Interface Timing, please refer to section 4.7.

### 2.3.2 $I^2C$

The $I^2C$ block provides a two-wire $I^2C$ serial interface. It provides the following features:

- 32-bit AMBA APB interface to allow access to data, control, and status Information by the host processor.
- Serial 2-wire $I^2C$ bus, compliant to the $I^2C$ Bus Specification Version 2.1.
- Supports only one transfer in Standard mode (100 Kb/s) and fast speed mode with a bit rate of up to 392 Kb/s.
- Supports Multi-Master System Architecture through $I^2C$ bus SCL line Synchronization and Arbitration.
- Transmitter and Receiver: The $I^2C$ block can act as the Transmitter or Receiver depending on the operation being performed.
- Master or slave $I^2C$ operation.
- 7- or 10-bit addressing.

- Ignores CBUS addresses (an older ancestor of $I^2C$ that used to share the $I^2C$ bus).
- Interrupt or polled mode operation.
- Combined interrupt line triggered by:
  - Tx FIFO not FULL.
  - Rx FIFO not EMPTY.
  - Rx FIFO FULL (can be used to transfer data by host interface in bursts).
  - Tx FIFO EMPTY (can be used to transfer data by host interface in bursts).
  - Rx FIFO OVER RUN.
  - Master mode to Slave Transfer Request.
  - Slave Transmit Request.
  - Break Interrupt (master mode): No Acknowledge received from slave for slave address or write data.
- Digital debounce logic for the received SDA and SCL lines.
- Hold Delay Insertion on SDA line.

### 2.3.3 UART

The GS1011MXX includes two UART blocks. Each UART block provides an asynchronous communication interface, using only two data lines: Rx data and Tx data. Hardware flow control using RTS/CTS signaling is provided as an option. The UART is a standard asynchronous serial interface, 16450/16550 compatible. It provides the following features:

- Operation in full-duplex mode.
- All standard bit rates up to 921.6 kbps are supported.
- RTS/CTS flow control handshake (standard 16550 approach).
- 5, 6, 7 and 8-bit character format.
- 1 or 2 stop bits (1.5 in case of a 5-bit character format).
- Parity bit: none, even, odd, mark, or space.
- 16-byte Rx and 16-byte Tx FIFOs.

The UART Serial port can be used to communicate with a PC or other devices, for debug or additional functionality.

### 2.3.4 JTAG

The JTAG ports facilitate debugging of the board and system designs. This block has the following features:

- Compliant to IEEE-1149.1 TAP ports.
- One JTAG boundary scan TAP port.
- One set of JTAG pins, which support the following mode of operation:
  - APP ARM7TDMI-S Debug Mode.

A detailed example of JTAG debug access is described in GainSpan Application Note AN-011 [4].

### 2.3.5 GPIO & LED Driver / GPIO

The GPIO ports are referenced to VDDIO. Two GPIO pins called GPIO30_LED1 & GPO31_LED2 have the capability to sink/source 20 mA typical (VDDIO=3.3V) to connect to devices such as switch contacts or LEDs. I2C_DATA/GPIO8 & I2C_CLK/GPIO9 have the capability to sink/source 12 mA typical (VDDIO=3.3V). Other GPIO's have the capability to sink/source 4 mA typical (VDDIO=3.3V). All inputs are capable of generating processor interrupts. They can be individually programmed to provide edge- or level-triggered interrupts. For details on configuring GPIO ports, refer to the GS1011 Peripheral and Register Description [2].

### 2.3.6 ADC

The ADC is a 10-bit, low-power, A-to-D converter capable of running at up to 32 ksps. The ADC contains an internal band-gap reference which provides a stable 1.2 V reference voltage. The ADC can be programmed to use the 1.8 V supply as the full-scale reference. The ADC uses an input clock with a maximum frequency of 1 MHz. A conversion requires 32 clock cycles.

When the internal band-gap reference is used, the reported integer *Value* at temperature *T* (ºC) is related to the voltage $V_{actual}$ at the input pin as:

$$V_{actual} = Value\left(\frac{1.2444 - 0.00014(25 - T)}{1023}\right)$$

When the 1.8V supply voltage is used as the reference, the corresponding relation is:

$$V_{actual} = Value\left(\frac{V_{DD,ADC} - 0.036}{1023}\right)$$

To reduce power consumption the ADC can be disabled automatically between periodic measurements and after single measurements.

For more information, consult the GS1011 Peripheral and Register Description [2] and GS1011 IC data sheet [3] for detailed descriptions.

## 2.4 Power Supply

In this section, diagrams are shown for various application power supply connection.

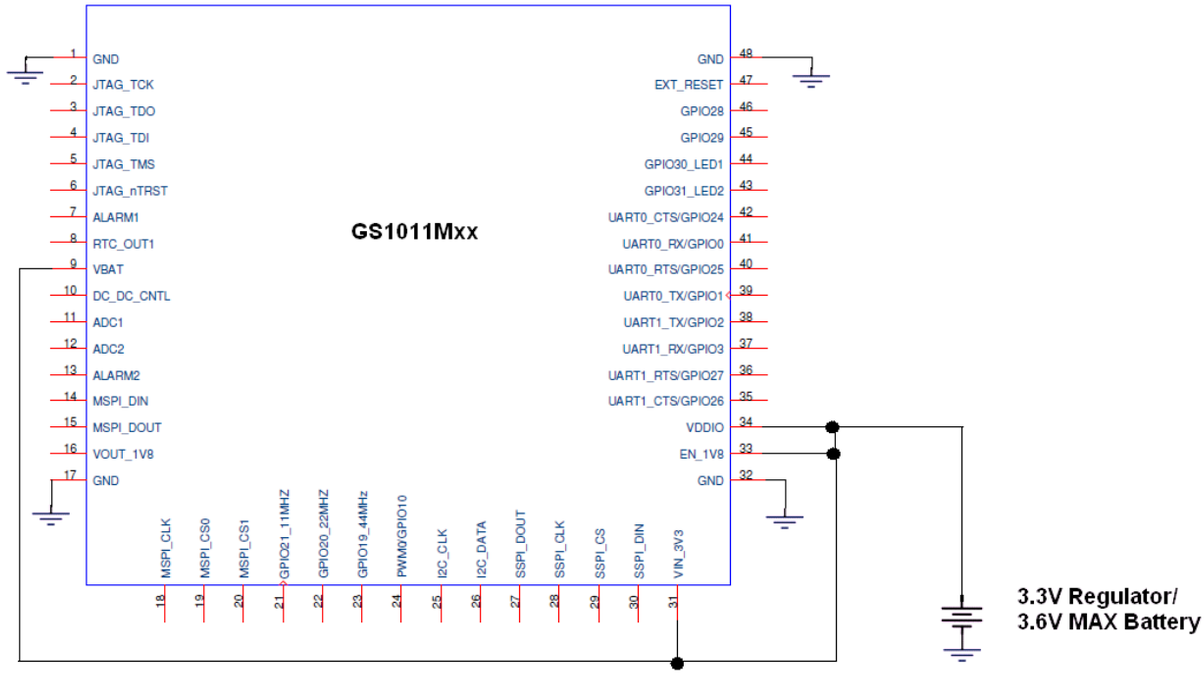


**Figure 2-4: GS1011Mxx Always ON Power Supply Configuration Block Diagram**

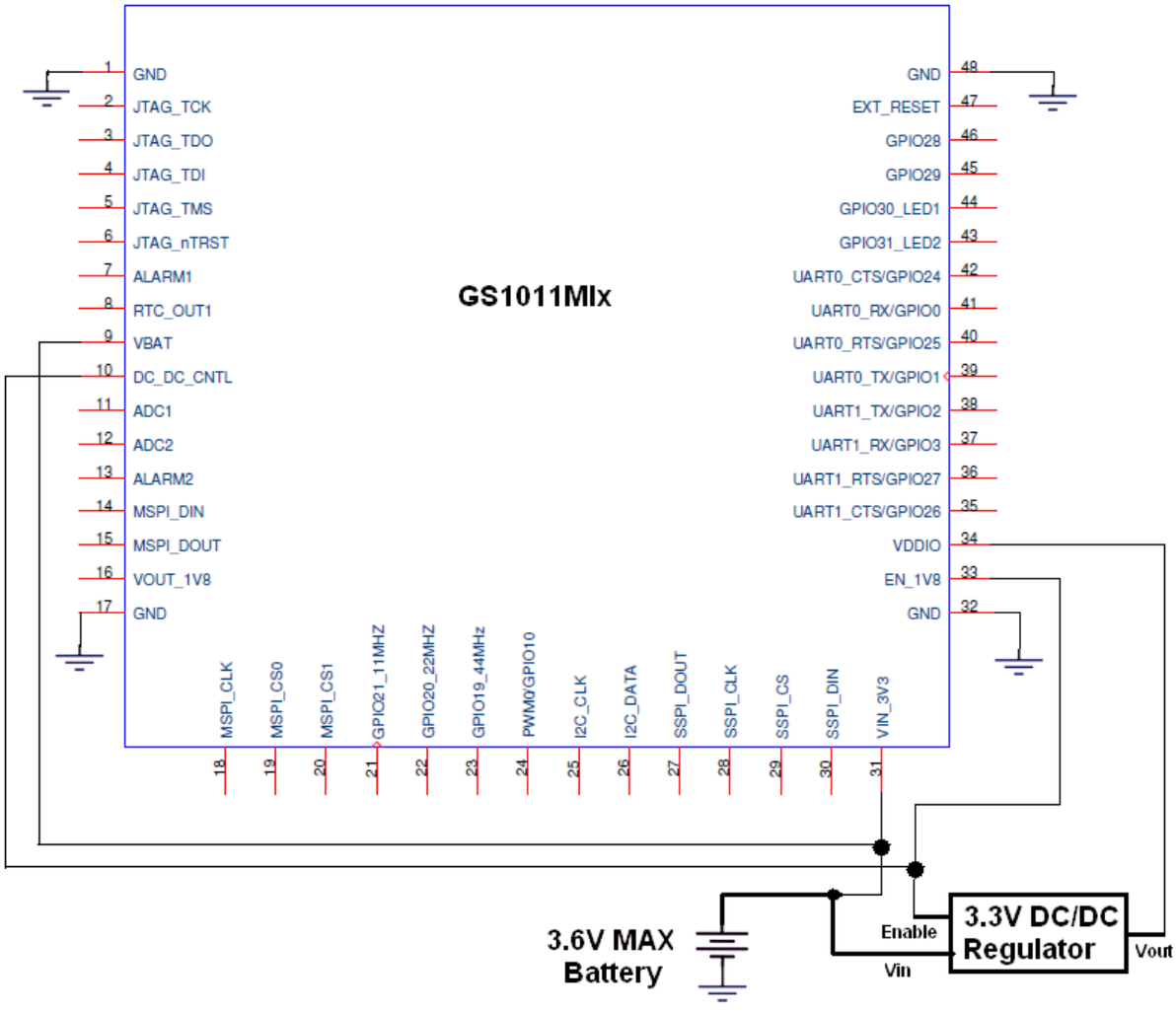


**Figure 2-5: GS1011MIx Battery Powered with 3.3V VDDIO and Regulator Controlled by DC_DC_CNTL Line Block Diagram**

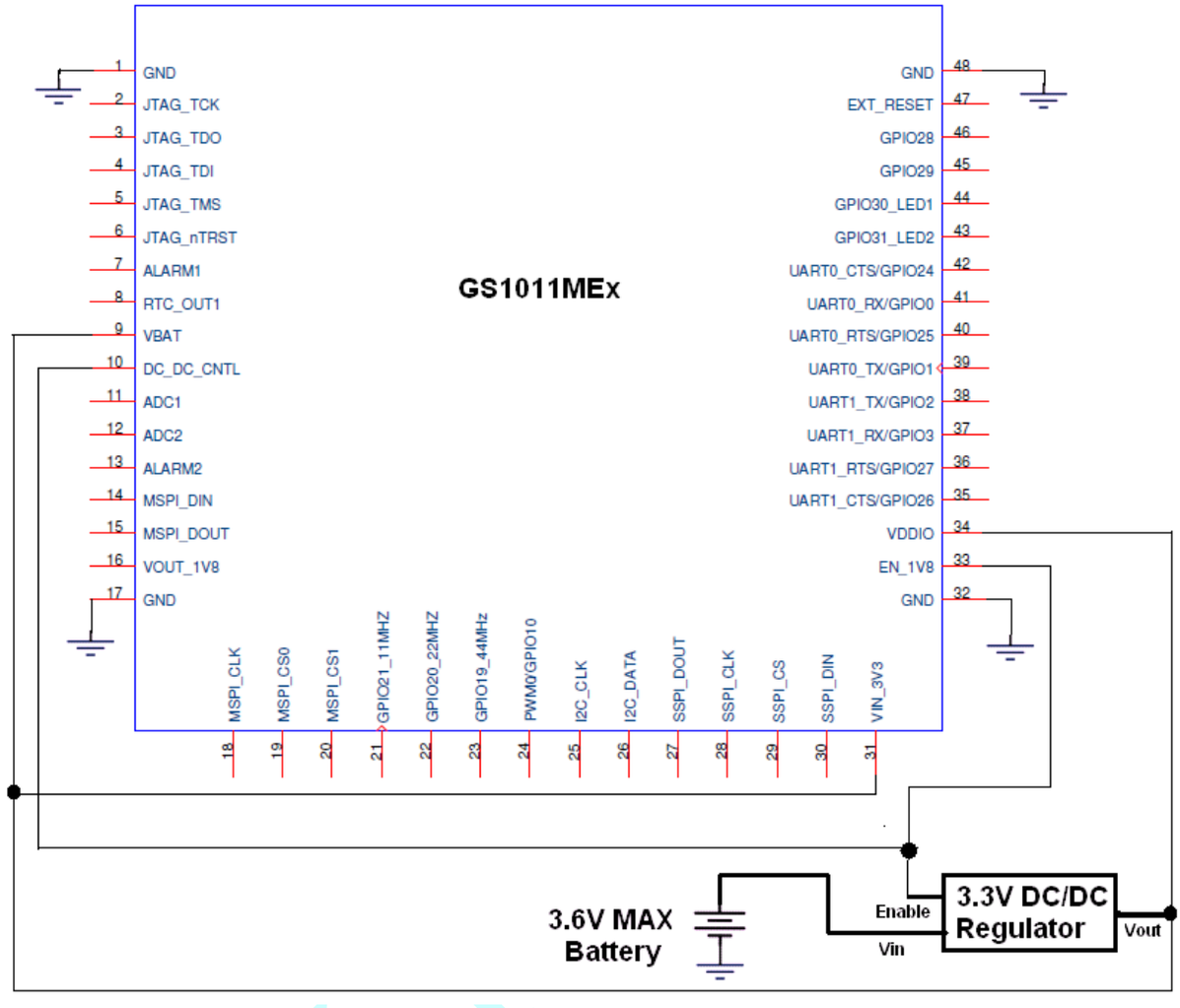


**Figure 2-6: GS1011MEx Battery Powered with 3.3V VDDIO and Regulator Controlled by DC_DC_CNTL Line Block Diagram**

Note that in GS1011MEx, module PA is supplied with VIN_3V3 and in-rush current for PA transmission; thus, the 3.3V DC/DC Regulator may have to be an Up/Down regulator depending on the Battery used.

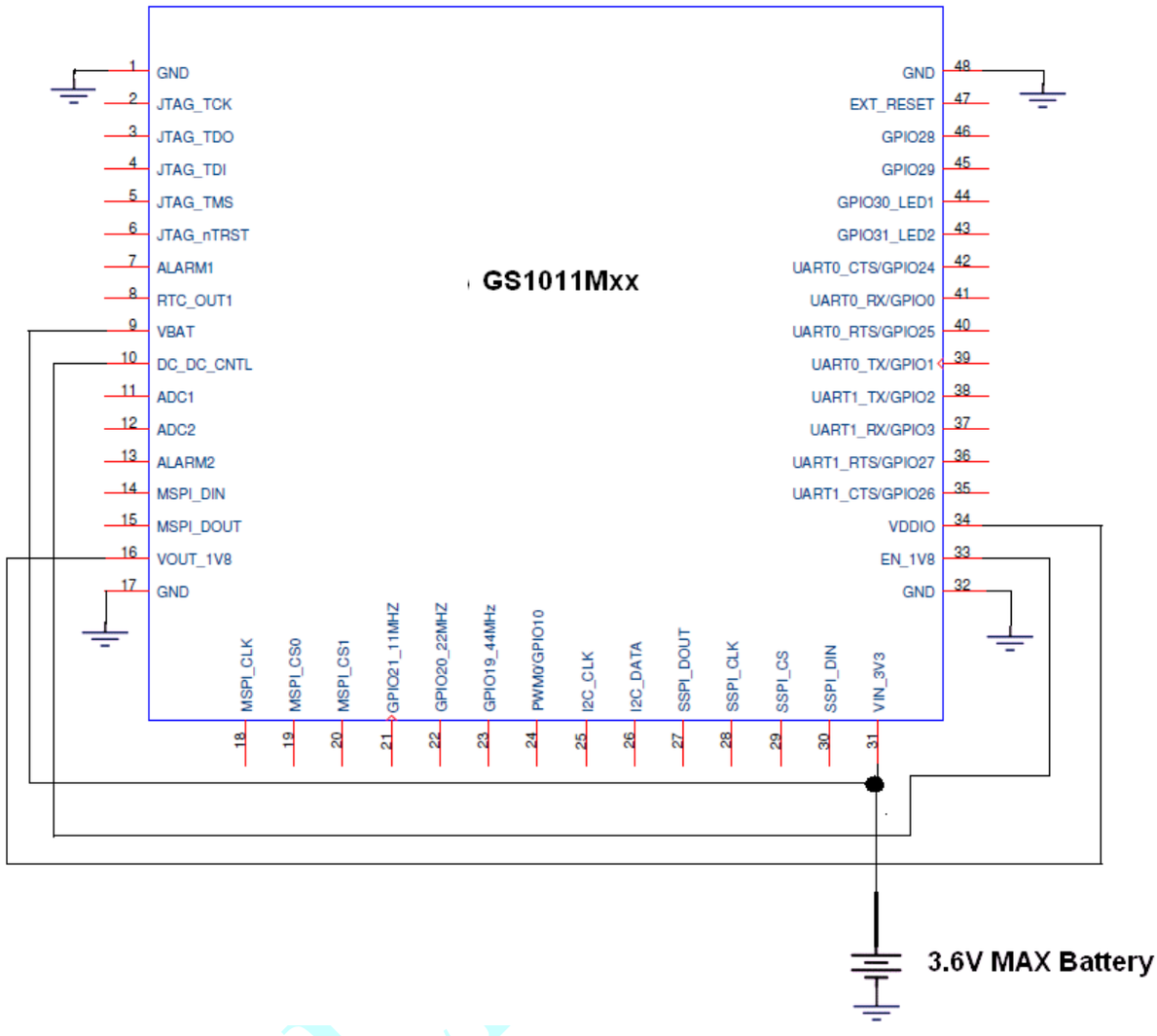


**Figure 2-7: GS1011Mxx Battery Powered with 1.8V VDDIO and Regulator Controlled by DC_DC_CNTL line Block Diagram Connections**

## 2.5 System States

Figure 2-8 shows the power management/clock states of the GS1011Mxx system.

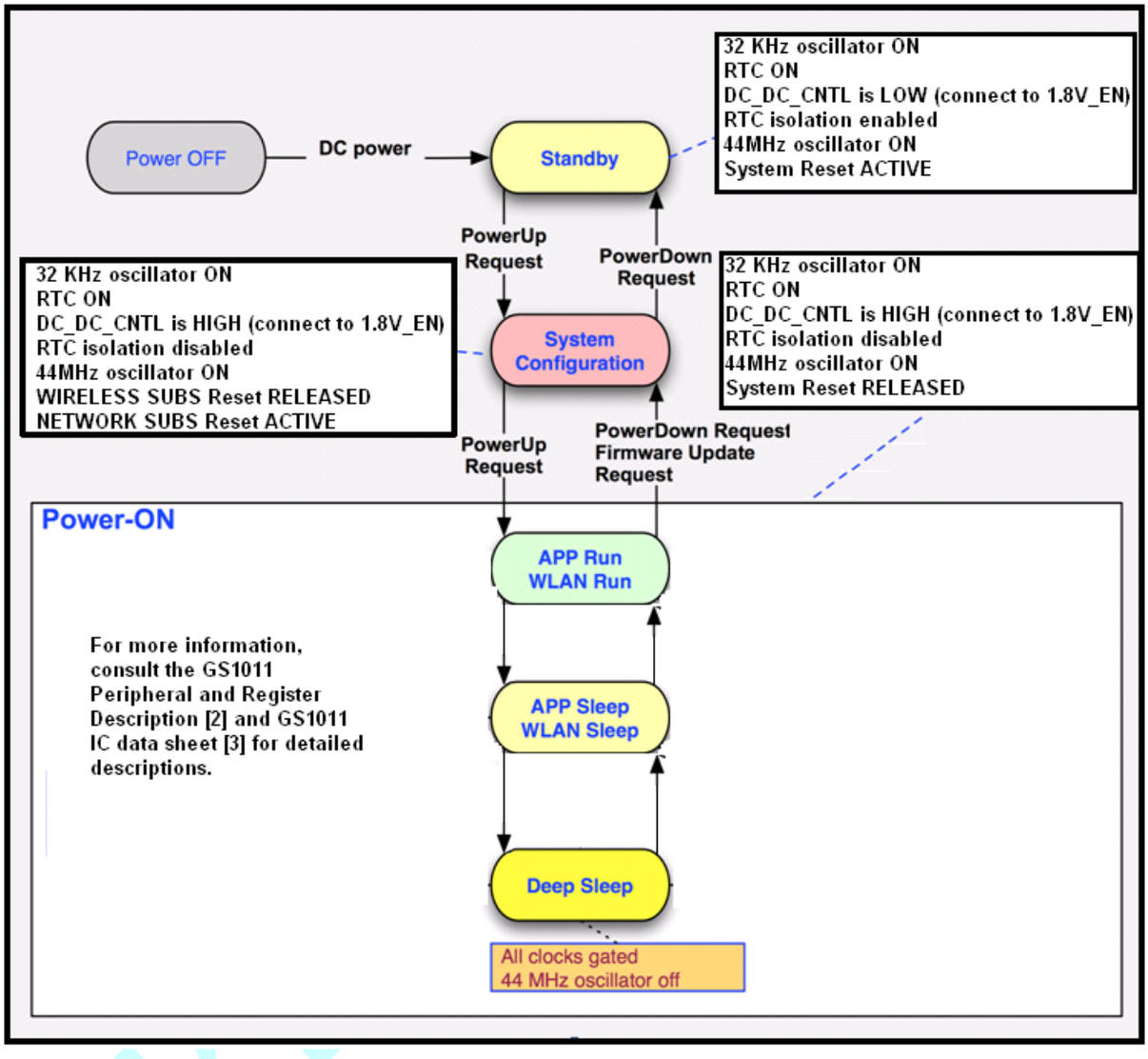


**Figure 2-8: GS1011Mxx System States**

The system states of the GS1011MXX system are as follows:

**Power OFF**: No power source connected to the system.

**Standby**: When supply voltage is stable per Figure 2-6, the RTC is powered up, and the system transitions from the Power OFF state to the Standby state. In this state only the 32.768 kHz clock is running, and the RTC is powered directly by the battery or DC supply.

This is the lowest-power-consumption state. In a typical application, the system returns to the Standby state between periods of activity, to keep the average power very low and enable years of operation using conventional batteries.

**System Configuration**: When a power-up is requested, the system transitions from the Standby state to the System Configuration state. In this state, the WLAN CPU is released from reset by the RTC. The APP CPU remains in the reset state during System Configuration. The WLAN CPU then executes the required system configurations, releases the APP CPU from reset, and transitions to the Power-ON state.

The System Configuration state is also entered on transition from the Power-ON state to the Standby state, to complete necessary preparations before shutting off the power to the core system. Finally, the System Configuration state is used for firmware updates.

**Power-ON**: This is the active state where all system components can be running. The Power-ON state has various sub-states, in which unused parts of the system can be in sleep mode, reducing power consumption. Sleep states are implemented by gating the clock signal off for a specific system component. The Deep-Sleep sub-state, in which all clocks are gated off, allows minimum power consumption while permitting rapid resumption of normal operation. In this state, the 44 MHz reference oscillator can be turned off to further reduce power consumption.

For more information, consult the GS1011 Peripheral and Register Description [2] and GS1011 IC data sheet [3] for detailed descriptions.

# 3 Pin-out and Signal Description

## 3.1 GS1011Mxx Device Pin-out Diagram (Module top view)

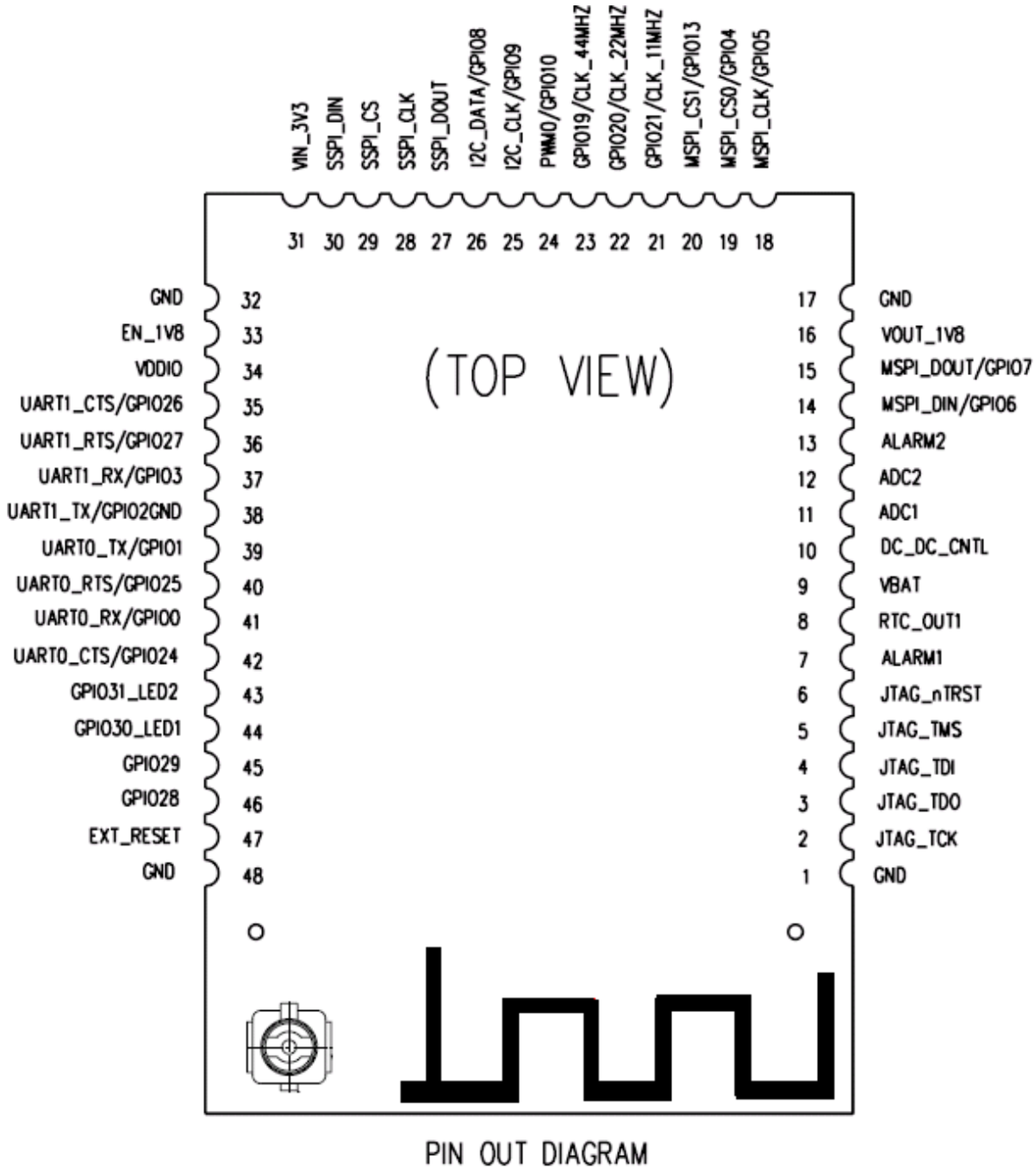


**Figure 3-1: GS1011Mxx Device Pin-out Diagram (Module top view)**

### 3.1.1 GS1011Mxx Module Pins Description

| Pins | Name | Voltage Domain | Internal Bias after hardware reset | Signal State | Description |
|---|---|---|---|---|---|
| 1 | GND | 0V | Not Applicable | Analog port | Ground |
| 2 | JTAG_TCK | VDDIO | Pull-up (See Note 1) | Digital Input | Joint Test Action Group Test Clock |
| 3 | JTAG_TDO | VDDIO | Not Applicable | Digital Output | Joint Test Action Group Test Data Out |
| 4 | JTAG_TDI | VDDIO | Pull-up (See Note 1) | Digital Input | Joint Test Action Group Test Data In |
| 5 | JTAG_TMS | VDDIO | Pull-up (See Note 1) | Digital Input | Joint Test Action Group Test Mode Select |
| 6 | JTAG_nTRST | VDDIO | Pull-up (See Note 1) | Digital Input | Joint Test Action Group Test Mode Reset Active Low |
| 7 | ALARM1 | VBAT | Pull-down (See Note 1) | Digital Input | Embedded Real Time Clock Wake Up Input 1 |
| 8 | RTC_OUT1 | VBAT | Not Applicable | Digital Output | Embedded Real Time Clock Wake Up Output 1 |
| 9 | VBAT | VBAT | Not Applicable | Analog port | On Board Module Real Time Clock Power Supply |
| 10 | DC_DC_CNTL | VBAT | Not Applicable | Digital Output | VIN_3V3 Regulator Control Output |
| 11 | ADC1 | VDD18 (internal) | Not Applicable | Analog Output | General Analog to Digital Converter 1 |
| 12 | ADC2 | VDD18 (internal) | Not Applicable | Analog Output | General Analog to Digital Converter 2 |
| 13 | ALARM2 | VBAT | Pull-down (See Note 1) | Digital Input | Embedded Real Time Clock Wake Up Input 2 |
| 14 | MSPI_DIN / GPIO6 | VDDIO | Pull-down | Digital Input | Master Serial Peripheral Interface Bus Data Input / General Purpose Input Output |
| 15 | MSPI_DOUT / GPIO7 | VDDIO | Pull-down | Digital Output | Master Serial Peripheral Interface Bus Data Output / General Purpose Input Output |
| 16 | VOUT_1V8 | VIN_3V3 (internally regulated) | Not Applicable | Analog port | Internal 1.8V Vout |
| 17 | GND | 0V | Not Applicable | Analog port | Ground |
| 18 | MSPI_CLK / GPIO5 | VDDIO | Pull-down | Digital Input / Output | Master Serial Peripheral Interface Bus Clock / General Purpose Input Output |
| 19 | MSPI_CS0 / GPIO4 | VDDIO | Pull-down | Digital Input / Output | Master Serial Peripheral Interface Bus Chip Select 0 / General Purpose Input Output |
| 20 | MSPI_CS1 / GPIO13 | VDDIO | Pull-down | Digital Output | Master Serial Peripheral Interface Bus Chip Select 1 / General Purpose Input Output |
| 21 | GPO21_11MHZ | VDDIO | Pull-down | Digital Input | Internal Clock Circuitry Test Point / General Purpose Input Output |
| 22 | GPO20_22MHZ | VDDIO | Pull-down | Digital Input | Internal Clock Circuitry Test Point / General Purpose Input Output |

| Pins | Name | Voltage Domain | Internal Bias after hardware reset | Signal State | Description |
|---|---|---|---|---|---|
| 23 | GPO19_44MHZ | VDDIO | Pull-down | Digital Input | Internal Clock Circuitry Test Point / General Purpose Input Output |
| 24 | PWM0 / GPIO10 | VDDIO | Pull-down | Digital Output | Pulse Width Modulator / General Purpose Input Output |
| 25 | I2C_CLK/GPIO9 | VDDIO | Pull-down (NOTE 4) | Digital Input / Output | Inter-Integrated Circuit Clock / General Purpose Input Output |
| 26 | I2C_DATA/GPIO8 | VDDIO | Pull-down (NOTE 4) | Digital Input / Output | Inter-Integrated Circuit Data / General Purpose Input Output |
| 27 | SSPI_DOUT | VDDIO | Pull-up (See Note 1) | Digital Input | SPI Slave Transmit Data Output to the HOST |
| 28 | SSPI_CLK | VDDIO | Pull-up (See Note 1) | Digital Input | SPI Slave Clock Input from the HOST |
| 29 | SSPI_CS | VDDIO | Pull-up (See Note 1) | Digital Input | SPI Slave Chip Select Input from the HOST |
| 30 | SSPI_DIN | VDDIO | Pull-down (See Note 1) | Digital Input | SPI Slave Receive Data Input from the HOST |
| 31 | VIN_3V3 | VIN_3V3 | Not Applicable | Analog port | Single Supply Port |
| 32 | GND | 0V | Not Applicable | Analog port | Ground |
| 33 | EN_1V8 | VDDIO | Need to be driven HIGH or LOW externally | Digital Input | Internal 1.8V regulator enable port-Active High |
| 34 | VDDIO | VDDIO | Not Applicable | Analog port | All I/O voltage domain (can be tied to VIN_3V3 or tied to HOST I/O supply) |
| 35 | UART1_CTS / GPIO26 | VDDIO | Pull-down | Digital Input | Universal Asynchronous Receiver Transmitter 1 Clear to Send Input / General Purpose Input Output |
| 36 | UART1_RTS / GPIO27 | VDDIO | Pull-down (See Note 2) | Digital Output | Universal Asynchronous Receiver Transmitter 1 Request to Send Output / General Purpose Input Output |
| 37 | UART1_RX / GPIO3 | VDDIO | Pull-down | Digital Input | Universal Asynchronous Receiver Transmitter 1 Receive Input / General Purpose Input Output |
| 38 | UART1_TX / GPIO2 | VDDIO | Pull-down | Digital Output | Universal Asynchronous Receiver Transmitter 1 Transmitter Output / General Purpose Input Output |
| 39 | UART0_TX / GPIO1 | VDDIO | Pull-down | Digital Output | Universal Asynchronous Receiver Transmitter 0 Transmitter Output / General Purpose Input Output |
| 40 | UART0_RTS / GPIO25 | VDDIO | Pull-down | Digital Output | Universal Asynchronous Receiver Transmitter 0 Request to Send Output / General Purpose Input Output |
| 41 | UART0_RX / GPIO0 | VDDIO | Pull-down | Digital Input | Universal Asynchronous Receiver Transmitter 0 Receive Input / General Purpose Input Output |

| Pins | Name | Voltage Domain | Internal Bias after hardware reset | Signal State | Description |
|---|---|---|---|---|---|
| 42 | UART0_CTS / GPIO24 | VDDIO | Pull-down | Digital Input | Universal Asynchronous Receiver Transmitter 0 Clear to Send Input / General Purpose Input Output |
| 43 | GPO31_LED2 | VDDIO | Pull-down | Digital Output | Light Emitting Diode Driver / General Purpose Input Output |
| 44 | GPIO30_LED1 | VDDIO | Pull-down | Digital Output | Light Emitting Diode Driver / General Purpose Input Output |
| 45 | GPIO29 | VDDIO | Pull-down (See Note 3) | Digital Input / Output | General Purpose Input Output |
| 46 | GPIO28 | VDDIO | Pull-down (See Note 3) | Digital Input / Output | General Purpose Input Output |
| 47 | EXT_RESET | VDDIO | Pull-up | Digital Input / Output | Module Hardware Reset Input and Power Supply Reset Monitor Indictor |
| 48 | GND | 0V | Not Applicable | Analog port | Ground |

**Table 3-1: Signal Description**

Notes:

1. These pins have onboard hardware configured pull-ups/downs and cannot be changed by software.
2. If UART1_RTS is high during boot, then the WLAN will wait for Flash download via UART0. For development purposes, route this pin to a test point on the board so it can be pulled up to VIN_3V3.
3. GPIO 28 and 29 are sampled at reset to establish JTAG configuration for debugging. These signals should not be driven from an external device. If using JTAG, configure these pins as outputs.
4. If $I^2C$ interface is used, provide 2K Ohm pull-ups, to VDDIO, for pins 25 and 26 (I2C_CLK and I2C_DATA)

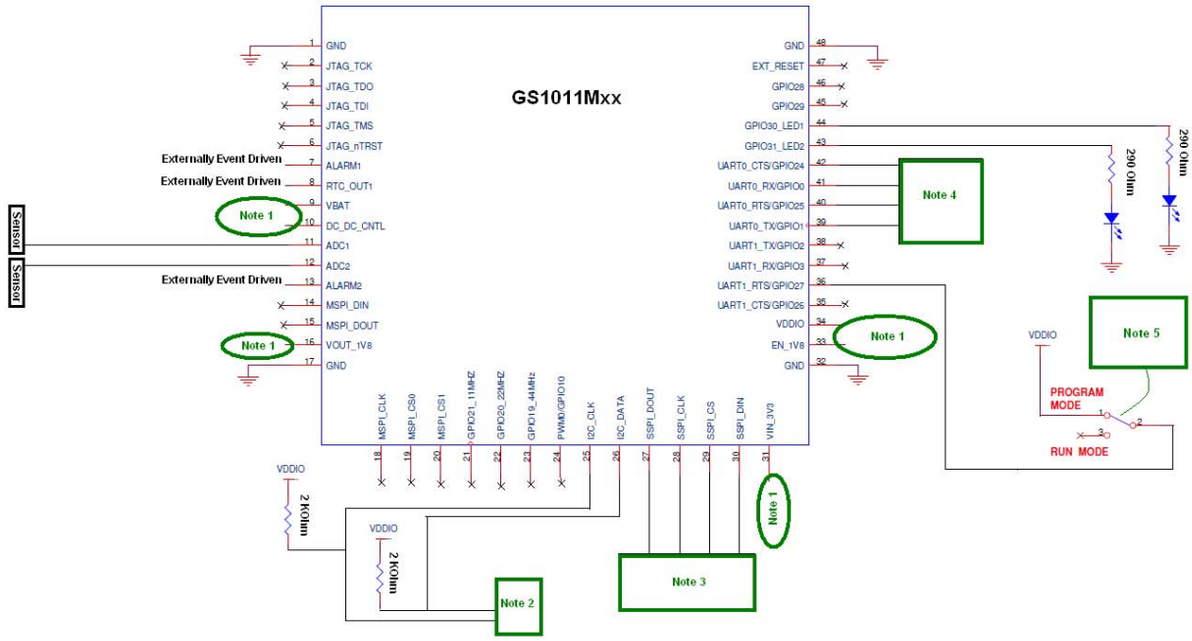


**Figure 3-2: Module pin connection diagram**

Note 1) For the noted pin configurations, please refer to data sheet power supply section.

Note 2) If $I^2C$ interface is used, provide 2KOhm pull-ups, to VDDIO, for pins 25 and 26 (I2C_CLK and I2C_DATA). If not used, leave pins 25 and 26 as No Connects.

Note 3) Connect to external HOST SPI (can be left as No Connects if not used).

Note 4) Connect to external serial HOST UART (can be left as No Connections if not used)

Note 5) This switch enables the programming of GS1011 onboard flash. Switch is recommended for development purposes and is not needed for production.

# 4 Electrical Characteristics

## 4.1 Absolute Maximum Ratings

Conditions beyond those cited in Table 4-1 may cause permanent damage to the GS1011MXX, and must be avoided.

| Parameter | Symbol | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| Storage temperature | $T_{ST}$ | -55 | | +125 | ºC |
| RTC Power Supply | Vbat | -0.5 | | 4.0 | V |
| I/O Supply voltage | VDDIO | -0.5 | | 4.0 | V |
| Single Supply Port | VIN_3V3 | 2.7 | 3.3 | 4.0 | V |

**Table 4-1: Absolute Maximum Ratings**

NOTE: For limitations on state voltage ranges, please consult section 2.6.1 Power supply.

## 4.2 Operating Conditions

| Parameter | Symbol | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| Extended temp. range | $T_A$ | -40 | | +85 | ºC |
| RTC Power Supply | Vbat | 1.2 | 3.3 | 3.6 | V |
| I/O Supply voltage | VDDIO | 1.7 | 3.3 | 3.6 | V |
| Single Supply Port GS1011Mix (as configured per Figure 2-4, 6, & 7) | VIN_3V3 | 2.7 | 3.3 | 3.6 | V |
| Single Supply Port GS1011Mix (as configured per Figure 2-5) | VIN_3V3 | 2.4 | 3.3 | 3.6 | V |
| Single Supply Port GS1011MEx | VIN_3V3 | 3.0 | 3.3 | 3.6 | V |

**Table 4-2: Operating Conditions**

## 4.3 Internal 1.8V regulator

VIN_3V3=VDDIO=Vbat=3.3V Temp=25ºC fOSC=3.0MHz

| Parameter | Symbol | Test conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| Output Voltage | VOUT_1V8 | | | 1.8 | | V |
| Maximum Output Current | IVOUT_1V8 | | | 30 | 50 | mA |
| Oscillation Frequency | fOSC | | 1.6 | | 3.45 | MHz |
| 1.8V Regulator Enable "H" Voltage | EN_1V8 | | 1.0 | | VIN_3V3 | V |
| 1.8V Regulator Enable "L" Voltage | EN_1V8 | | 0 | | 0.25 | V |

**Table 4-3: Operating Conditions**

## 4.4 I/O DC Specifications

### 4.4.1 Digital Input Specifications

| Parameter | Symbol | Minimum | Typical | Maximum | Unit | Note |
|---|---|---|---|---|---|---|
| Input Low Voltage | $V_{IL}$ | -0.3 | | 0.25* VDDIO | V | |
| Input High Voltage | $V_{IH}$ | 0.8* VDDIO | | VDDIO | V | |

**Table 4-4: Digital Input Parameters**

### 4.4.2 Digital Output Specification

| Parameter | Symbol | Mininum | Typical | Maximum | Unit | Note |
|---|---|---|---|---|---|---|
| Output Low Voltage | $V_{OL}$ | 0 | | 0.4 | V | With 4 mA load |
| Output High Voltage | $V_{OH}$ | 1.3 V | | VDDIO | V | $V_{DDIO}$=3.0V, DC current load 4.0 mA<br>$V_{DDIO}$ =1.62 V, DC current load 2.0 mA |
| Output rise time @ VDDIO=3.3V | $t_{TLH}$ | | | 7 | ns | With 4 mA, 33 pF load |
| Output fall time @ VDDIO=3.3V | $t_{THL}$ | | | 7 | ns | With 4 mA, 33 pF load |

**Table 4-5: Digital Output Parameters**

### 4.4.3 I/O Digital Specifications (Tri-State)

| Parameter | Symbol | Mininum | Typical | Maximum | Unit | Note |
|---|---|---|---|---|---|---|
| Input Low Voltage | $V_{IL}$ | -0.3 | | 0.25* VDDIO | V | |
| Input High Voltage | $V_{IH}$ | 0.8* VDDIO | | VDDIO | V | |
| Schmitt trig. Low to High threshold point | $V_{T+}$ | 1.5 | | | V | |
| Schmitt trig. High to Low threshold point | $V_{T-}$ | | | 1 | V | |
| Input Leakage Current | $I_L$ | | | 5 | µA | Pull up/down disabled |
| Tri-State Output Leakage Current | $Oz_L$ | | | 5 | µA | Pull up/down disabled |

| Parameter | Symbol | Mininum | Typical | Maximum | Unit | Note |
|---|---|---|---|---|---|---|
| Pull-Up Resistor | $R_u$ | 0.05 | | 1 | MΩ | |
| Pull-Down Resistor | $R_d$ | 0.05 | | 1 | MΩ | |
| Output Low Voltage | $V_{OL}$ | 0 | | 0.4 | V | With 4/12/20 mA load |
| Output High Voltage | $V_{OH}$ | 1.3 V | | VDDIO | V | With 4/12/20 mA load<br>With 2/6/10 mA load |
| Output rise time @ VDDIO =3.3V | $t_{ToLH}$ | | | 7 | ns | With 4/12/20 mA load, 33 pF |
| Output fall time @ VDDIO = 3.3V | $t_{ToHL}$ | | | 7 | ns | With 4/12/20 mA load, 33 pF |
| Input rise time | $t_{TiLH}$ | | | 7 | ns | |
| Input fall time | $t_{TiHL}$ | | | 7 | ns | |

**Table 4-6: I/O Digital Parameters**

### 4.4.4 RTC Input Specifications (with Schmitt Trigger)

| Parameter | Symbol | Mininum | Typical | Maximum | Unit | Note |
|---|---|---|---|---|---|---|
| I/O Supply Voltage | $V_{DDRTC}$ | 1.2 | | Vbat | V | |
| Input Low Voltage | $V_{IL}$ | -0.3 | | 0.25*$V_{DDRTC}$ | V | |
| Input High Voltage | $V_{IH}$ | 0.8*$V_{DDRTC}$ | | $V_{DDRTC}$ | V | |
| Schmitt trig. Low to High threshold point | $V_{T+}$ | 0.57*$V_{DDRTC}$ | | 0.68*$V_{DDRTC}$ | V | |
| Schmitt trig. High to Low threshold point | $V_{T-}$ | 0.27*$V_{DDRTC}$ | | 0.35*$V_{DDRTC}$ | V | |
| Input Leakage Current | $I_L$ | | 260 | | pA | |

**Table 4-7: RTC Input Parameters**

### 4.4.5 RTC Output Specifications

| Parameter | Symbol | Mininum | Typical | Maximum | Unit | Note |
|---|---|---|---|---|---|---|
| I/O Supply Voltage | $V_{DDRTC}$ | 1.2 | | Vbat | V | |
| Output Low Voltage | $V_{OL}$ | 0 | | 0.4 | V | |
| Output High Voltage | $V_{OH}$ | 0.8*$V_{DDRTC}$ | | $V_{DDRTC}$ | V | |
| Output rise time | $t_{TLH}$ | 19 | | 142 | ns | 50 pF load |
| Output fall time | $t_{THL}$ | 21 | | 195 | ns | 50 pF load |
| Input Leakage Current | $I_L$ | | 730 | | pA | |

**Table 4-8: RTC Output Parameters**

## 4.5 Power Consumption

Test Conditions: VDD33=VDDIO=Vbat=3.3V Temp=25ºC

| System state | Current (Typ.) |
|---|---|
| Standby | TBD |
| Deep Sleep | TBD |
| Receive (GS1011Mxx; -90 dBm RX sens. @ 1Mb/Sec. | TBD |
| Transmit (GS1011MIx; +9 dBm at antenna port @ 1Mb/Sec.) | TBD |
| Transmit (GS1011MEx; +17 dBm at antenna port @ 1Mb/Sec.) | TBD |

**Table 4-9: Power Consumption in Different States**

## 4.6 Radio Parameters

Test Conditions: VIN_3V3=VDDIO=Vbat=3.3V Temp=25ºC

| Parameter | Minimum | Typical | Maximum | Unit | Notes |
|---|---|---|---|---|---|
| RF Frequency range | 2412 | | 2497 | MHz | |
| Radio bit rate | 1 | | 11 | Mbps | |
| Transmit specification for GS1011MIx | | | | | |
| Output power (average) | | 9 | | dBm | Modulated signal at antenna port; 1Mb/Sec. |
| Spectrum Mask<br>F0 +/- 11 MHz<br>Offset >= 22 MHz | <br>-30<br>-50 | | | dBr | Modulated signal at antenna port |
| Receive Sensitivity at antenna port | | -81<br>-84<br>-88<br>-90 | | dBm | 11 Mbps QPSK, 8% PER<br>5.5 Mbps QPSK, 8% PER<br>2 Mbps QPSK, 8% PER<br>1 Mbps BPSK, 8% PER |
| Transmit specification for GS1011MEx | | | | | |
| Output power (average) | | 17 | | dBm | Modulated signal at antenna port; 1Mb/Sec. |
| Spectrum Mask<br>F0 +/- 11 MHz<br>Offset >= 22 MHz | <br>-30<br>-50 | | | dBr | Modulated signal at antenna port |
| Receive Sensitivity at antenna port | | -81<br>-84<br>-88<br>-90 | | dBm | 11 Mbps QPSK, 8% PER<br>5.5 Mbps QPSK, 8% PER<br>2 Mbps QPSK, 8% PER<br>1 Mbps BPSK, 8% PER |

**Table 4-10: Radio Parameters**

## 4.7 ADC Parameters

Test Conditions: VIN_3V3=VDDIO=Vbat=3.3V Temp=25ºC

| Parameter | Minimum | Typical | Maximum | Unit | Notes |
|---|---|---|---|---|---|
| ADC Resolution | - | 10 | - | Bits | |
| ADC Sample Freq | 1.024 | - | 31.25 | ksps | |

| | | | | | |
|---|---|---|---|---|---|
| ADC input Clock Freq | 32.768 | - | 1000 | kHz | |
| ADC Full Scale Voltage | | VOUT_1V8 – 0.036 | | V | Reference = VOUT_1V8 |
| Conversion Time | | 32 | | Clocks | Based on internally generated 1MHz or 32.768 KHz Clocks |
| ADC Integral Non-Linearity (INL) | -2.0 | - | 2.0 | LSB | |
| ADC Differential non-linearity (DNL) | -1.0 | - | 1.0 | LSB | |
| AVDD Power Supply current (operational) | - | 400 | 800 | µA | |
| ADC Offset Error | -10 | - | 10 | mV | |
| ADC Gain Error | -10 | - | 10 | mV | |
| Settling Time | | - | 1 | µS | |
| Input resistance | 1 | - | - | MOhm | |
| Input Capacitance | - | 10 | - | pF | |
| Bandgap Output Voltage (Vref) (T = 25 ºC) | 1.179 | 1.24 | 1.301 | V | |

**Table 4-11: ADC Parameters**

## 4.8 SPI Interface Timing

Test Conditions: VIN_3V3=VDDIO=Vbat=3.3V Temp=25ºC

### 4.8.1 Motorola SPI, clock polarity SPO = 0, clock phase SPH = 0

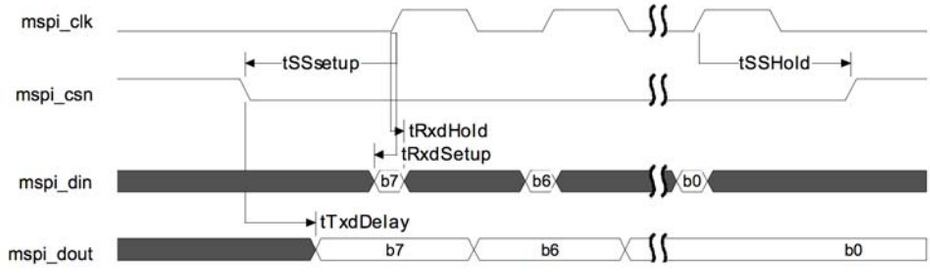


**Figure 4-1: timing diagram, Master mode, SPO=SPH=0.**

| Parameter | Description | Minimum | Maximum | Unit |
|---|---|---|---|---|
| tSSetup | Minimum time between falling edge of Select line and first rising edge of SPI clock | 1 | | MSPI clock period |
| tTxdDelay | Delay in Master asserting TX line after falling edge of Select line | | 2 core SPI clock peri-ods + 3 nsec | mixed |
| tRxdSetup | Time before rising edge of SPI clock by which received data must be ready | 30 | | nsec |
| tRxdHold | Time for which received data must be stable after rising edge of SPI clock | 10 | | nsec |
| tSSHold | Time for which the Select line will be held after the sampling edge for the final bit to be transferred | 1 | | MSPI clock period |

**Table 4-12: timing parameters, Master mode, SPO=SPH=0.**

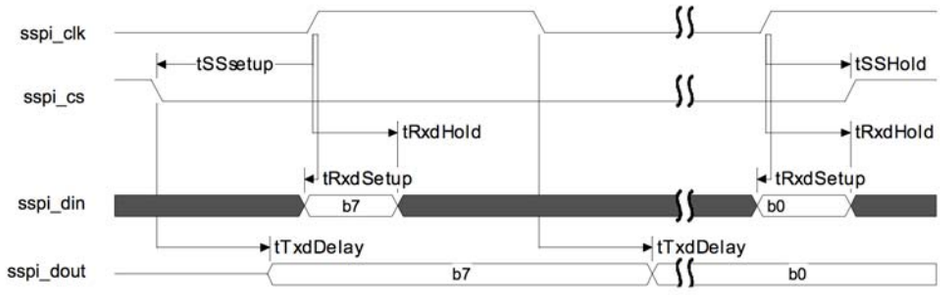


**Figure 4-2: timing diagram, Slave mode, SPO=SPH=0.**

| Parameter | Description | Minimum | Maximum | Unit |
|---|---|---|---|---|
| tSSetup | Minimum time between falling edge of Select line and first rising edge of SPI clock. | 4 core SPI clock periods + 68 ns | | mixed |
| tTxdDelay | Delay in Slave asserting TX line after falling edge of SPI clock, or the first bit after falling edge of the Select line. | | 4 core SPI clock periods + 68 ns | mixed |
| tRxdSetup | Time before rising edge of SPI clock by which received data must be ready | 15 | | ns |
| tRxdHold | Time for which received data must be stable after rising edge of SPI clock | 3 core SPI clock periods + 14 ns | | mixed |
| tSSHold | Time for which the Select line will be held after the sampling edge for the final bit to be transferred | 3 core SPI clock periods + 14 ns | | mixed |

**Table 4-13: timing parameters, Slave mode, SPO=SPH=0.**



### 4.8.2 Motorola SPI, clock polarity SPO = 0, clock phase SPH = 1

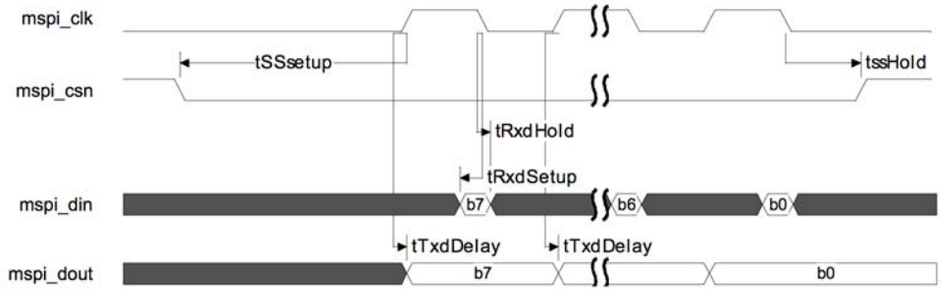


**Figure 4-3: timing diagram, Master, SPO=0, SPH=1.**

| Parameter | Description | Minimum | Maximum | Unit |
|---|---|---|---|---|
| tSSetup | Minimum time between falling edge of select line and first rising edge of SPI clock. | 1.5 | | MSPI clock period |
| tTxdDelay | Delay in Master asserting TX line after rising edge of SPI clock. | | 0 | ns |
| tRxdSetup | Time before falling edge of SPI clock by which received data must be ready. | 30 | | ns |
| tRxdHold | Time for which received data must be stable after falling edge of SPI clock. | 10 | | ns |
| tSSHold | Time for which the Select line will be held low after the sampling edge for the final bit to be transferred. | 0.5 | | MSPI clock period |

**Table 4-14: timing parameters, Master mode; SPO=0, SPH=1.**



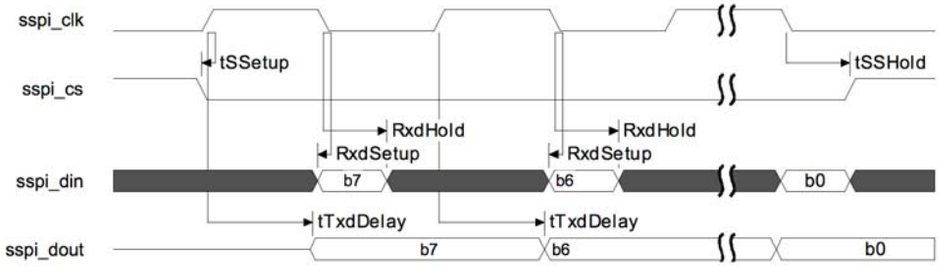

**Figure 4-4: timing diagram, Slave, SPO=0, SPH=1.**

| Parameter | Description | Minimum | Maximum | Unit |
|---|---|---|---|---|
| tSSetup | Minimum time between falling edge of select line and first rising edge of SPI clock. | 15 | | ns |
| tTxdDelay | Delay in Slave asserting TX line after rising edge of SPI clock. | | 4 core SPI clock periods + 68 ns | mixed |
| tRxdSetup | Time before falling edge of SPI clock by which received data must be ready. | 15 | | ns |
| tRxdHold | Time for which received data must be stable after falling edge of SPI clock. | 3 core SPI clock periods + 14 ns | | mixed |
| tSSHold | Time for which the Select line will be held low after the sampling edge for the final bit to be transferred. | 3 core SPI clock periods + 14 ns | | mixed |

**Table 4-15: timing parameters, Slave mode, SPO=0, SPH=1.**



### 4.8.3 Motorola SPI, clock polarity SPO = 1, clock phase SPH = 0

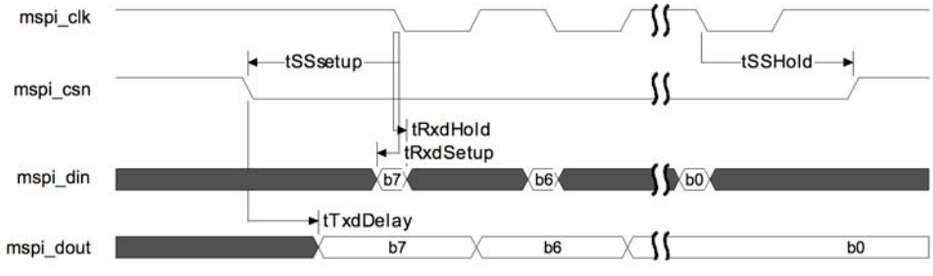


**Figure 4-5: timing diagram, Master mode, SPO=1, SPH=0.**

| Parameter | Description | Minimum | Maximum | Unit |
|---|---|---|---|---|
| tSSetup | Minimum time between falling edge of select line and first falling edge of SPI clock. | 1 | | MSPI clock period |
| tTxdDelay | Delay in Master asserting TX line after falling edge of Select line. | | 2 core SPI clock periods + 3 ns | mixed |
| tRxdSetup | Time before falling edge of SPI clock by which received data must be ready. | 30 | | ns |
| tRxdHold | Time for which received data must be stable after falling edge of SPI clock. | 10 | | ns |
| tSSHold | Time for which the Select line will be held low after the sampling edge for the final bit to be transferred. | 1 | | MSPI clock period |

**Table 4-16: timing parameters, Master mode, SPO=1, SPH=0.**

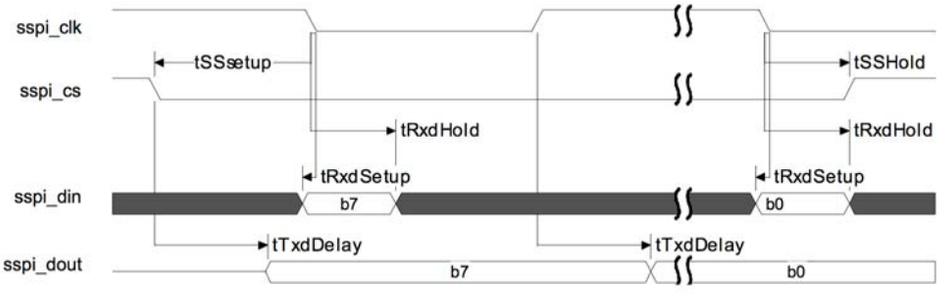


**Figure 4-6: timing diagram, Slave mode, SPO=1, SPH=0.**

| Parameter | Description | Minimum | Maximum | Unit |
|---|---|---|---|---|
| tSSetup | Minimum time between falling edge of Select line and first falling edge of SPI clock. | 4 core SPI clock periods + 68 ns | | Mixed |
| tTxdDelay | Delay in Slave asserting TX line after rising edge of SPI clock, or the first bit after falling edge of the Select line. | | 4 core SPI clock periods + 68 ns | Mixed |
| tRxdSetup | Time before falling edge of SPI clock by which received data must be ready. | 15 | | ns |
| tRxdHold | Time for which received data must be stable after falling edge of SPI clock. | 3 core SPI clock periods + 14 ns | | Mixed |
| tSSHold | Time for which the Select line will be held low after the sampling edge for the final bit to be transferred. | 3 core SPI clock periods + 14 ns | | MSPI clock period |

**Table 4-17: timing parameters, Slave mode, SPO=1, SPH=0.**

### 4.8.4 Motorola SPI, clock polarity SPO = 1, clock phase SPH = 1

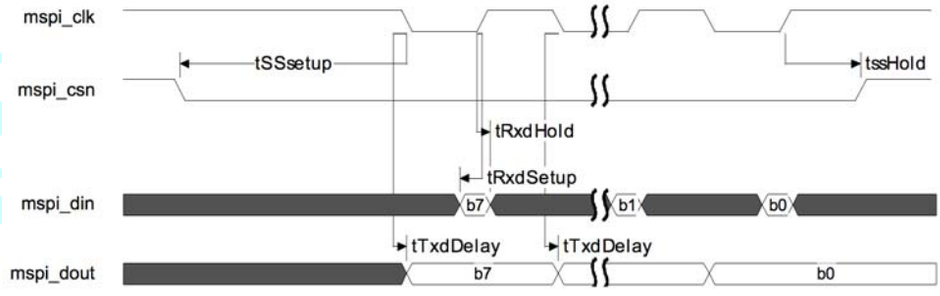


**Figure 4-7: timing diagram, Master mode, SPO=SPH=1.**

| Parameter | Description | Minimum | Maximum | Unit |
|---|---|---|---|---|
| tSSetup | Minimum time between falling edge of select line and first falling edge of SPI clock. | 1.5 | | MSPI clock period |
| tTxdDelay | Delay in Master asserting TX line after falling edge of SPI clock. | | 0 | ns |
| tRxdSetup | Time before rising edge of SPI clock by which received data must be ready. | 30 | | ns |
| tRxdHold | Time for which received data must be stable after rising edge of SPI clock. | 10 | | ns |
| tSSHold | Time for which the Select line will be held low after the sampling edge for the final bit to be transferred. | 0.5 | | MSPI clock period |

**Table 4-18: timing parameters, Master mode, SPO=SPH=1.**

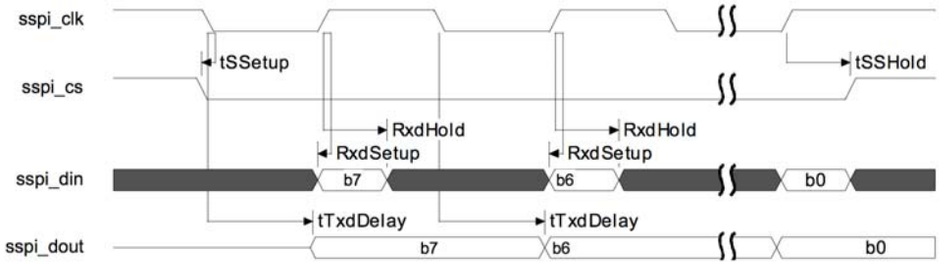


**Figure 4-8: timing diagram, Slave mode, SPO=SPH=1.**

| Parameter | Description | Minimum | Maximum | Unit |
|---|---|---|---|---|
| tSSetup | Minimum time between falling edge of select line and first falling edge of SPI clock. | 15 | | ns |
| tTxdDelay | Delay in Slave asserting TX line after falling edge of SPI clock. | | 4 core SPI clock periods + 68 ns | Mixed |
| tRxdSetup | Time before rising edge of SPI clock by which received data must be ready. | 15 | | ns |
| tRxdHold | Time for which received data must be stable after rising edge of SPI clock. | 3 core SPI clock periods + 14 ns | | Mixed |
| tSSHold | Time for which the Select line will be held low after the sampling edge for the final bit to be transferred. | 3 core SPI clock periods + 14 ns | | Mixed |

**Table 4-19: timing parameters, Master mode, SPO=SPH=1.**

## 4.9 Electrostatic discharge (ESD)

TBD

# 5 Package and Layout Guidelines

## 5.1 GS1011MIx Recommended PCB Footprint and Dimensions

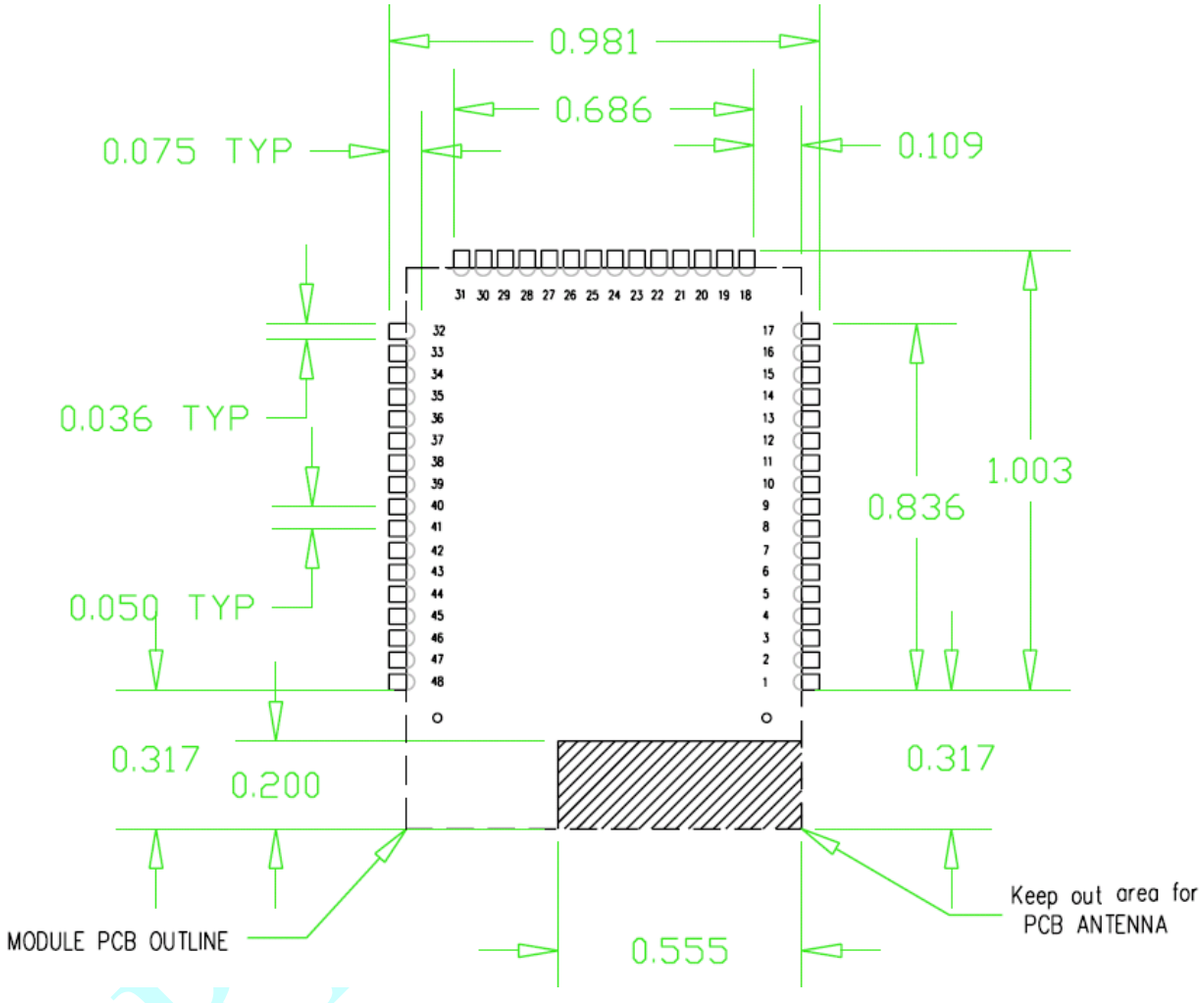


**Figure 5-1: GS1011MIx Module Recommended PCB Footprint**

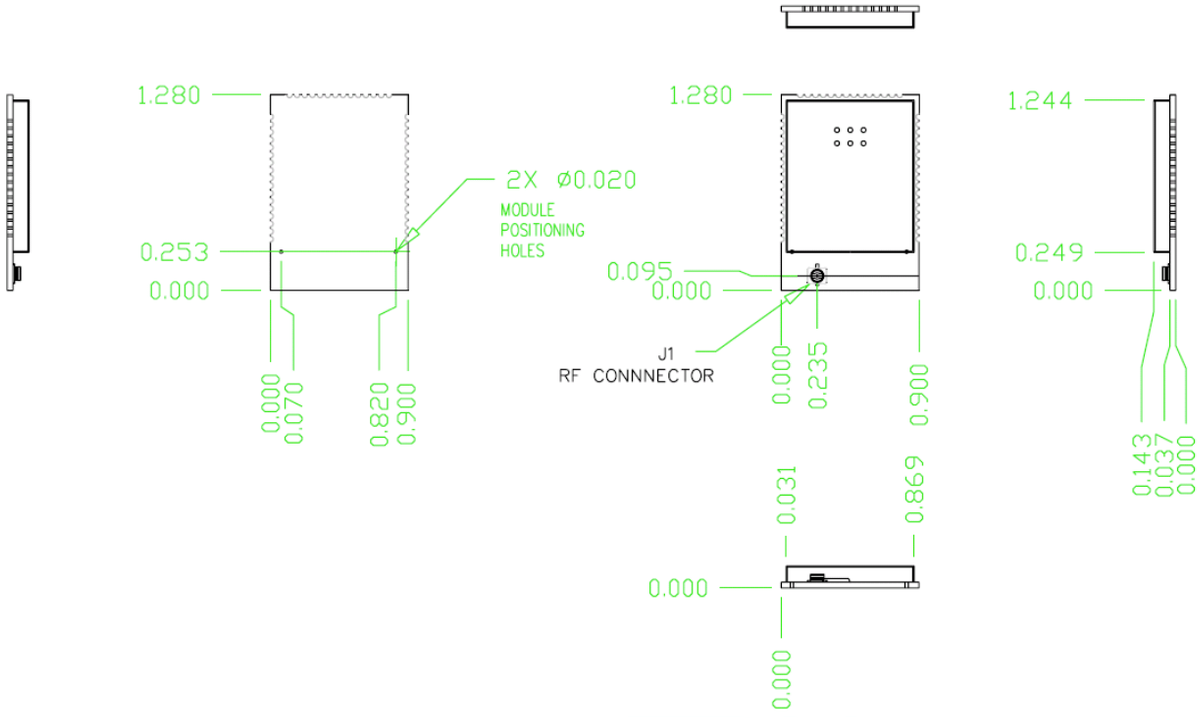


**Figure 5-2: GS1011MIx Module Dimensions**

## 5.2 GS1011MEx Package

**TBD**

**Figure 5-3: GS1011MIx module layout pad dimensions**

## 5.3 GS1011Mxx Layout Guidelines

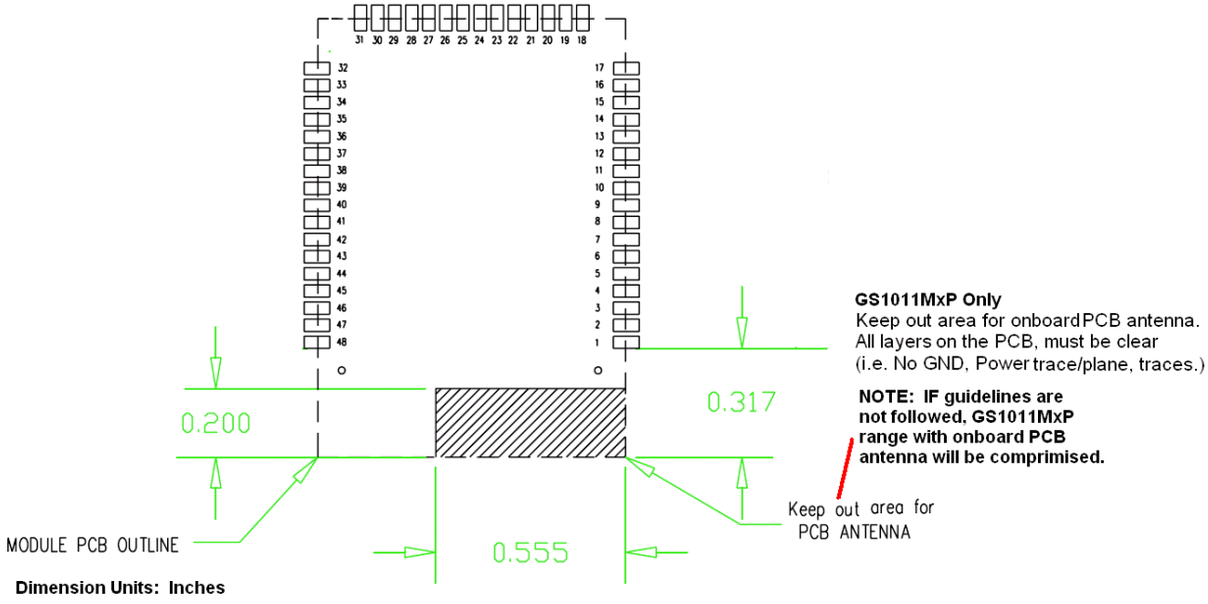


**Figure 5-4: GS1011MIx module layout pad dimensions**

In addition to the guidelines in Figure 13, note the following suggestions:

GS1011MEx and GS1011MIx

- External Bypass capacitors for all module supplies should be as close as possible to the module pins.
- Never place the antenna very close to metallic objects.
- The external dipole antennas need a reasonable ground plane area for antenna efficiency.

GS1011MxP onboard PCB antenna specific

- The PCB antenna keep out area, as shown in Figure 5-4, must be adhered to (i.e. No ground, power trace/plane, traces; all layers of PCB, in the keep out area, must be clear), or the over the air range of the GS1011MxP will be compromised.
- Do not use a metallic or metalized plastic for the end product enclosure.
- Keep Plastic enclosure 1cm min height above the GS1011MxP PCB antenna while maintaining the keep-out area, as shown in Figure 5-4.

### 5.3.1 Surface Mount Assembly

The reflow profile is shown in Figure 5-5. Recommended reflow parameters are summarized in Table 5-1.

TBD

**Figure 5-5: Reflow temperature profile.**

| Profile Feature | |
|---|---|
| **PreHeat** | |
| Ramp up rate from 25°C to 150°C | TBD |
| | |
| **Soak or dryout** | |
| Temperature Min (Tsmin) | TBD |
| Temperature Max (Tsmax) | TBD |
| Time (Ts) from Tsmin to Tsmax | TBD |
| | |
| **Reflow** | |
| Liquidus Temperature ($T_L$) | TBD |
| Time ($t_L$) maintained above $T_L$ | TBD |
| Ramp up rate from $T_L$ to $T_P$ | TBD |
| Peak Temperature (Tp) | TBD |
| Time ($t_P$) within 5°C of the peak temperature $T_P$ | TBD |
| Ramp up rate from $T_P$ to $T_L$ | TBD |
| Time 25°C to Peak Temperature | TBD |

**Table 5-1: Recommended reflow parameters.**

# 6 Ordering Information

| DEVICE DESCRIPTION | ORDERING NUMBER |
|---|---|
| Extended range module using PCB antenna | GS1011MEP |
| Extended range module using external antenna | GS1011MEE |
| **DEVICE DESCRIPTION** | **ORDERING NUMBER** |
| Low power module using PCB antenna | GS1011MIP |
| Low power module using external antenna | GS1011MIE |

# 7 References


| | | | | |
|---|---|---|---|---|
| [1] | **Title** | Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) Specifications | | |
| | **Reference** | IEEE Standard 802.11-2007 | | |
| | **Version** | | **Date** | June 12, 2007 |
| | **Source** | IEEE | | |

| | | | | |
|---|---|---|---|---|
| [2] | **Title** | GS1011 Peripheral and Register Description | | |
| | **Reference** | GS1011-PRD | | |
| | **Version** | 1.0 | **Date** | November 11, 2009 |
| | **Source** | GainSpan | | |

| | | | | |
|---|---|---|---|---|
| [3] | **Title** | GS1011 ULTRA LOW-POWER WIRELESS SYSTEM-ON-CHIP DATA | | |
| | **Reference** | GS1011-DS | | |
| | **Version** | 1.0 | **Date** | November 9, 2009 |
| | **Source** | GainSpan | | |

| | | | | |
|---|---|---|---|---|
| [4] | **Title** | Slingshot and JTAG Configuration | | |
| | **Reference** | AN-011 | | |
| | **Version** | 3.0 | **Date** | Feb 24, 2009 |
| | **Source** | GainSpan | | |

# 8 Limitations

THIS DEVICE AND ASSOCIATED SOFTWARE ARE NOT DESIGNED, MANUFACTURED OR INTENDED FOR USE OR RESALE FOR THE OPERATION OF APPLICATION IN A HAZARDOUS ENVIRONMENT, OR REQUIRING FAIL-SAFE PERFORMANCE, OR IN WHICH THE FAILURE OF PRODUCTS COULD LEAD DIRECTLY TO DEATH, PERSONAL INJURY, OR SEVERE PHYSICAL OR ENVIRONMENTAL DAMAGE (COLLECTIVELY, "HIGH RISK APPLICATIONS"). YOU AGREE AND ACKNOWLEDGE THAT YOU HAVE NO LICENSE TO, AND SHALL NOT (AND SHALL NOT ALLOW A THIRD PARTY TO) USE THE TECHNOLOGY IN ANY HIGH RISK APPLICATIONS, AND LICENSOR SPECIFICALLY DISCLAIMS ANY WARRANTY REGARDING, AND ANY LIABILITY ARISING OUT OF, HIGH RISK APPLICATIONS.