Raman Research Institute, Bangalore

RRI EEG Bio-Amp

Documentation

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1.0 Introduction

1.1 What and Why?

The RRI EEG Bio-Amp or the EEG Bio-signal Amplifier is an Electronic Module indigenously developed at Raman Research Institute, Bangalore for amplification of electrical signals emanating from the brain. The Human Brain communicates with various parts of the human body with weak electrical signals. These signals are a result of voltage fluctuations due to the flow of ionic current within the neurons of the brain. Different lobes of the brain are responsible for carrying out different functions of the human body. Tapping and studying the electrical activity of these lobes helps in deciphering the communication protocol the brain uses to command other organs. Electroencephalography (EEG), a widely used technique in medical sciences to analyze brain health, is performed by recording and analyzing electrical activity of the brain.

Since the brain is enclosed within a highly protected cage - the Skull, the signals that are tapped non-invasively (from the scalp) are highly attenuated. Which is why, the need for an EEG Bio-signal amplifier is born. This amplifier is responsible for amplifying such faint brain signals collected non-invasively from electrodes attached to the subject's scalp, preserving signals of frequencies within the operating range while rejecting unwanted frequencies.

1.2 Operating Characteristics

Operating Frequency Range	1 - 125 Hz
Gain	7000 - 15000
Notch	50 Hz
Input Voltage Levels	1-100µV
Output Voltage Levels	Typically, 0.5-2.0 V (peak to peak)
DC Offset in output	~ 2.5 V

1.3 Utility

The amplified output of the brain signals will be subjected to various analyses working on digital logic, which require signals as data (bits). This conversion will be possible with the help of Analog to Digital Converter (ADC) circuits. The RRI EEG Bio-Amp aims at amplifying the brain signals to levels usable by an ADC module, implemented on Arduino™ Platform.

2.0 Bio-Amp Circuit and Simulation

2.1 Components Used

S.No	Component	Description	Package	Quantity
1	INA114	Instrumentation Amplifier	SOL-16	2 Nos.
2	LM7805C	Voltage Regulator (5V)	SOT-223	1 No.
3	1N5819	Schottky Barrier Rectifier	SOD-123	
4	AP358	Low Power Dual Op-Amps	SOP-8L	
5	BAV199	Dual Diode (Low Leakage)	SOT-23	
6	PGB1010603	ESD Suppressor	0603	
7	TMV 0505S	DC-DC Converter		1 No.
8	3.5mm Jack	Input / Output Connectors	SMD	7 Nos.

2.2 Distinct Circuits present

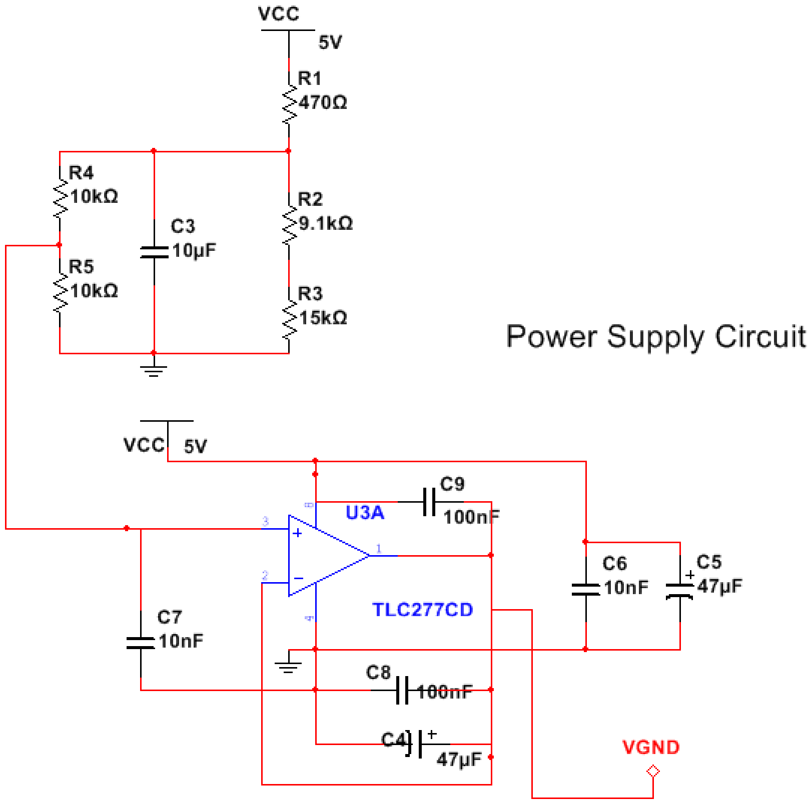
S.No	Circuit	Remarks	No. present
1	Power Supply Circuit	Consumes 9V DC from Battery and supplies 5V, 2.5V and GND terminals	1 No.
2	Instrumentation Amplifier Circuit	Input from 3.5MM jack is supplied to Instrumentation amplifier present in each channel to improve CMRR and Gain by a factor of 12.36	1 per channel
3	50Hz Notch	Output of Instrumentation Amp is stripped of 50Hz hum. Gain is Unity.	1 per channel
4	Low Pass Filter (1-125 Hz)	Rejects signals of Frequencies > 125Hz; Unity Gain	1 per channel
5	Gain Stage	Improves the Gain of the incoming signal to a final variable factor of 7000 - 15000, making it usable for Analog-Digital Converter modules	1 per channel

2.3 Simulation Software and Parameters

National Instruments MultiSim v13.0 (Trial Version) was used for simulating the Bio-signal Amplifier Circuit. AC Analysis was carried out and the frequency response was obtained to satisfy the requirements. Throughout this simulation, TLC277 Dual Op-Amp is used in place of AP358. The simulation is performed for a single channel. Throughout the document, the **X and Y axes in the output graphs are in logarithmic and decibel scales respectively**.

2.4 Simulation Circuit

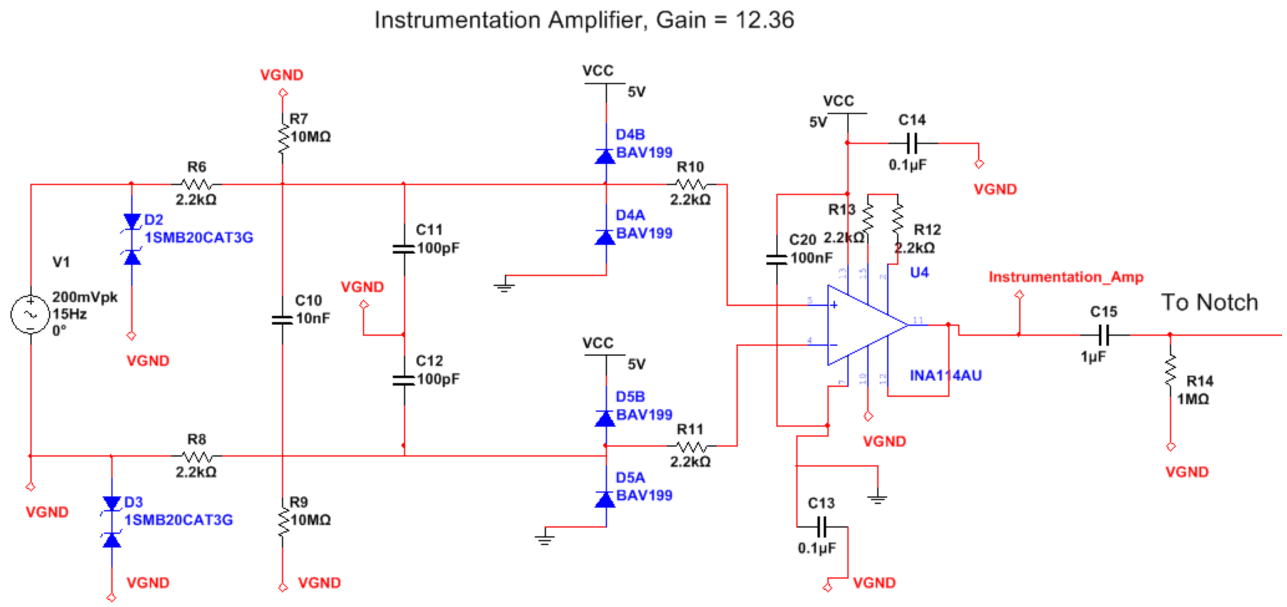
2.4.1 Power Supply Circuit



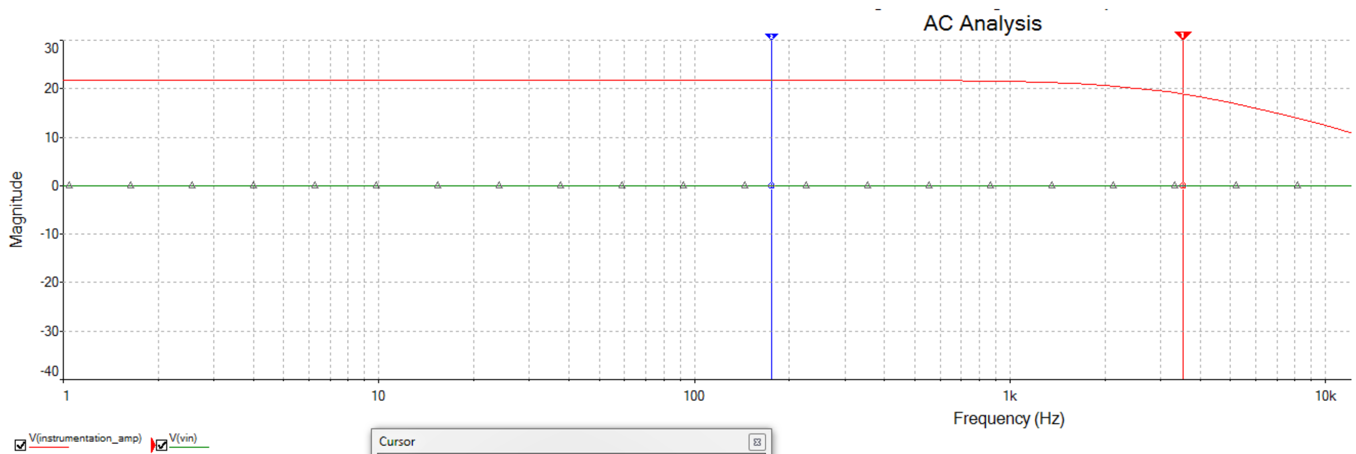
The power supply circuit consists of a 5V input, which is assumed to have come from a 9V Battery / Voltage Regulator / DC-DC Converter circuit. The output of the power supply circuit provides three terminals: Vcc, VGND and AGND. AGND is Actual Ground or negative terminal of the battery. VGND is a virtual/lifted ground that caters as the 0V level for all components in the board. Since Op-Amps in the board require a negative power supply, AGND acts as a negative supply source (-Vcc) while VGND acts as 0V source (GND).

2.4.2 Instrumentation Amplifier Stage

The input (differential mode) signals from electrodes are sent to the Instrumentation Amplifier for Common Mode noise reduction and amplification and through Dual Diodes and ESD suppressors. The instrumentation amplifier chip INA114 amplifies the input by a factor of 12.36. The output of this stage is fed to the 50Hz notch filter for eliminating the 50Hz hum seen in the signals because of power lines.



As seen in the response below, the output signal (red) is 12.36 times the input, represented in Decibel scale (20 log (12.36) = 21.8). The red cursor indicates the gain at -3dB point, which is 18.8 dB at 3.5 kHz.

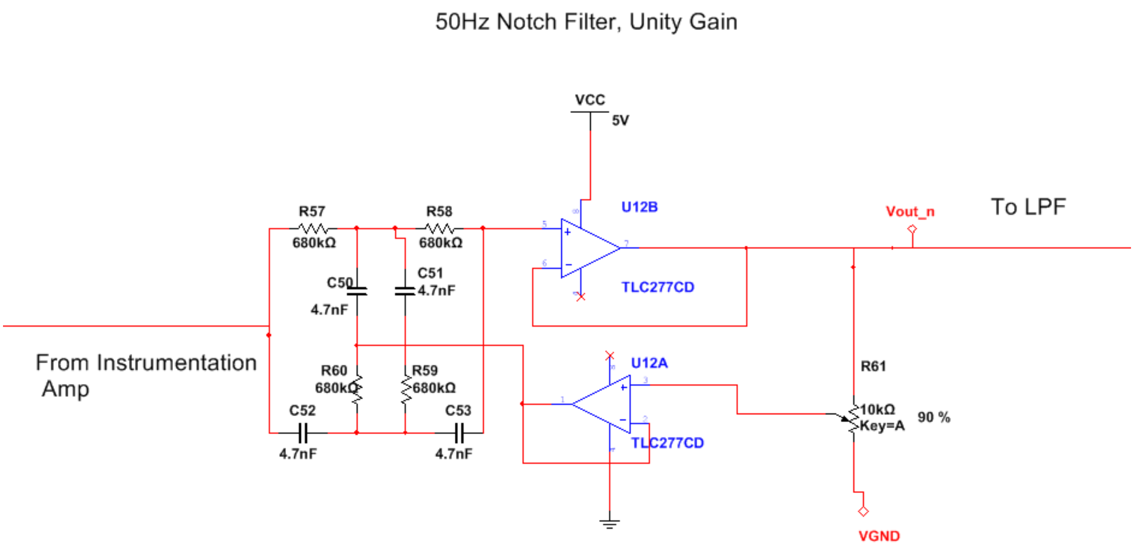


Cursor

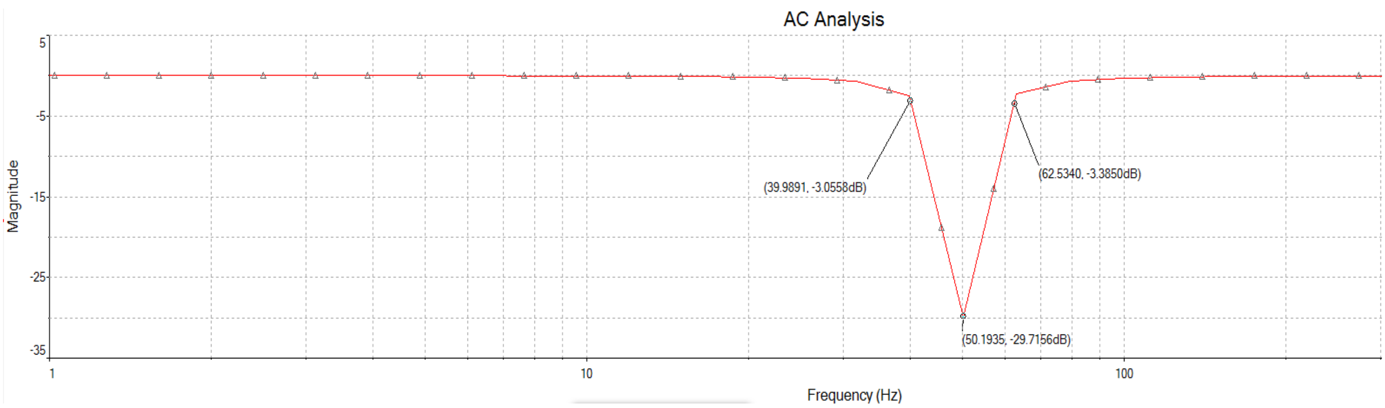
	V(instrumentation_amp)	V(vin)
x1	3.5327k	3.5327k
y1	18.8691	728.5396µ
x2	175.5191	175.5191
y2	21.8300	92.5103µ
dx	-3.3572k	-3.3572k
dy	2.9609	-636.0293µ
dy/dx	-881.9567µ	189.4528n
1/dx	-297.8680µ	-297.8680µ

2.4.3 50Hz Notch filter

As the name goes, the notch filter rejects 50Hz waves from the signal. The value 50 Hz is determined by the RC Combination. The gain is Unity.

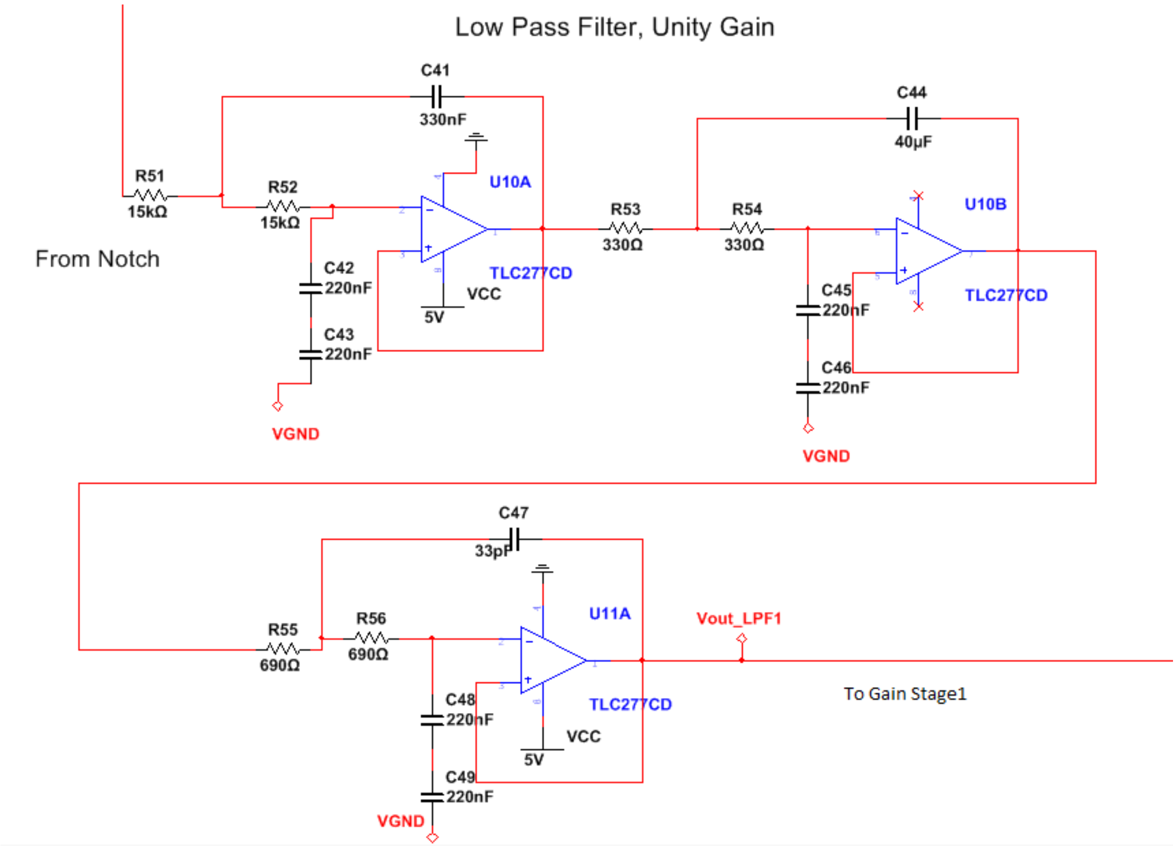


The plot below shows the response of the notch filter. At 50 Hz, the attenuation is 30 dB. The -3dB bandwidth is approximately 12 Hz (F_H - F_L) where F_L is 40 Hz and F_H is 62 Hz.

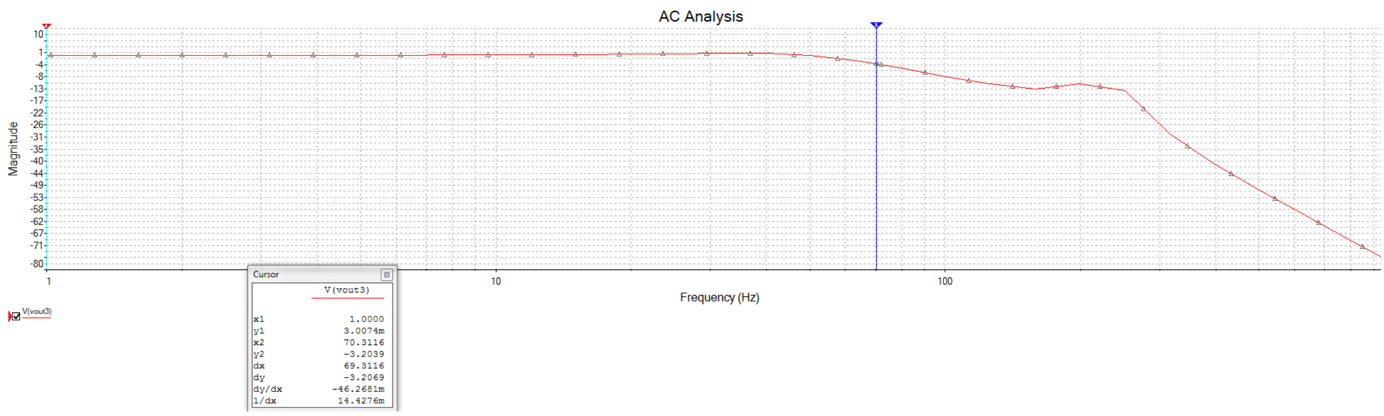


2.4.4 Low Pass Filter

The Unity Gain Low Pass filter is a 3-stage active filter intended to cut-off at 125Hz.

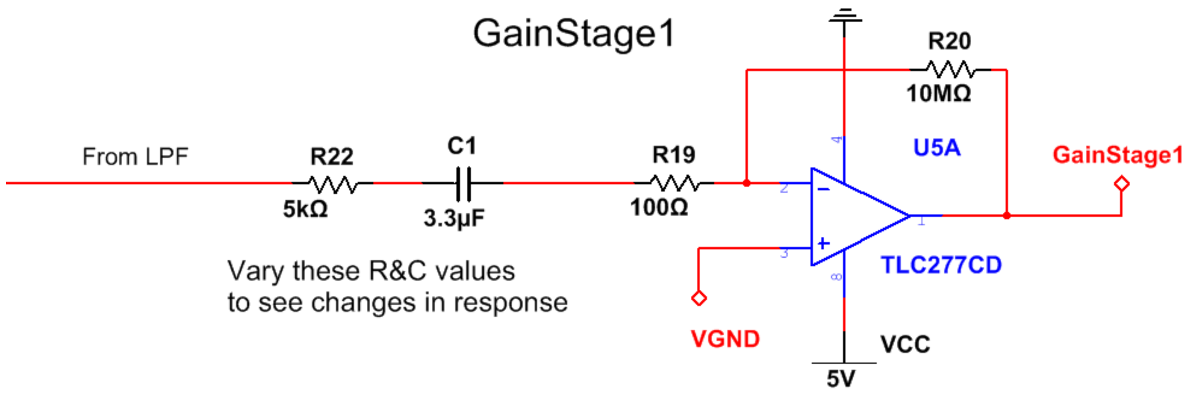


The -3 dB point of the low pass filter, as shown below, is situated at 70 Hz and it continues to attenuate the signals at frequencies beyond 70Hz.

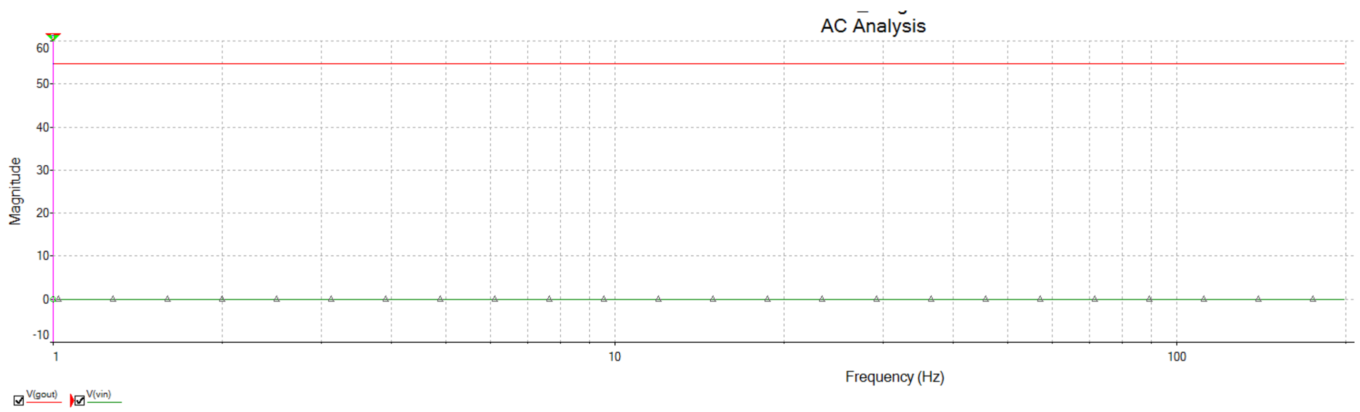


2.4.5 Gain Stage

The gain stage improves the gain of the input signal by a factor of $10^3(V_o/V_{in})$ to make it usable by ADC stages that may follow the Bio-Amp. Typically the output signals have a peak-to-peak magnitude of 0.5 to 2V. The R & C values determine the characteristics of the output waveform.

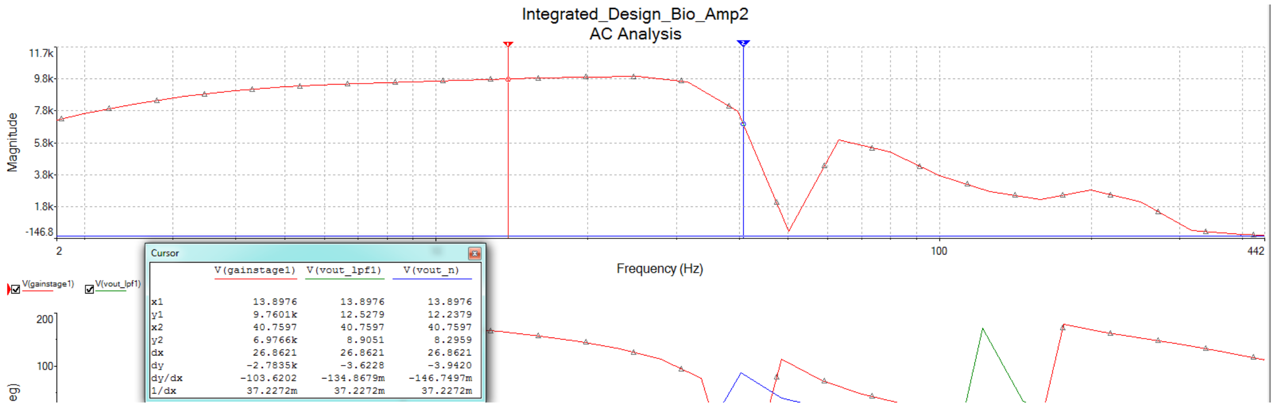


The gain of this stage as seen in the circuit is variable. The plot below shows V_{OUT} = 55 dB, which is 1000 times the input as seen in the circuit (20 log (10M/10.1k)).



2.5 Simulation Output

The output of GainStage1 (V_o/V_{in}), the final stage in the Bio-Amp is plotted on y-axis with Frequency on x-axis, in logarthmic scale. As shown, the gain begins to roll-off completely after 125Hz and is also notched at 50Hz. The gain in the operating range is shown as 9500, which is actually variable from 7000 to 15000.



3.0 PCB Schematic and Layout Design

Following the simulation, PCB schematic was designed to accommodate 2 channels in a 2-Layer Bio-Amp card of 10cm x 5cm dimension. The PCB schematic was done with Cadence Allegro Design Entry CIS and PCB Layout was done with Cadence Allegro PCB Editor Suite v16.6. PCB Design and Layout was done in-house while fabrication was done by 3rd party vendors.

3.1 PCB Schematic

The schematic for PCB has been laid out in Cadence Allegro Design Entry CIS v16.6 for two channels. SMD packages of ICs have been used along with resistors and capacitors of 0805 package.

3.2 PCB Layout

The following are the Gerber files of different layers of the final PCB Layout of the Bio-Amp board that was sent to the manufacturer. The Gerber files are of RS-274X format.

3.3 Layout Design Data

Etch Track Parameters:

	Minimum	Maximum
Etch Track width (all nets)	0.5 mm	0.6 mm
VCC, VCC1, VGND line width	0.75 mm	1 mm

Min neck width (all nets)	0.38 mm
VCC, VCC1, VGND min neck width	0.43 mm
Max Neck length (all)	20mm

Spacing Parameters

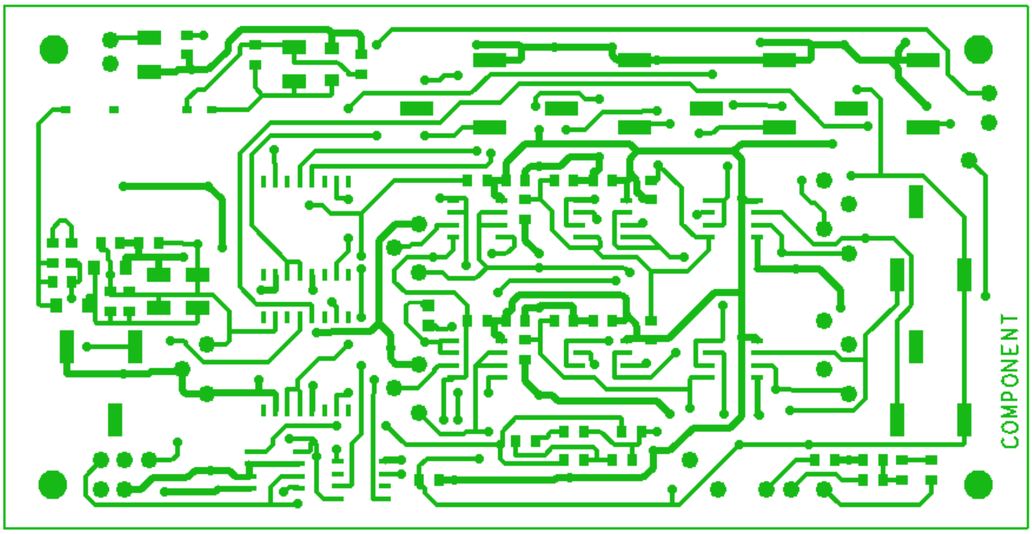
Line to line spacing	0.38 mm
Line to Thru pin spacing	0.38 mm
Line to SMD pin spacing	0.38 mm
Thru pin to Thru Via spacing	0.40 mm
SMD pin to Thru Via spacing	0.40 mm

Drill dimensions

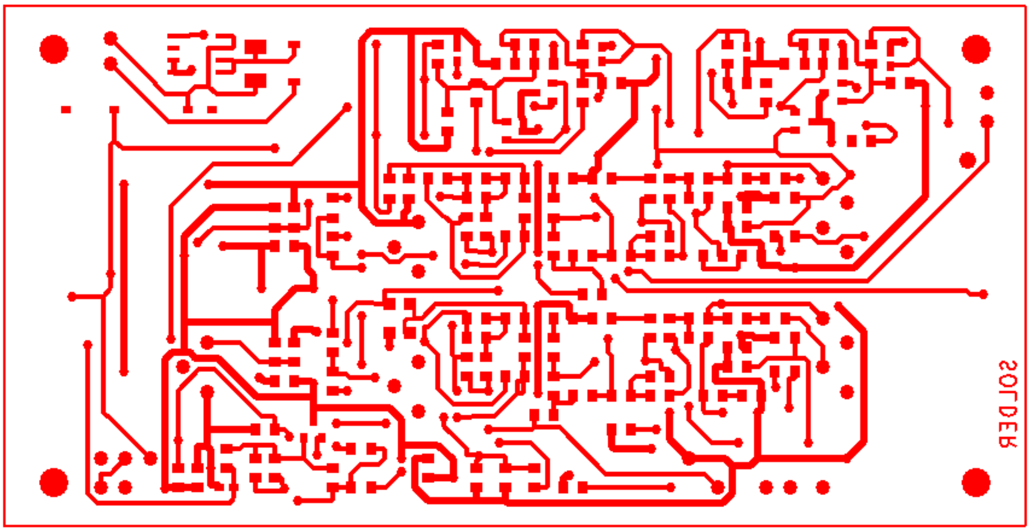
VIA Drill diameter	0.6096 mm
VIA Regular pad diameter	1 mm
Thru Pin Drill diameter	0.9 mm
Thru Pin Regular pad diameter	1.8 mm

All other parameters that are not mentioned above have their respective default values, given by the software.

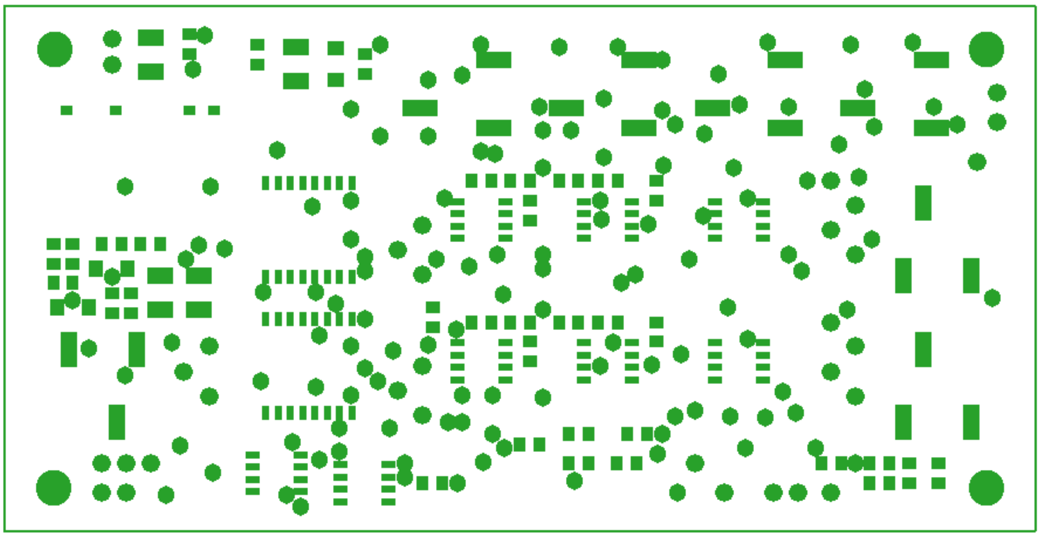
3.3.1 ETCH-TOP



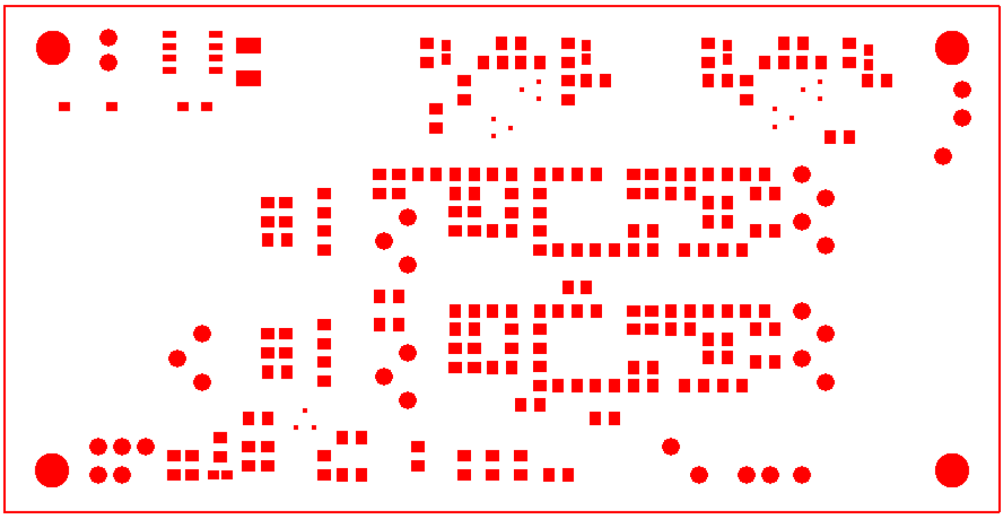
3.3.2 ETCH-BOTTOM



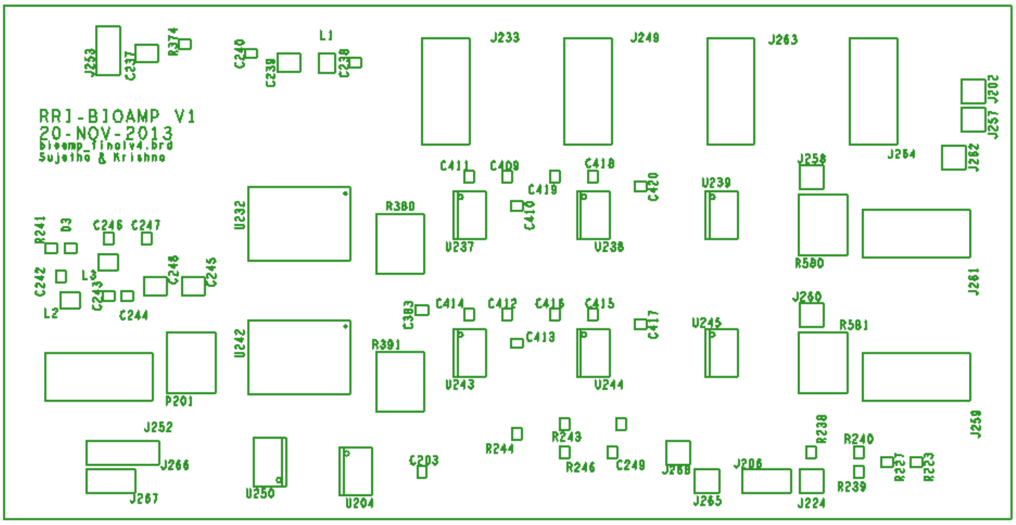
3.3.3 SOLDERMASK-TOP



3.3.4 SOLDERMASK-BOTTOM



3.3.5 SILKSCREEN-TOP



3.3.6 SILKSCREEN-BOTTOM