# Paolo A. Gargini

Dr. Gargini was born in Florence, Italy and received a doctorate in Electrical Engineering in 1970 and a doctorate in Physics in 1975 from the Universita di Bologna, Italy, both with full honor and marks.

**1972** Post-Doc at Stanford.

**1974** Fairchild R&D, Paolo Alto.

October **1978**, Joined Intel.

April **1980**, he was responsible for developing the building blocks of HMOS III and CHMOS III technologies used in the 1980's for the **80286 and the 80386 processors**.

September **1985,** he headed the **first submicron** process development team at Intel.

April **1996,** Chairman of the Executive Steering Council (ESC) of **I300I** and, subsequently, of International Sematech from 1996 to 2000.

July **1998, Chairman** of the International Technology Roadmap for Semiconductors **(ITRS)**.

He has served as a member of advisory boards of Sematech, the Semiconductor Research Corporation (SRC), and the Technology Strategic Council (TSC) of the SIA in the US, IMEC in Europe, ASET and MIRAI in Japan.

April **2000,** Chairman of International Consortia Cooperation Initiative **(ICCI)**.

**February 2001, Chairman of International EUV Initiative (IEUVI).**

September **2003**, Dr. Gargini was included by **EE Times** in a very selected group of Influencers of the semiconductor industry.

June **2005,** Chairman of the Governing Council of the Nano Electronics Research Initiative **(NRI)** of SIA.

**Chairman of IMEC Scientific Advisory Board (SAB).**

Dr. Gargini elevated to **IEEE Fellow in 2008**.

Dr. Gargini elevated to **IEC Fellow in 2009**.

**Chairman of IMEC (Belgium) Scientific Advisory Board since 2009**.

**December 2009, inducted in the Semiconductor Industry Hall of Fame of VLSI Research**.