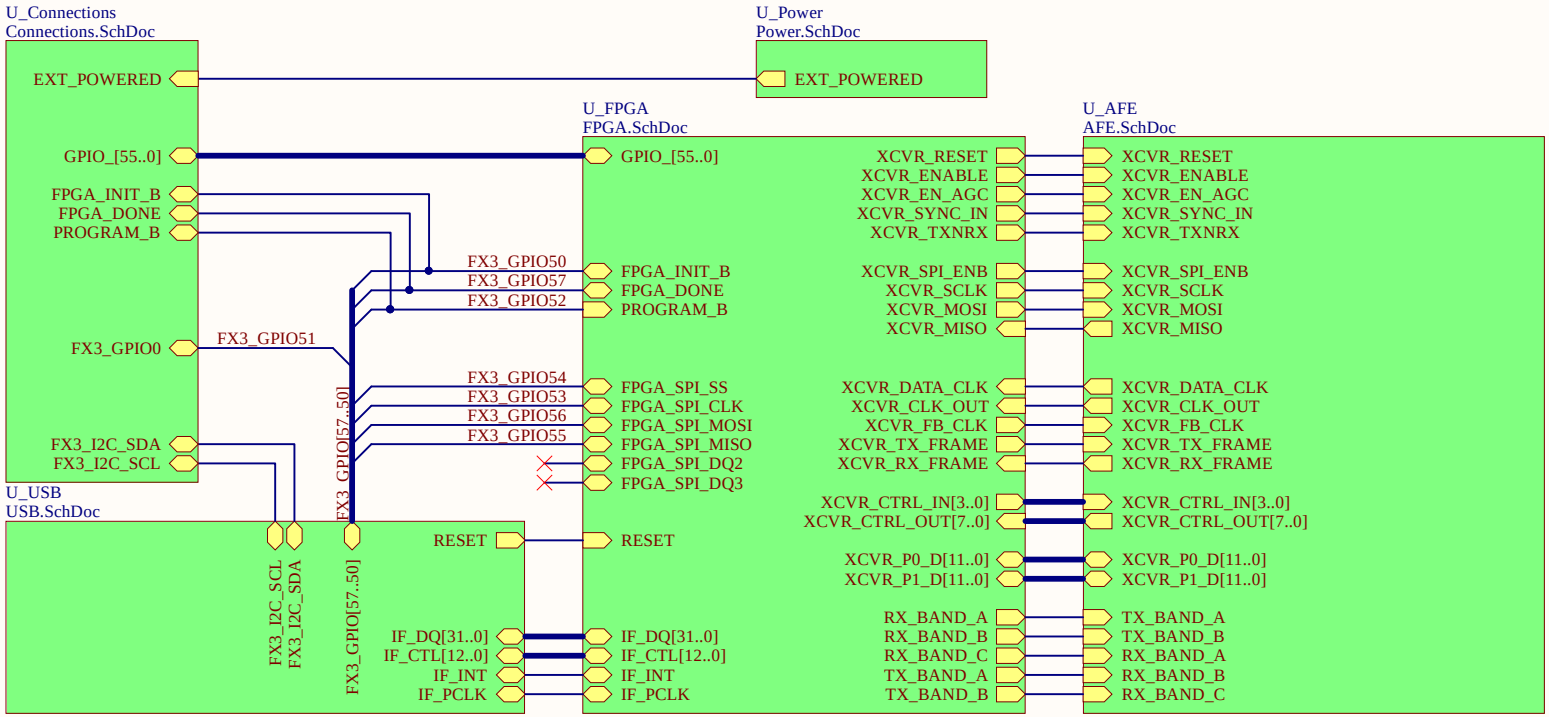
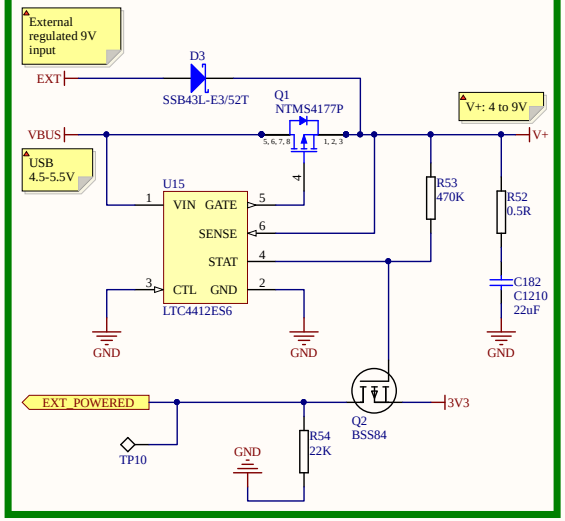


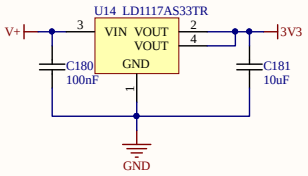
Title	**FreeSRP**	
Size: A4	Number: **1**	Revision: **2**
Date: 29/02/2016		Sheet 1 of 7
File: C:\Users\..\FreeSRP.SchDoc		Drawn By: Lukas Lao Beyer

IMPORTANT:
Check out layout & stencil recommendations in datasheet

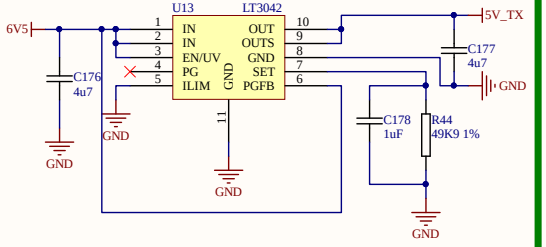
BUS/EXTERNAL POWER SELECTION



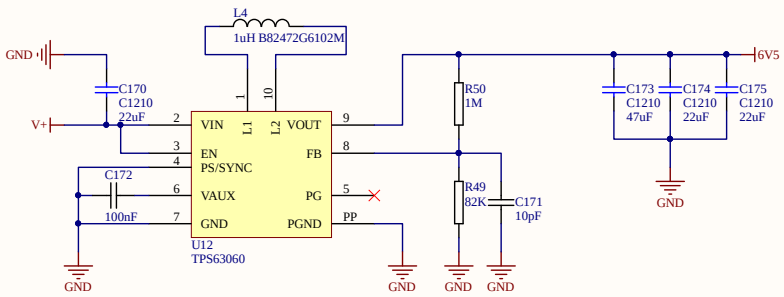
3V3: 3.30V, 0.8A



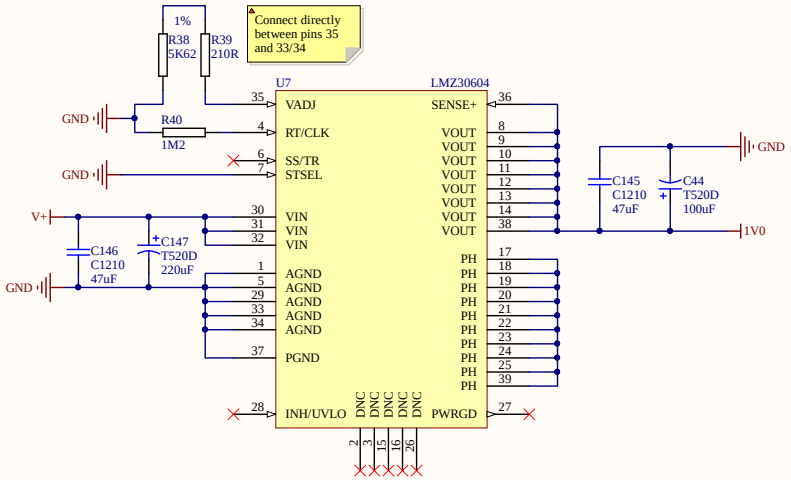
5V_TX: 5.00V, 0.2A



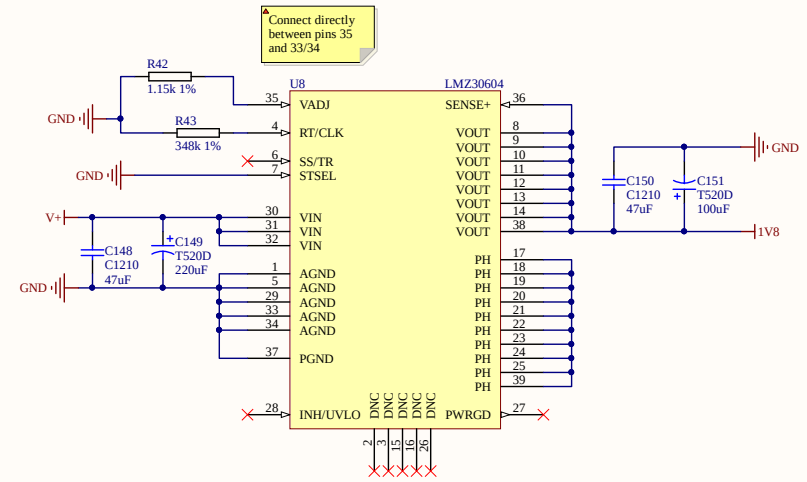
6V5: 6.50V, 1A



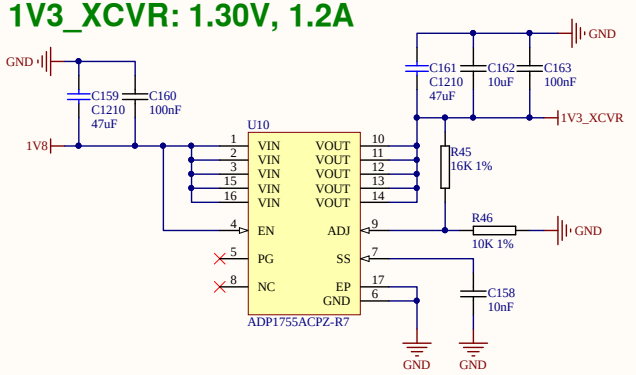
1V0: 1.00V, 4A



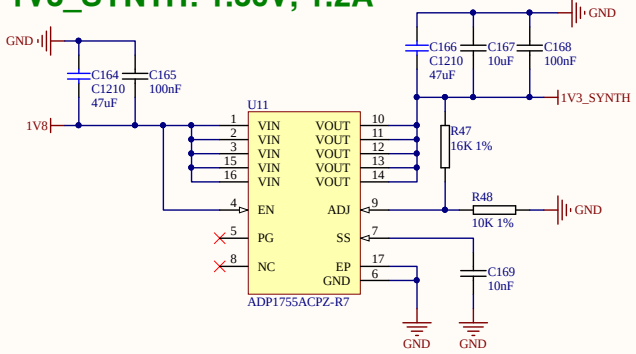
1V8: 1.80V, 4A



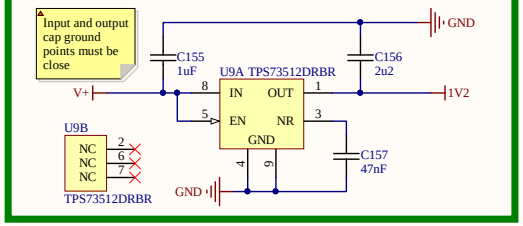
1V3_XCVR: 1.30V, 1.2A



1V3_SYNTH: 1.30V, 1.2A

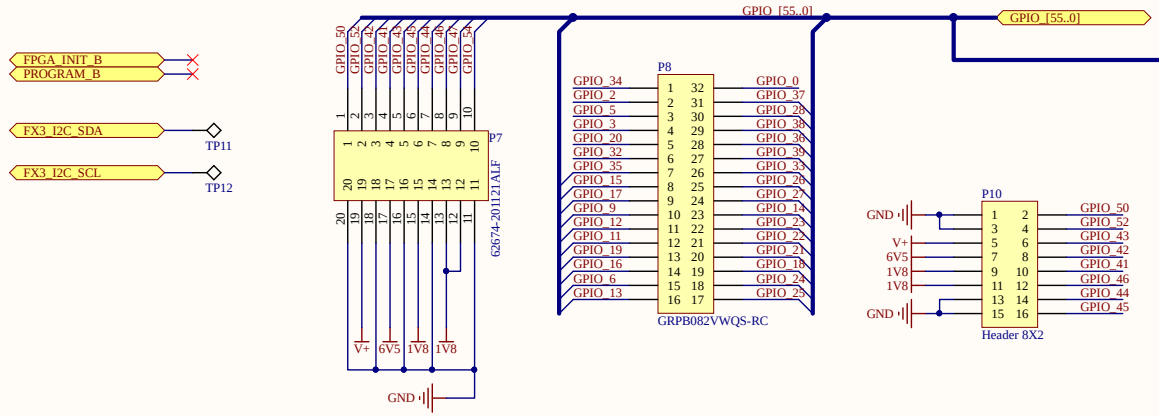


1V2: 1.20V, 0.5A



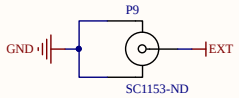
Title: **Power**		
Size: A3	Number: **2**	Revision: **2**
Date: 29/02/2016		Sheet 2 of 7
File: C:\Users\..\Power.SchDoc		Drawn By: Lukas Lao Beyer

EXPANSION HEADERS



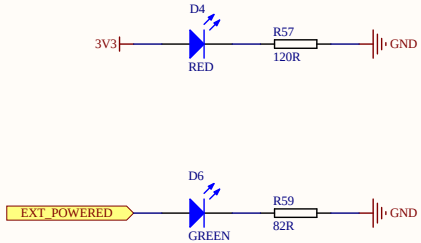
EXTERNAL POWER

6V REGULATED INPUT



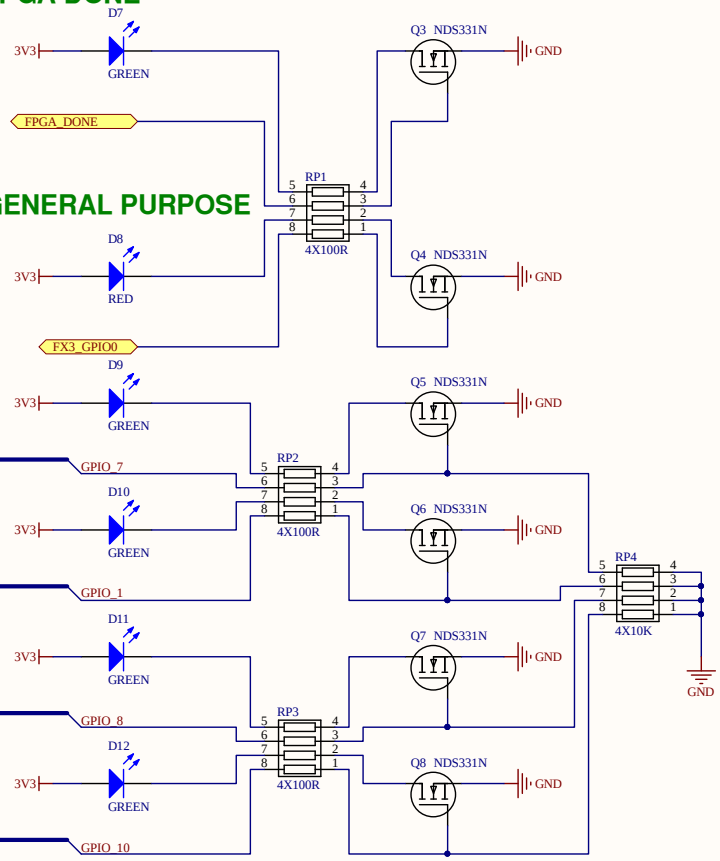
LED INDICATORS

POWER INDICATORS

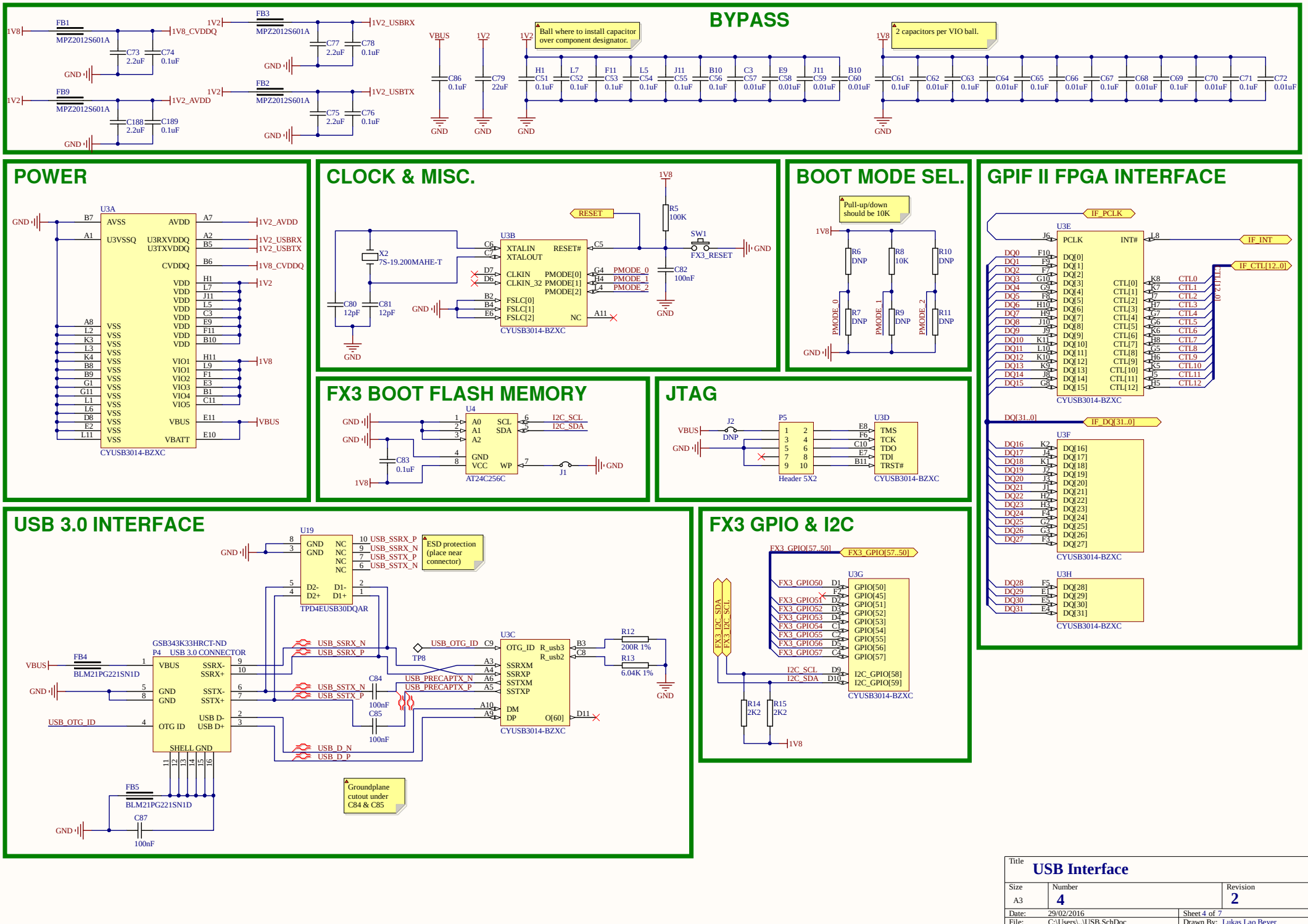


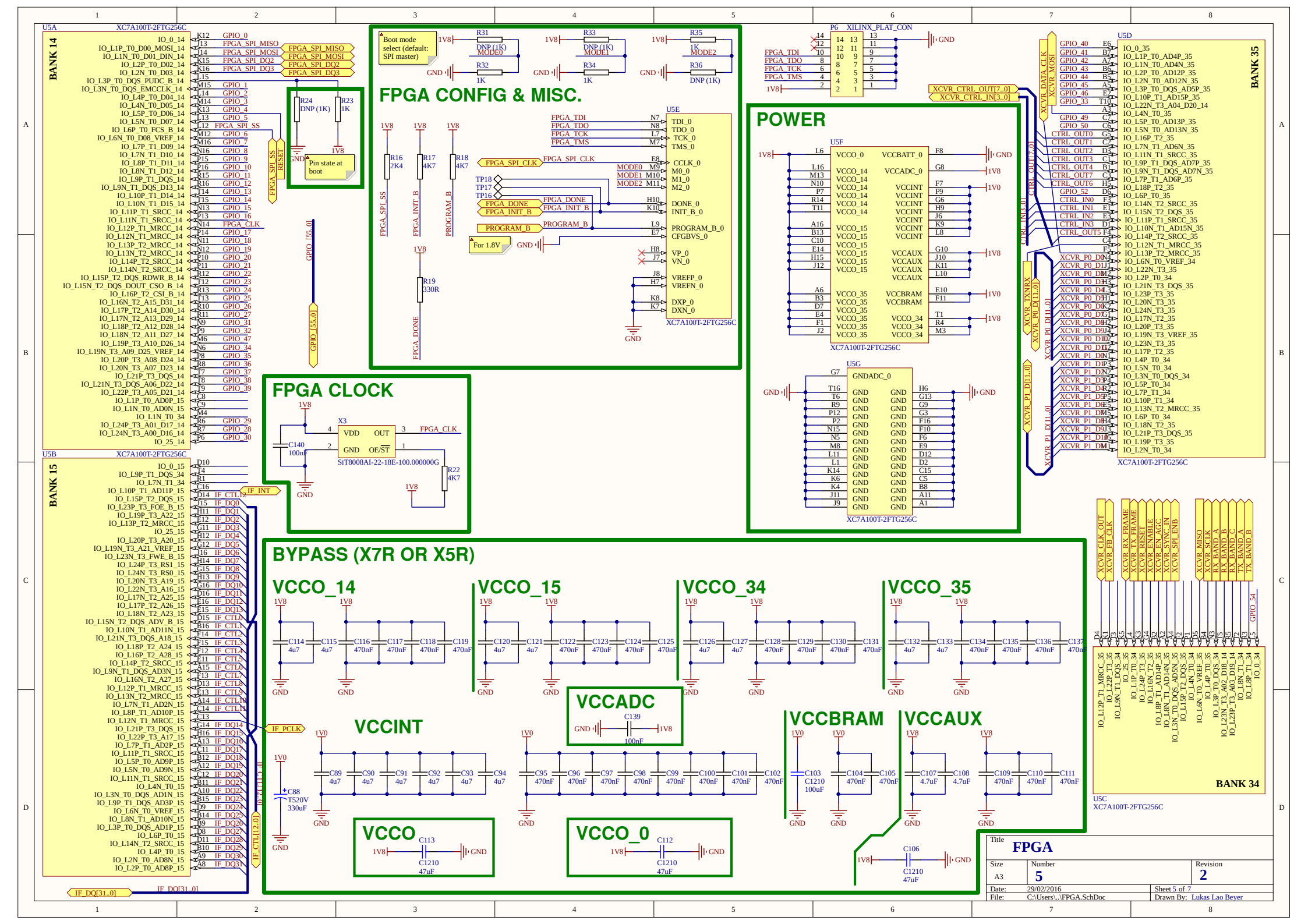
FPGA DONE

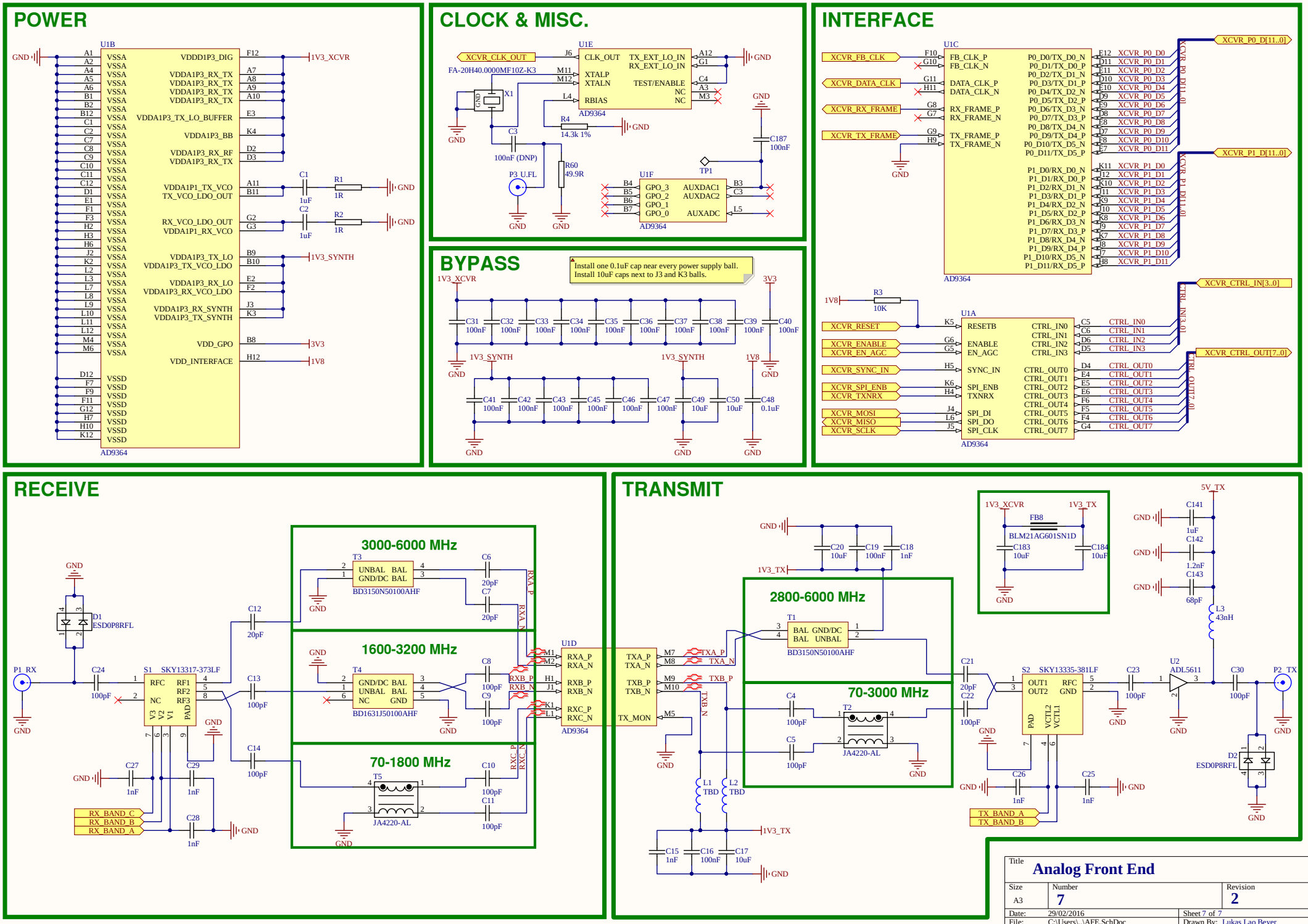
GENERAL PURPOSE



Title	**Expansion Connectors and Status LEDs**	
Size: A3	Number: **3**	Revision: **2**
Date: 29/02/2016	Sheet 3 of 7	
File: C:\Users\..\Connections.SchDoc	Drawn By: Lukas Lao Beyer	


BYPASS
POWER
CLOCK & MISC.
BOOT MODE SEL.
GPIF II FPGA INTERFACE
FX3 BOOT FLASH MEMORY
JTAG
USB 3.0 INTERFACE
FX3 GPIO & I2C
Ball where to install capacitor over component designator.
2 capacitors per VIO ball.
Pull-up/down should be 10K
ESD protection (place near connector)
Groundplane cutout under C84 & C85
CYUSB3014-BZXC
TPD4EUSB30DQAR
AT24C256C
GSB343K33HRCT-ND
P4 USB 3.0 CONNECTOR
Header 5X2
Title
USB Interface
Size
A3
Number
4
Revision
2
Date: 29/02/2016
File: C:\Users\..\USB.SchDoc
Sheet 4 of 7
Drawn By: Lukas Lao Beyer


FPGA CONFIG & MISC.
POWER
FPGA CLOCK
BYPASS (X7R OR X5R)
VCCO_14
VCCO_15
VCCO_34
VCCO_35
VCCADC
VCCINT
VCCBRAM
VCCAUX
VCCO
VCCO_0
BANK 14
BANK 15
BANK 35
BANK 34
U5A XC7A100T-2FTG256C
U5B XC7A100T-2FTG256C
U5C XC7A100T-2FTG256C
U5D
U5E XC7A100T-2FTG256C
U5F XC7A100T-2FTG256C
U5G XC7A100T-2FTG256C
P6 XILINX_PLAT_CON
X3 SiT8008AI-22-18E-100.000000G
Boot mode select (default: SPI master)
Pin state at boot
For 1.8V
Title FPGA
Size A3
Number 5
Revision 2
Date: 29/02/2016
File: C:\Users\..\FPGA.SchDoc
Sheet 5 of 7
Drawn By: Lukas Lao Beyer


POWER
CLOCK & MISC.
INTERFACE
BYPASS
Install one 0.1uF cap near every power supply ball.
Install 10uF caps next to J3 and K3 balls.
RECEIVE
3000-6000 MHz
1600-3200 MHz
70-1800 MHz
TRANSMIT
2800-6000 MHz
70-3000 MHz
Title
Analog Front End
Size
A3
Number
7
Revision
2
Date:
29/02/2016
File:
C:\Users\..\AFE.SchDoc
Sheet 7 of 7
Drawn By:
Lukas Lao Beyer