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fitlet GPIO Connector

User guide

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Revision History

Revision	Author/Engineer	Revision Changes
0.99	Maxim Birger	Preliminary release
1.0	Maxim Birger	Initial public release
1.1	Maxim Birger	Update cable color code tables to correspond reverse order assembly
1.2	Maxim Birger	Update after fitlet GPIO SDK ready. Fix GPIO and pinout tables.
1.3	Maxim Birger	Added GPIO drive strength information

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1 Introduction

1.1 About This Document

This document is part of a set of reference documentation necessary to operate fitlet optional periphery, as GPIOs and interfaces available.

1.2 Related Documents

Document	Link
Fitlet GPIO SDK for Linux	http://fit-pc.com/wiki/index.php/Fitlet_GPIO_SDK_for_Linux
Fitlet GPIO SDK for Windows	http://fit-pc.com/wiki/index.php/Fitlet_GPIO_SDK_for_Windows

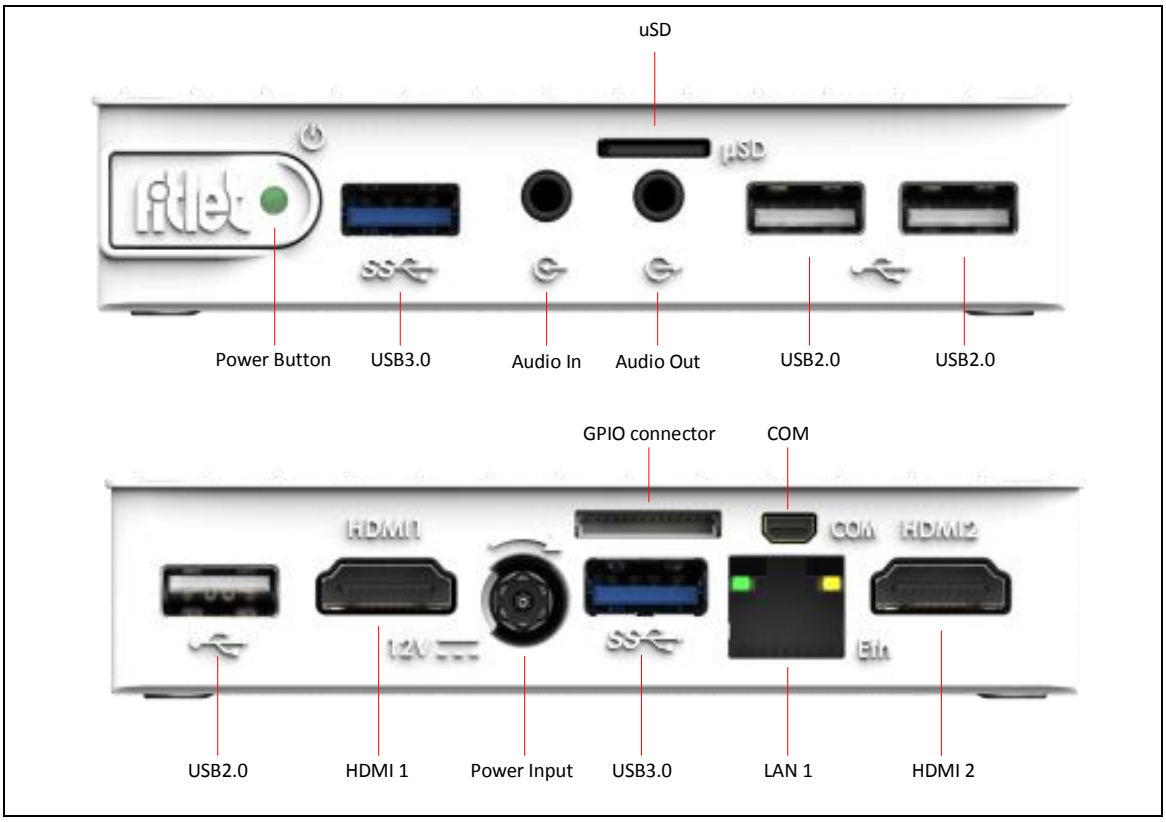
2 Fitlet GPIO Connector

fitlet GPIO interface provides easy and convenient way to operate external devices without the need to open the box, solder wires and designs special hardware. The interface accessible from fitlet's back panel connector via 14-pin ribbon cable (sold as accessory).

2.1 Fitlet Port View

Fitlet front and back panel ports shown in the figure below.

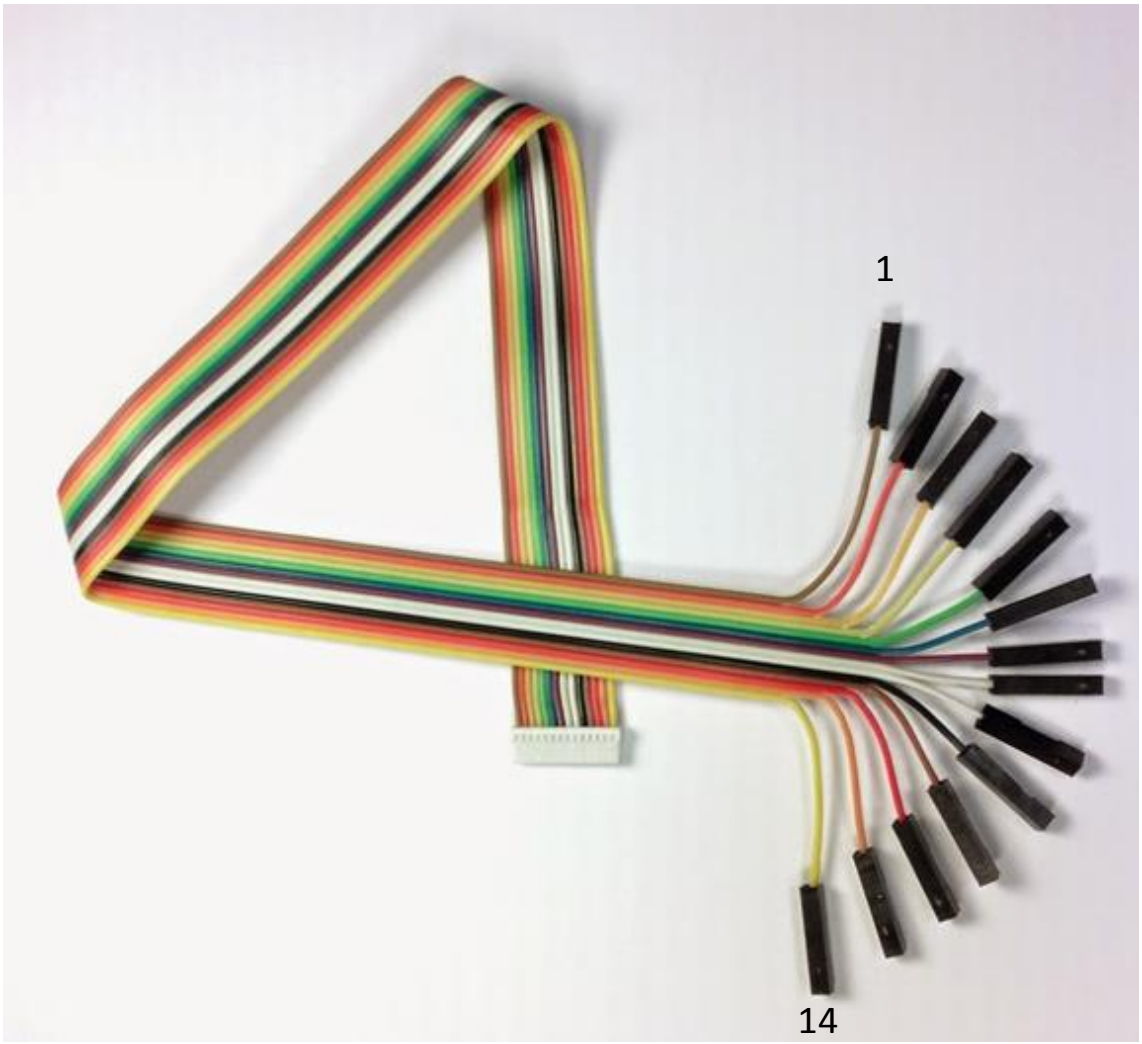
Figure 1 – fitlet front/back panel ports



2.2 Ribbon Cable

The ribbon cable provides easy GPIO connection and signals spreading. On one end it connects to GPIO connector and on the other spreads each signal to its own 1x1 header.

Figure 2 – fitlet GPIO ribbon cable



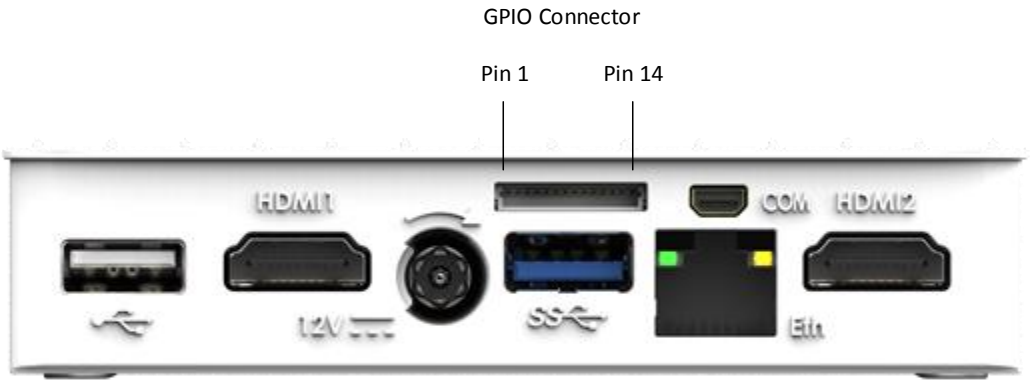
3 GPIO Configuration

3.1 GPIO Connector Pinout and Color Map

Fitlet GPIO connector (P49) pinout, as well as signal drivers/receivers with the default and configured function provided below.

Table 1 – GPIO connector pinout

GPIO Connector		Source	GPIO#/ Function	GPIO# in Linux Kernel	Power domain	Direction	Pull (PU/PD)
Pin Number	**Color Code**						
1	Brown	SoC	GPIO_1	GPIO89	3.3V	In	PU
2	Red	SoC	GPIO_2	GPIO132	3.3V	In	PU
3	Orange	SoC	GPIO_3	GPIO65	3.3V	Out High	PU
4	Yellow	SoC	GPIO_4	GPIO66	3.3V	Out High	PU
5	Green	SoC	GPIO_5	GPIO29	1.5V	In	PD
6	Blue	SoC	I^2C Clock		3.3V		
7	Purple	SoC	I^2C Data		3.3V		
8	Grey	SoC	GPIO_6	GPIO73	3.3V	Out Low	PD
9	White	SoC	GPIO_7	GPIO27	1.5V	In	PD
10	Black	SoC	GPIO_8	GPIO28	1.5V	In	PD
11	Brown	SoC	GPIO_9	GPIO12	3.3V	In	PU
12	Red	SuperIO	UART Rx		3.3V		
13	Orange	SuperIO	UART Tx		3.3V		
14	Yellow				GND		



3.2 GPIO Configuration Table

GPIO configuration table maps the available signals voltage, functionality, direction and other characteristics in default state (power up) and BIOS configured state.

Figure 3 – GPIO Reset and Configuration states table

GPIO#	Power domain	Functionality	Direction		Pull (PU/PD)	
		Reset state	Reset state	BIOS config. state	Reset state	BIOS config. state
GPIO_1	3.3V	GPIO	In	In	PU	PU
GPIO_2	3.3V	CLK_REQG_L	In	In	PU	PU
GPIO_3	3.3V	GPIO	In	Out High	PU	PU
GPIO_4	3.3V	GPIO	In	Out High	No Pull	PU
GPIO_5	1.5V	AZ_SDIN3	In	In	PD	PD
GPIO_6	3.3V	GPIO		Out Low		PD
GPIO_7	1.5V	AZ_SDIN1	In	In	PD	PD
GPIO_8	1.5V	AZ_SDIN2	In	In	PD	PD
GPIO_9	3.3V	IR_LED_L	In	In	PU	PU

Note: GPIO BIOS configuration settings are subject to changes. Please refer to up to date document for the latest information.

3.3 GPIO Drive Strength

GPIO drive strength value is configured via GPIO control registers and have 4 possible configurations: 4mA, 8mA, 12mA, 16mA

Warning: Proper ESD protection required to eliminate damage when operating fitlet with external hardware. Proper grounding required to provide stable signaling and avoid damage.
Do NOT operate the interface unless you know what you're doing!