Fully Differential Receiver Chipset for 40 Gb/s Applications Using GaInAs/InP Single Heterojunction Bipolar Transistors

K. Kızıloğlu, S. Seetharaman, K.W. Glass, C. Bil, H.V. Duong and G. Asmanis
Intel Corporation, Intel Communications Group
2200 Mission College Blvd., Santa Clara, CA 95052
kursad.kiziloglu@intel.com, shivakumar.seetharaman@intel.com

1. Introduction

Advent of multimedia applications, which require data links with ever-increasing capacity, is necessitating high-speed optical communication systems and driving research and development for high-speed ICs operating at 40 Gb/s. These optical fiber communication systems require high performance and low power chipsets, which incorporate useful service functions. Figure 1 illustrates a typical receiver block diagram. The transimpedance amplifier (TIA) converts the current variations generated by the photodetector to an amplified voltage swing at its output. A limiting amplifier, by providing a large dynamic range and a constant limited output, is generally utilized to further shape the signal received from the TIA. The serial high-bit rate data are then passed through a clock and data recovery stage (CDR) for further signal shaping and demultiplexed down to multiple parallel lanes at lower bit rates for easy interfacing with the transport / service ICs, such as de-framers, and finally passed on to network processors for further manipulation.

In this work, we report on the design and characterization of a fully-differential 40 Gb/s receiver chipset, which includes a transimpedance amplifier and a limiting amplifier for SONET/SDH STS-768/STM-256 applications. The chipset is realized using a GaInAs/InP single heterojunction bipolar transistor (SHBT) process with a nominal f_T > 150 GHz and f_{max} >180 GHz.

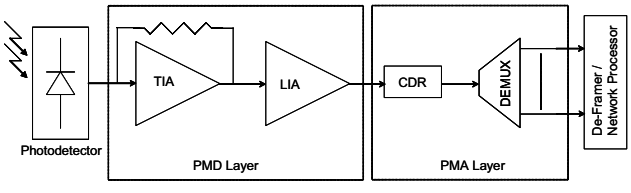

Fig. 1. System block diagram for an optoelectronic receiver.

2. Transimpedance Amplifier (TIA)

2.1. Design

A critical part of an optical receiver is the TIA as its noise, gain and frequency performance largely determines the overall data rate and the sensitivity that can be achieved in an optical system. TIA designs present an additional challenge in that to be able to accommodate wideband data, the amplifier has to have a wideband frequency response, extending from dc to high frequencies, while maintaining minimum in-band ripple and phase distortion. We have implemented the TIA in a fully differential configuration for good noise immunity, excellent common mode noise rejection and wide-band operation [1-2]. The architecture incorporates an innovative biasing circuitry, which increases the current with temperature, keeping transconductance constant to achieve a consistent gain-bandwidth performance at a broad range of temperature, supply and process corners [3]. Figure 2 shows the block diagram of the fully differential TIA architecture with single ended excitation [4].

2.2. Measurements

Figure 3 depicts the transimpedance (Z_T) of the TIA, which is computed from on-wafer *S*-parameter measurements. A single ended gain of 54 dBΩ and an unloaded bandwidth of more than 50 GHz are observed. Based on previously characterized detector and interconnect parasitics, we estimate the O/E bandwidth of the detector and the TIA combination to be more than 40 GHz. Figure 4 shows the single ended output return loss, which is better than 10 dB up to 50 GHz. Reverse isolation (s_{12}) is also shown. For transient measurements, the TIA was mounted on an evaluation board along with a commercially available *pin*-photodetector. Figure 5 shows

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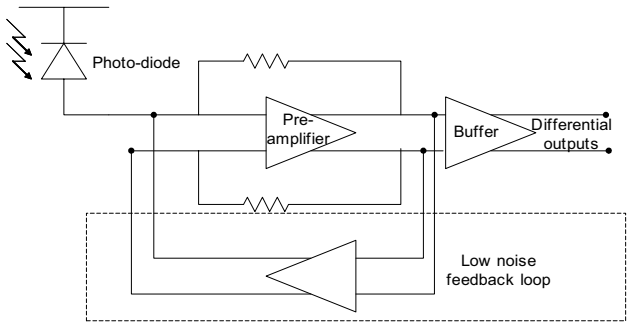

Fig. 2. TIA block diagram.

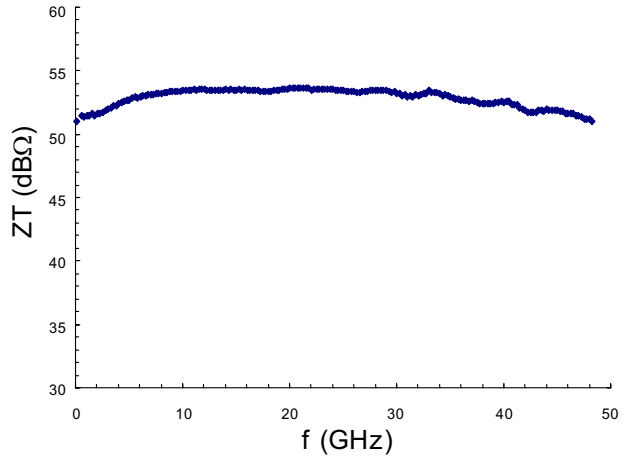

Fig. 3. Unloaded transimpedance (Z_T) gain of the TIA.

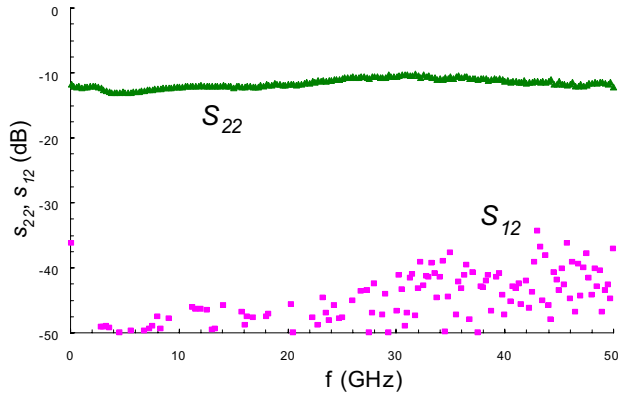

Fig. 4. Output return loss (s_{22}) and reverse isolation (s_{12}) measurements of the TIA.

a typical single ended output eye diagram at the input optical power level of -10.5 dBm. We also tested the TIA at the input optical power level of +3 dBm, which is the maximum our instrumentation can provide. Figure 6 shows typical single ended eye diagrams for each output at this maximum input power level. Clean and open eye diagrams are observed for both power levels. We expect the sensitivity and the performance of the TIA to improve

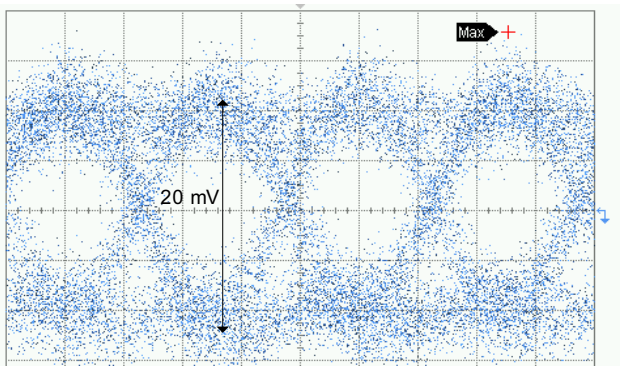

Fig. 5. Transient response of the TIA at 40 Gb/s and -10.5 dBm optical input power.

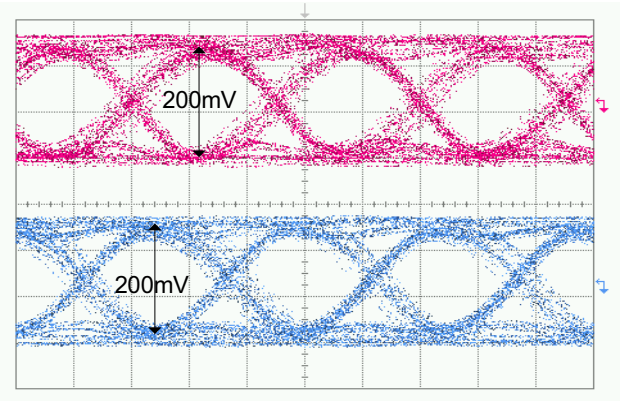

Fig. 6. Differential TIA outputs at 40 Gb/s and +3 dBm optical input power.

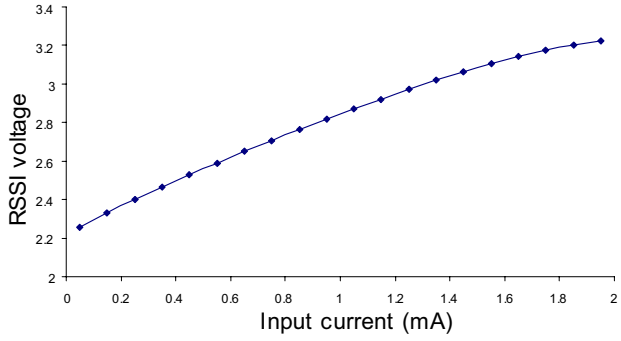

Fig. 7. Received signal strength indicator (RSSI) output of the TIA vs. input photodetector *dc* current.

with a better optimized interconnect between the detector and the TIA. The design also includes a new dc-feedback loop technique, which achieves a lower low cut-off frequency and reduces the input referred noise [5]. A received signal strength indicator (RSSI) function is also included on the chip to facilitate the automation of fiber alignment over photodiodes. Figure 7 shows the measured

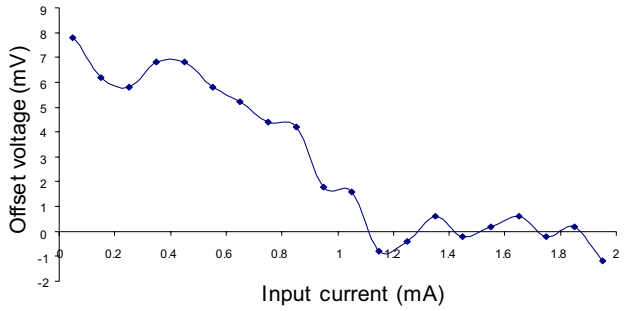

Fig. 8. Output offset voltage of the TIA vs. input photodetector DC current.

Z_T (differential gain)	Z_T (dBΩ)	Bandwidth (GHz)	DC power (mW)	Chip Size (mm^2)	Z_T-BW/mW
1000	60	50	290	1.0x1.0	172

Table 1. Performance matrix for the TIA.

RSSI output with respect to average input photodiode current. Figure 8 shows the dc voltage differential between the complementary outputs with respect to the average input photodiode current. An offset voltage of less than 8 mV is obtained for an average input current up to 2 mA (~4 mA peak-to-peak). To summarize, the TIA combines a constant g_m-biasing scheme, a robust and low-noise dc feedback loop technique and a carefully designed rf chain, thereby achieving excellent ac and dc performance (Table 1).

3. Limiting Amplifier (LIA)

3.1. Design

The output of the TIA in an optical receiver is generally small compared to the amplitude requirements for driving the succeeding clock and data recovery (CDR) and demultiplexer stages. The limiting post-amplifier (LIA), cascaded to the output of the TIA, performs the following functions: (i) provides additional voltage gain, (ii) cleans up the incoming signal, and (iii) presents a fixed output level independent of the input amplitude variations. The LIA was designed using a fully differential, cascode architecture. It comprises a number of cascaded gain stages as well as an offset correction and input slice level adjustment circuitry to accomplish broad gain and bandwidth characteristics with minimal output offset. It also sports an input common-mode threshold adjustment feature for ease of dc-coupling with the preceding chip.

3.2. Measurements

Prior to measurements on the LIA itself, the on-wafer measurement system was characterized. Figure 9 shows the system block diagram, along with the input and output eyes at 40 Gb/s. Due to the cable, connector and probe losses and bandwidth limitations, the output eye diagram of the system is degraded significantly compared to the input waveform. Figure 10 depicts the on-wafer characterization of the LIA, showing constant single-ended outputs for three different input levels and indicating limiting behavior over a minimum input dynamic range of 20 dB. Improvement in the LIA output eye diagrams over the underlying system response is also notable. The 40 mV and the 400 mV input levels represent the minimum and the maximum output levels of the TIA, demonstrating full compatibility between these two components. Figure 12 shows the performance of the slice adjust feature as a function of an external adjustment resistor. The circuitry can perform a slicing adjustment of ±25% around the nominal 50% level. This adjustment utility is necessary to correct a potential asymmetry of the 0 and 1 levels at the received input signal due to the nonlinearities of the optical link. As a final test of the entire receiver link, the TIA and the LIA evaluation boards were also connected together. Figure 11 shows the output eye diagrams of the receiver chipset with respect to two optical input levels. The performance of the LIA is summarized in Table 2.

Differential Gain (dB)	Sensitivity (mV)	Input dynamic range (dB)	DC power (mW)	Chip Size (mm^2)
36	40	20	640	2.0 x 1.4

Table 2. Performance matrix for the LIA.

4. Summary

In conclusion, we have reported a 40 Gb/s receiver chipset realized in GaInAs/InP single heterojunction bipolar transistor (SHBT) technology comprising a TIA and a LIA, with a combined power consumption of less than 1 W and a combined gain of 96 dBΩ. In addition to their excellent input sensitivity, overload protection, power and ac performance, both of these components pack many additional service features, such as offset correction, received signal strength indication (RSSI), input slice level and threshold adjustment. We therefore believe that this chipset is uniquely positioned to serve multiple 40 Gb/s receiver applications.

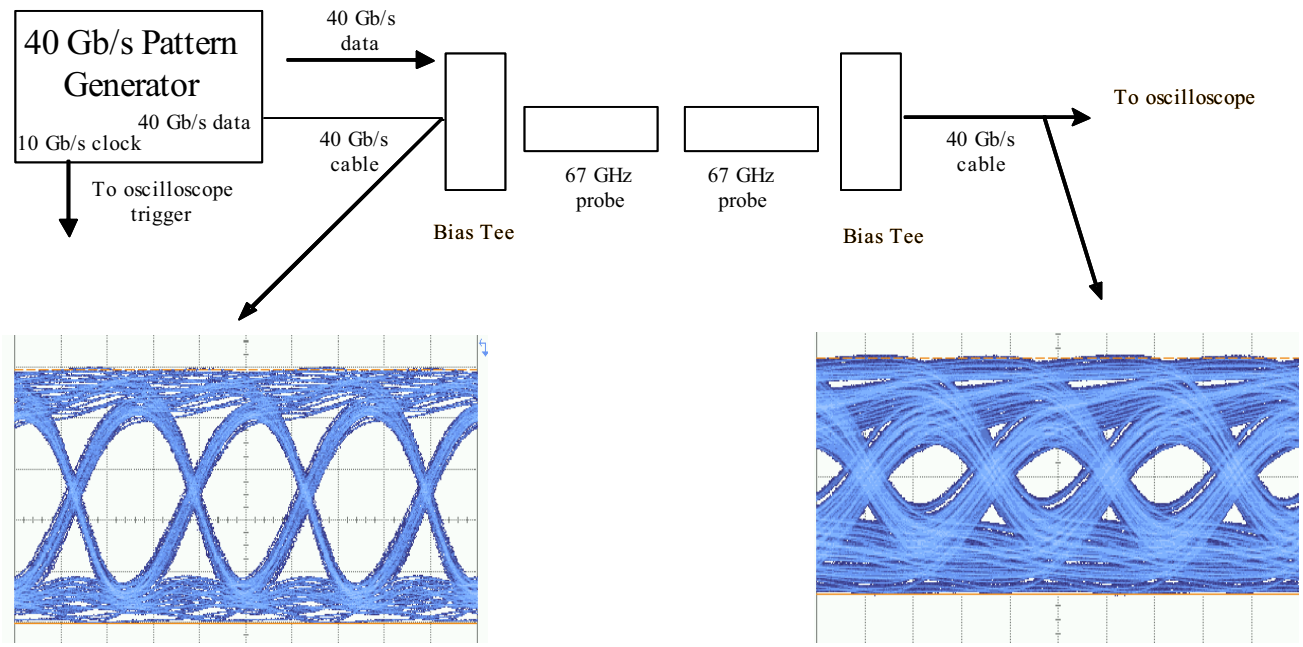

Fig. 9. 40 Gb/s on-wafer characterization system and its time domain response.

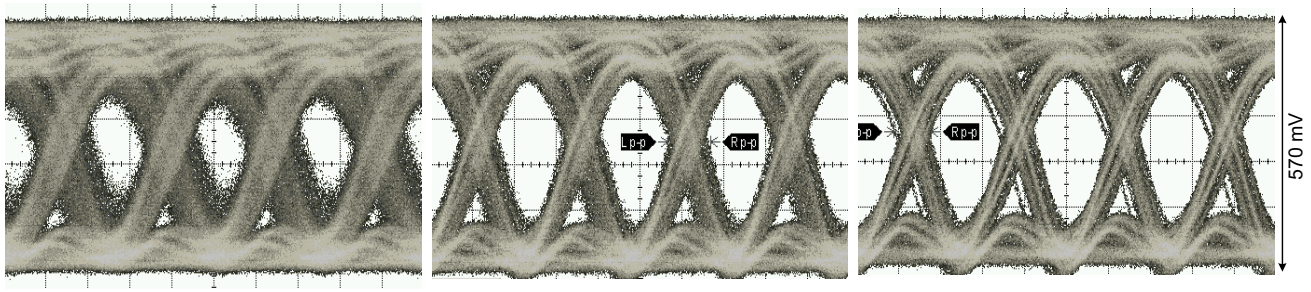

Fig. 10. On-wafer single ended LIA output measurements at 40 Gb/s with input amplitudes of 40 mVp-p (left), 80 mVp-p (center) and 400 mVp-p (right).

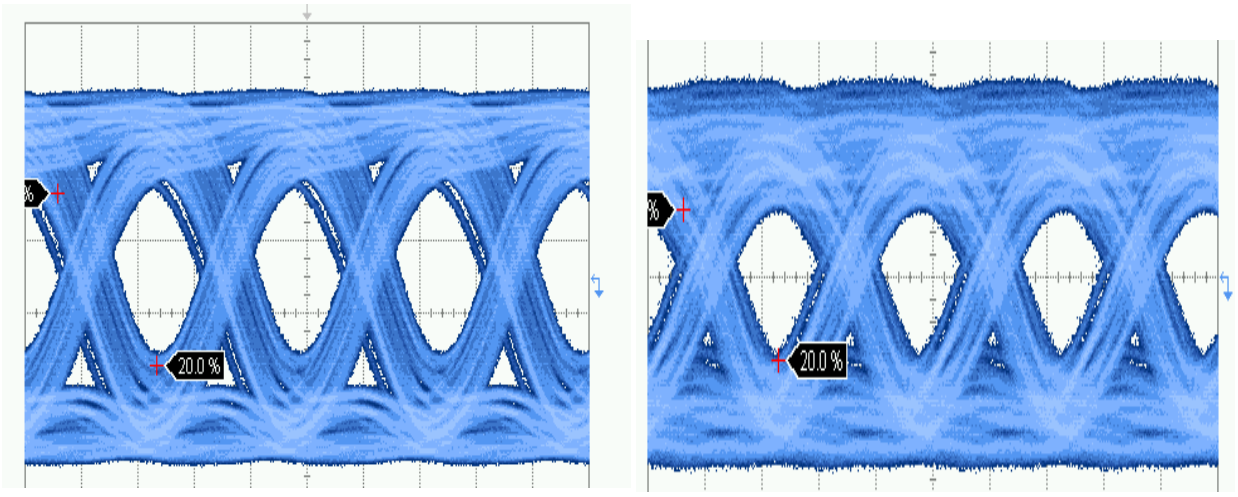

Fig. 11. Single ended receiver (combined TIA-LIA) output measurements at 40 Gb/s with an optical input power level of -8 dBm (left) and +3 dBm (right).

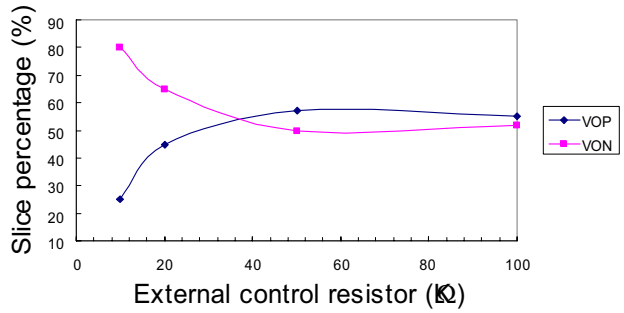

Fig. 12. Input slice level controllability (% variation from the nominal 50% level) as a function of external adjustment.

5. References

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