A Continuously Variable Digital Delay Element.

C. W. Farrow

AT&T
Middletown, New Jersey 07748

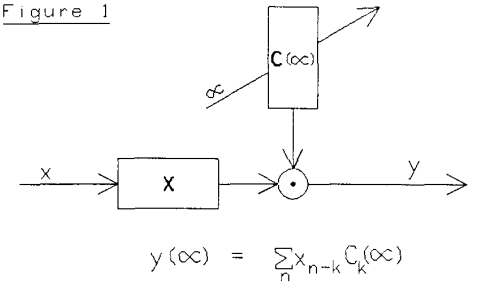
ABSTRACT

This paper describes a Finite Impulse Response (FIR) Filter which synthesizes a controllable delay. By changing the delay the filter has the ability to interpolate between samples in the data stream of a band-limited signal. The original motivation for this work was to provide a digital interpolator capable of compensating for the delay between echo canceller output and the receiver input for echo cancellation based modems, for example CCITT's V.32 modem. Another possible application is the transfer of data between quasi-synchronous T-carrier systems. The variable delay filter can also be used as a more general computational element. Because high sampling rates are not required, this filter is especially suited for implementation on a DSP (Digital Signal Processor). The interpolator has been implemented, in real time, on a WE® DSP20. This interpolator can also be used as a practical way to reconstruct an original band-limited signal from samples taken at the Nyquist rate.

1. INTRODUCTION.

A Continuously Variable Digital Delay (CVDD) Element has been built using an FIR filter whose tap coefficients are a function of the desired delay. This is represented in Figure 1. where T = tap spacing, αT = Delay.

Figure 1

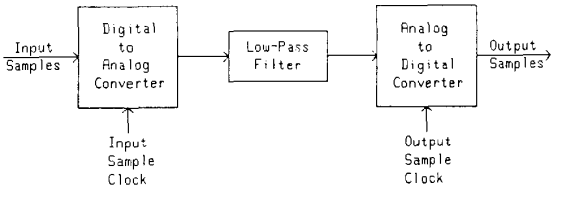


Vector Form of Continuously Variable Digital Delay.

To transfer digital samples of analog data from a system running under one clock to a system running under another clock requires an interpolator to compensate for delay between clocks.

One way to do this is to generate an analog signal by outputting the digital samples through a Digital-to-Analog Converter (DAC); pass the DAC output through a Low-Pass Filter and then re-sample the LPF output using an Analog-to-Digital Converter (ADC) (Figure 2).

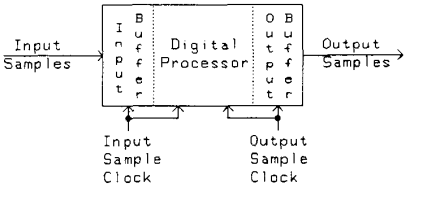
Figure 2.



ANALOG INTERPOLATOR.

A new approach, presented here, uses a DSP as a Continuously Variable Digital Delay (CVDD) (Figure 3). The "input" samples are sampled into the "input" buffer by the "input" clock. The DSP is synchronous with the "output" clock, which also measures the delay between the output and input clocks to give $\alpha = D/T$. The DSP has a delay line into which data samples are shifted. Normally just one *new* sample is shifted into the delay line from the input buffer.

Figure 3.



DIGTAL INTERPOLATOR.

If the delay parameter α overflows two *new* samples are shifted into the delay line; if α underflows then no new samples are shifted in. The interpolated samples generated by the DSP are then transferred to the "output" buffer.

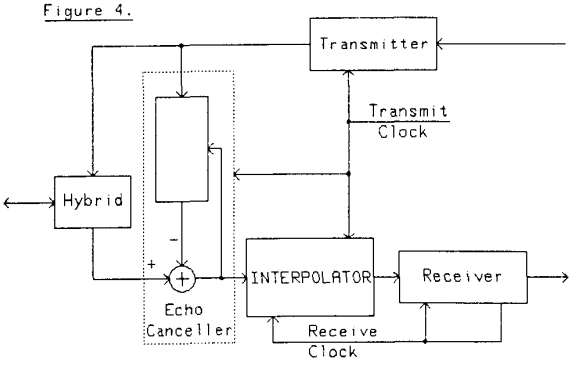
2. APPLICATIONS.

Following are some interpolation applications of the CVDD:

Echo Canceller.

The application that stimulated this work was the Echo Canceller (EC), used to cancel echoes of the local transmit signal in modems where the transmit and receive signals occupy the same spectrum [1]. A high-level architecture of the modem is shown in Figure 4. Without an EC, the receiver has no way to distinguish between the far-end signal and the echoes of the near-end signal.

Figure 4.



Architecture of Voice-Band Modem,

The EC operates under the transmit clock, because the signals from the transmitter are used as an "Ideal Reference" to generate a signal to cancel echo signals generated synchronously from the transmitted signal. The signals from the EC now have to be re-sampled at the Receive Clock rate, for processing in the receiver. Although the far transmitter operates at nominally the same rate as the near transmitter, their two signals are generated using separate crystal oscillators so that their phase difference may be constantly changing i.e. there is a slight frequency offset.

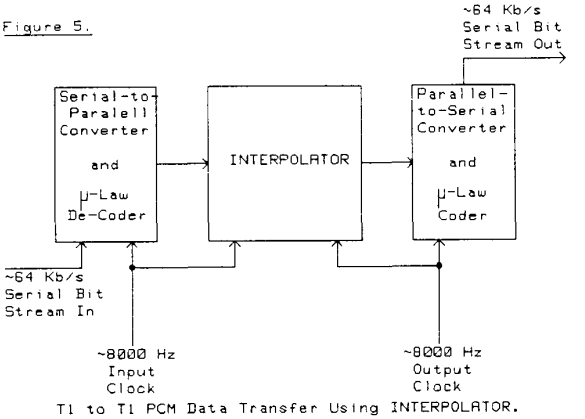
PCM-PCM Interface.

Figure 5 shows a method of converting PCM (Pulse Code Modulation) data samples from one T1 carrier system to data samples for another T1 carrier system, each operating under independent "8000 Hz" clocks (see [2]).

PCM-"Analog" Modem Interface.

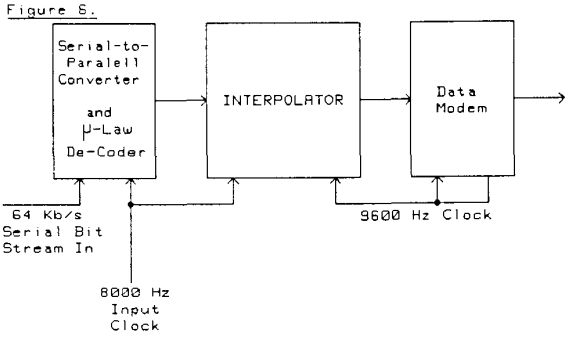
Figure 6 show a way of converting T1 carrier PCM samples at 8000 Hz directly to samples at 9600 Hz into the front end of an "analog" modem, thus obviating the need for an ADC or a DAC.

Figure 5.



T1 to T1 PCM Data Transfer Using INTERPOLATOR.

Figure 6.



T1 to Data Modem Using INTERPOLATOR.

3. IMPLEMENTATION.

If we make each of the tap coefficients of the system of Figure 1 an nth order polynomial in α, then we can re-arrange the structure to have n+1 FIRs with fixed coefficients, and the delayed output is a polynomial in delay whose coefficients are the outputs of each FIR. This structure is represented in Figure 7.

4. COEFFICIENT COMPUTATION.

The transfer function of a filter with a flat delay τ is given by:

$$G(\omega,\tau) = e^{j\omega\tau} \tag{1}$$

and the transfer function of an FIR with coefficients $\cdots C_k \cdots$ and sampling interval T is:

$$G(\omega) = \sum_n C_n \cdot e^{jn\omega T} \tag{2}$$

using a delay parameter α such that $\tau = \alpha T$ and tap coefficients which are a polynomials in α then:

$$G(\omega,\alpha) = \sum_n C_n(\alpha) \cdot e^{jn\omega T} = \sum_n \sum_m \alpha^m \cdot C_{n,m} \cdot e^{jn\omega T} \tag{3}$$

If we to want to determine the coefficients for a CVDD, we minimize:

$$\int_{\omega_0}^{\omega_1}\int_{\alpha_0}^{\alpha_1} \left|\sum_n\sum_m \alpha^m \cdot C_{n,m} \cdot e^{jn\omega T} - e^{j\omega(\alpha T)}\right|^2 d\alpha \cdot d\omega \qquad (4)$$

with respect to [**C**].

For a filter of length N the filter coefficients are numbered from $C_0(\alpha)$ to $C_{N-1}(\alpha)$. Using a CVDD of length N, where N is even, we subject (4) to the constraints:

$$\begin{aligned} C_n(\tfrac{1}{2}) &= 0; \quad n \neq (N-1)/2 \\ &= 1; \quad n = (N-1)/2 \end{aligned} \qquad (5)$$

$$\begin{aligned} C_n(-\tfrac{1}{2}) &= 0; \quad n \neq N/2 \\ &= 1; \quad n = N/2 \end{aligned}$$

With the above constraints and a delay of $\pm\frac{1}{2}$–tap about the center of the filter the sample just before or just after the center is transmitted exactly (with an even length filter, there is no center tap). This Delay element is not intended to serve any smoothing (or band limiting) function and no attempt is made to control its out-of-band response, as will be seen later.

5. COMPUTATIONAL APPLICATIONS.

Referring to Figure 7.

$$\begin{aligned} y_m &= \sum x_n \cdot c_{n,m} \\ z &= \sum \alpha^m \cdot y_m \end{aligned} \qquad (6)$$

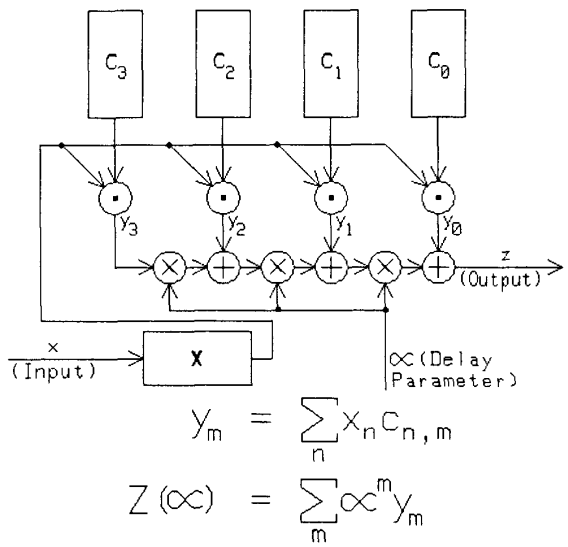


Figure 7. Structure of, 3rd Order, Continuously Variable Digital Delay.

from (6) we see that

$$\frac{dz}{d\alpha} = \sum m \cdot \alpha^{m-1} \cdot y_m$$

Having optimized [**C**] over one sample interval, we can find the derivative of the interpolated function of x at any point in the range $-\frac{1}{2} \leq \alpha \leq \frac{1}{2}$. Indeed we can make a good polynomial approximation of the interpolated function of x over the above range.

6. PERFORMANCE.

A laboratory model of the CVDD used as an interpolator has been implemented on a WE® DSP20. In this set-up, the line signal was sampled into an ADC at a constant clock rate, asynchronously with the transmitter clock. These samples were then fed into an interpolator using the CVDD and interpolated by the receiver clock, into a V.32 receiver. The receiver clock was derived by the receiver "timing recovery" from the interpolated samples. Tests run over this system using a V.32 signal showed no significant degradation in performance. What was used was an 8-Tap, 3rd-Order CVDD; the tap coefficients are given in Table I.

TABLE I. -- C(N,M)

	M			
	0	1	2	3
0	-.013824	.003143	.055298	-.012573
1	.054062	-.019287	-.216248	.077148
2	-.157959	.1008	.631836	-.403198
3	.616394	-1.226364	-.465576	.905457
4	.616394	1.226364	-.465576	-.905457
5	-.157959	-.1008	.631836	.403198
6	.054062	.019287	-.216248	-.077148
7	-.013824	-.003143	.055298	.012573

Coefficients, C(N,M), for 8-Tap, 3rd Order, Ditial Variable Delay with Tap Spacing 1/9600 secs. and Upper Useful Frequency of 3150 Hz.

This CVDD was designed to operate over a frequency band from 0 to 3150 Hz. Figures 8 and 9 are plots of Delay and Amplitude error over this frequency range for $-\frac{1}{2} \leq \alpha \leq \frac{1}{2}$. These figures show relatively level plateaus for the range of interest. As was stated in section 5. no attempt has been made to constrain the out-of-band response. The CVDD is a linear FIR, for any given setting of α, and if the timing drift between transmitter and receiver is very small, i.e $d\alpha/dt$ is very small, then a receiver using an adaptive equalizer will have no trouble tracking any slight variations of delay or amplitude introduced by the CVDD.

Figure 10. shows the behavior of $C_n(\alpha)$ as a function of α. It can be seen that, as a consequence of the constraints (5) that $C_4(-\frac{1}{2}) = 1$ and and $C_3(\frac{1}{2}) = 1$. A further consequence of (5) is that:

$$\begin{aligned} C_{n,0} + (\tfrac{1}{2})\cdot C_{n,1} + (\tfrac{1}{2})^2 \cdot C_{n,2} + (\tfrac{1}{2})^3 \cdot C_{n,3} \ldots &= 0 \\ C_{n,0} + (-\tfrac{1}{2})\cdot C_{n,1} + (-\tfrac{1}{2})^2 \cdot C_{n,2} + (-\tfrac{1}{2})^3 \cdot C_{n,3} \ldots &= 0 \end{aligned}$$

this agrees with the fact that the numbers in column 2

of Table I are -4 times the numbers in column 0, and the numbers in column 3 are -4 times the numbers in column 1: except for rows 3 and 4. This suggests that this CVDD can be implemented with only 2 instead of 4 FIRs, thus reducing the amount of computation. In fact for any polynomial of degree "N" the CVDD can be implemented with N-1 FIRs. This type of CVDD has three parameters:

1. Upper Useful Frequency.
2. Number of Taps (Nt).

and 3. Degree of Polynomial (Dp).

Figures 11. and 12. are plots of the upper useful frequency for -40 dB and -60 dB rms error for CVDDs of various numbers of taps and degrees of polynomial. Thus it is possible to select Dp and Nt to meet the requirements for any particular CVDD.

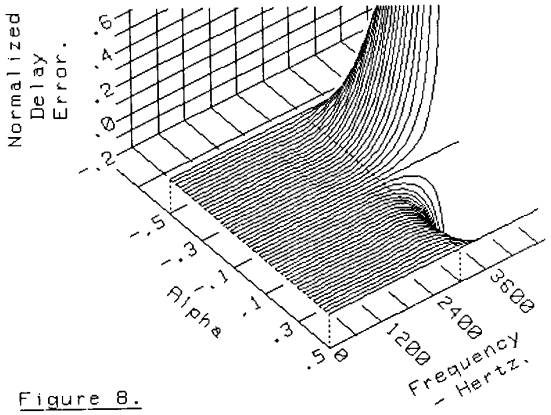


Figure 8.

Plot of Normalized Delay Error vs. Delay (Alpha) and Frequency for the Digital Variable Delay with coefficients given in table I.

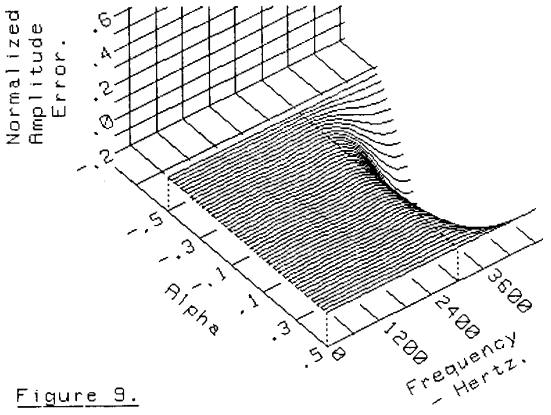
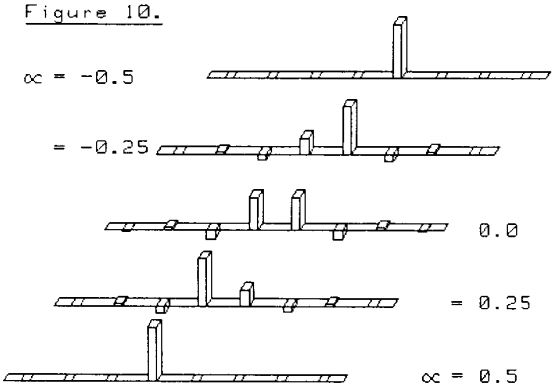


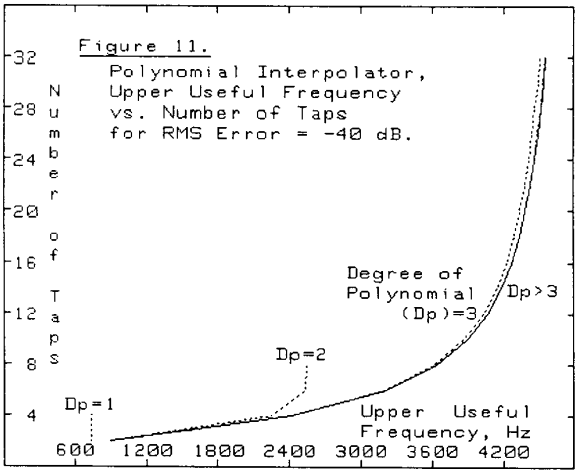
Figure 9.

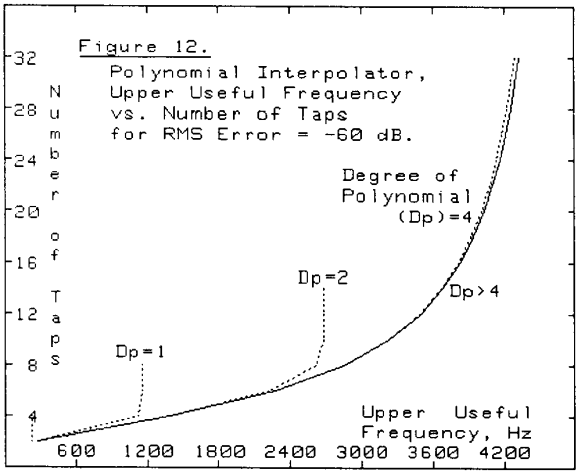
Plot of Normalized Amplitude Error vs. Delay Setting (Alpha) and Frequency for the Digital Variable Delay with coefficients given in table I.

Figure 10.



Plot of Tap Coefficients (C(Alpha,N)) for various values of Alpha for the Digital Variable Delay with the Coefficients given in table I.





The plots of Figures 8,9,11 and 12 were all made for a sampling rate of 9600 samples/second.

7. FEATURES.

What has been described is a Continuously Variable Digital Delay Element which can be used to generate a delayed version of a sampled signal from the samples.

The CVDD can be incorporated in Digital Signal Processing applications as interpolator for applications such as modems with Echo Cancellers, transfer of PCM data from one clocked system to another, or a more general computational element for generating functions, i.e. the derivative, of the sampled signal.

When a band-limited signal is sampled at the Nyquist rate it is theoretically possible to reconstruct the original signal from the samples. One might ask the question "how?". The Continuously Variable Digital Delay described here gives an answer: at least for a limited length CVDD, we can come up with a very good approximation.

8. COMPARISON.

In this approach to interpolation, an interpolated sample is generated only as needed. Other approaches [2] generate a continuum of closely spaced samples and select the desired outputs from them. Thus, the amount of computation required here is much less than other approaches. Also, because "Delay" is a parameter in the computation, the resolution of the delay is limited only by the precision of the arithmetic, not by the computation rate.

9. EXTENSIONS.

It should be apparent that, within reason, we can generate filters with arbitrary transfer functions of the form $G(\omega,x)$. One such application might be to control the formant in music applications. Extending the same concept to more dimensions we could simultaneously control the delay and amplitude distortions in a transmission line simulator.

REFERENCES

[1] Jean-Jacques Werner, "An Echo-Cancellation-Based 4800 Bit/s Full-Duplex DDD Modem", IEEE Journal on Selected Areas in Communication, Vol SAC-2, No 5, September 1984.

[2] J. C. Candy and O. J. Benjamin, "A Circuit That Changes the Word Rate of Pulse Code Modulated Signals", The Bell System Technical Journal, Vol. 62, No. 4, April 1983, pp 1161-1168.

APPENDIX

Figure A1 shows two different representations of the same FIR (Finite Impulse Response Filter). Figure A1 is included here to explation the symbology used in the rest of the paper.

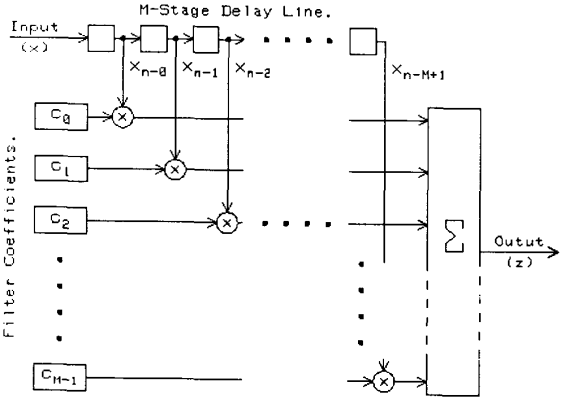


Figure A1.