Development of a Digital Optical Instrument Transformer with Process Bus Interface According to IEC 61850-9-2 Standard

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***Abstract*— This article presents a prototype development of a digital optical Instrument Transformer with IEC 61850-9-2 interface. We present the main topics related to the implementation of a process bus according with IEC 61850-9 standard and a block diagram of Instrument Transformer prototype proposed. Some results from mathematical simulations and prototype testing are presented at the end of this article.**

***Index Terms*—IEC 61850-9, instrument transformers, power system measurements, power system protection.**

I. Introduction

The IEC 61850 standard [1] defines requirements for implementing a real-time process bus enabling the Instrument Transformers (ITs), present at process level, to sample voltages and currents from a power system and to transmit these sampled values via process bus.

Moreover, the optical technology is an interesting way for the development of electronic ITs for voltage classes higher than 69 KV, presenting the following advantages:

- no saturation (ITs for current measurement);
- low size;
- low weight;
- high security due to electrical insulation;
- better response against electromagnetic interferences;

The possibility of joining the advantages of these two technologies with the development of an innovative IT is the main goal of this work. This article presents a summary of the main requirements of the IEC61850-9 standard to be met by an IT with process bus interface and the development of a digital optical IT prototype for measuring the high voltage of a power system that meets these requirements. Initial results are presented at the end of the article.

II. IEC 61850 Requirements for ITs with Process Bus Interface

According to [2] [3], the main requirements to be met by Intelligent Electronic Devices (IEDs) connected to a process bus may be subdivided into five categories: variations of the IEC 61850-9 standard, process bus reliability, time synchronism, cyber security and measurement accuracy analysis. Based on these studies, an IT with IEC 61850-9 interface must meet the following recommendations:

- *variations of the standard*: the IT must meet the IEC 61850-9-2 standard requirements; the IEC 61850-9-1 standard should be discontinued in the future;
- *process bus reliability*: the IT must implement redundancy features in its network interface with zero recovery time; the most promising solutions are defined by the IEC 62439-3 standard (HSR protocol for low-cost solutions, and PRP protocol to other solutions);
- *time synchronism*: the IT must be able to synchronize its internal clock via network using the PTP protocol defined by the IEEE 1588v2 standard; 1pps format can also be accepted, to be compatible with the devices already installed;
- *cyber security*: physical protection methodologies must be applied to improve network security; implementation of signature-based methodologies, as defined in IEC 62351 standard, should be implemented in the future due to the latency of current IEDs processors;
- *measurement accuracy analysis*: the IEC 61869 standard, currently in its final stage of elaboration, will replace the IEC 60044 standard. This new standard will provide several updates, establishing new requirements to be met by electronic ITs (e.g. harmonic response, time delay, anti-aliasing filter characteristics, etc.); this information is of great importance for ITs developers, and for defining test requirements for electronic ITs with IEC 61850-9 interface.

III. Optical IT with IEC 61850-9 Interface

Based on the chapter II recommendations, the next step was to develop a simplified block diagram of the digital optical IT prototype, as shown in Fig. 1.

Fig. 1. Block diagram of the digital optical IT with process bus interface

The IT design is based on researches performed in [4] [5] to develop an Optical Digital Voltage Transformer prototype with process bus interface according to the IEC 61850-9 standard. First, the high voltage is applied to the *interferometer high voltage sensor*, as shown in Fig. 2.

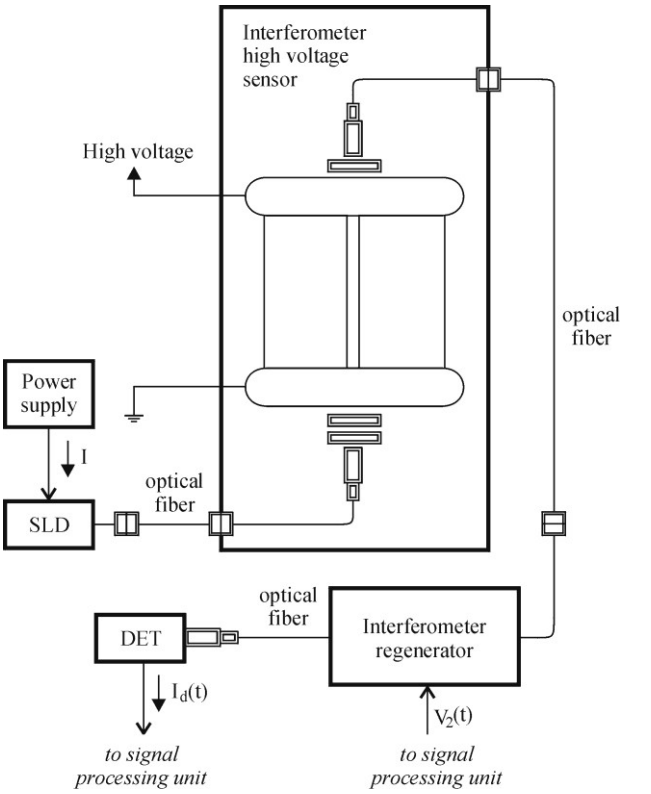

Fig. 2. Block diagram of electro-optical unit

It consists of a Pockels sensor, based on White Light Interferometer (WLI), which modulates the optical signal emitted by a Super Luminescent Diode (*SLD* block) according to the high voltage waveform applied. In the next step, the optical signal has its optical path difference compensated by a second interferometer (*interferometer regenerator* block), and thereafter, it is detected by a photo-detector (*DET* block) and sent to the *signal processing unit* block, as shown in Fig. 3.

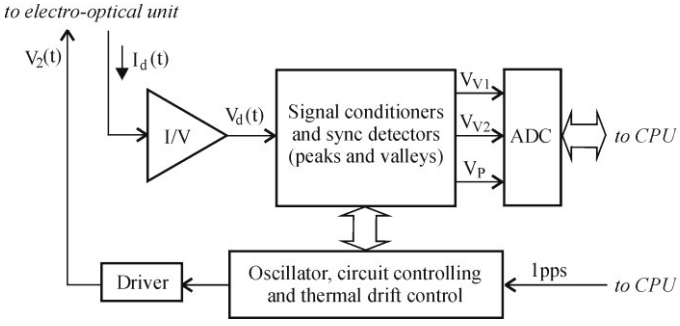

Fig. 3. Block diagram of signal processing unit

According to [4] [5], signal *Id(t)* can be expressed by:

$$I_d(t) = I_{d0}\left\{1 + \frac{1}{2}\cos[\phi_1 \text{sen}\ \omega_1(t) + \phi_2 \text{sen}\ \omega_2 t]\right\} \quad (1)$$

$Ø_1$ e $Ø_2$ are the optical phase delays electrically introduced by the *interferometer high voltage sensor* and *regenerator interferometer*, respectively. Fig. 4 shows an example of signal *Id(t)* modulated by a high sinusoidal voltage applied on the *interferometer high voltage sensor*, considering $\omega_2 = 16\omega_1$, $Ø_1 = 0{,}5$ and $Ø_2 = \pi/2$, where $\omega_1 = 2\pi f_1$, f_1 is the high voltage frequency applied to sensor and $T_1 = 1/f_1$ its period. Similarly, $\omega_2 = 2\pi f_2$ and $T_2 = 1/f_2$.

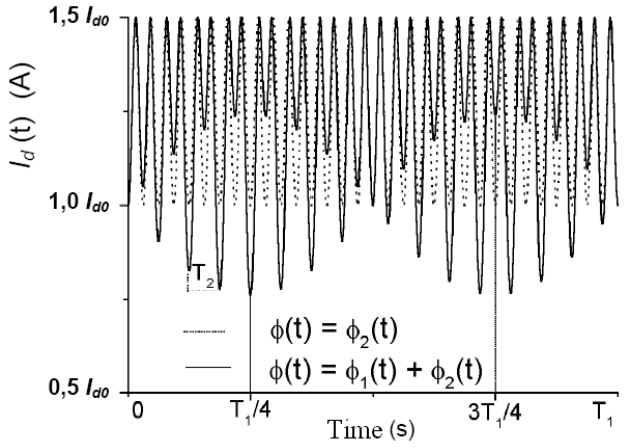

Fig. 4. Id(t) signal example

Signal *Id(t)* is applied into the transimpedance amplifier *I/V*, which converts the current signal *Id(t)* into a corresponding voltage signal *Vd(t)*. Following the conditions imposed in [4] [5], signal *Vd(t)* can be discretized into samples through an analysis of a set of valley values (V_{V1} and V_{V2}) and peak value (V_P) of signal *Vd(t)*, as shown in Fig. 5.

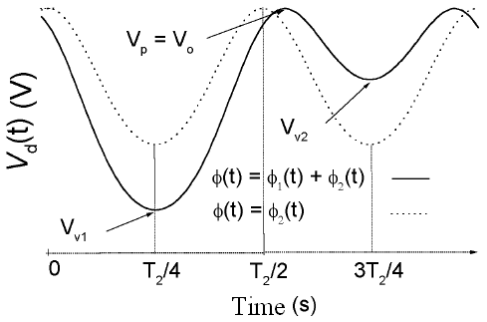

Fig. 5. Expansion, in time domain, with transimpedance amplifier output signal between 0 and T_2.

In this situation, the value of one high voltage sample may be obtained through the expression:

$$\phi_1(t)\big|_{\phi_2 = \pi/2} = \text{arcsen}\left(\frac{V_{V2} - V_{V1}}{V_O}\right) \quad (2)$$

Following the block diagram of Fig. 3, *oscillator, circuit controlling and thermal drift control* block has a thermally stable oscillator, responsible for generating the electrical

signal $V_2(t)$, which is applied to the *electro-optical unit* block. This block also sends control signals to sample-and-holder circuits of the *signal conditioners and sync detectors* block, so that they can sample synchronous voltages V_{V1}, V_{V2} and V_P. Before being applied to the sample-and-holder circuits, high frequencies components of signal *Vd(t)* are eliminated by anti-aliasing filters inside the *signal conditioners and sync detectors* block. Then, voltages V_{V1}, V_{V2} and V_P are digitized by analog-to-digital converters inside the *ADC* block in order to be read by the *CPU* block, as shown in Fig. 6.

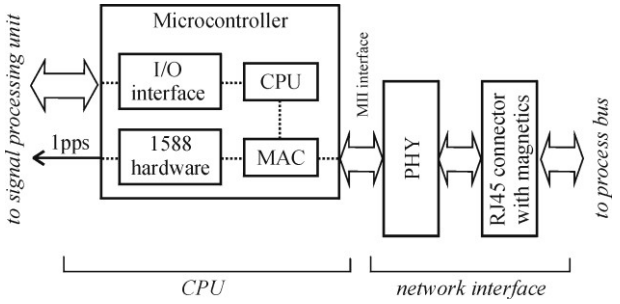

Fig. 6. Block diagram of CPU and network interface

In *CPU* block, high voltage signal samples, time synchronism and construction of network message are processed. This message is sent via process bus through *network interface* block. The IEC 61850-9-2 standard defines that a high voltage signal must be sampled, digitized and transmitted via process bus through specific messages called Sample Value Messages (*SV Messages*). These samples are performed in a synchronous way according to a time base defined, or by the IEEE 1588v2 standard, or by 1pps format (for legacy devices), as shown in Fig. 7, below.

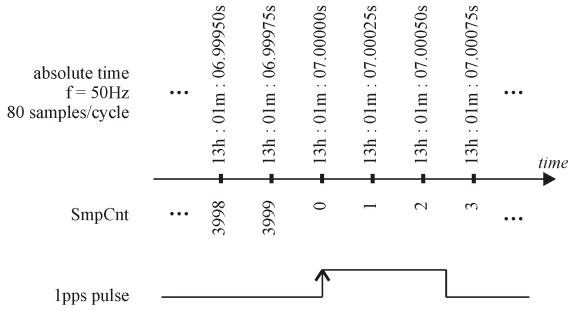

Fig. 7. SV Message timestamp example considering 50Hz for power system frequency, 1pps sync and 80 samples/cycle

The representation of the moment when the samples are made is performed by a sample counter (*SmpCnt*), whose value is incremented at each sample and inserted into the *SV Message*. This counter returns to zero at every transition of a new second. The IEC 61850-9-2 standard defines two sample rates: 80 samples/cycle (for protection purposes) and 256 samples/cycle (for measurement purposes). The IEC 61850-5 standard defines three performance classes applied to time synchronism of ITs, according to Tab. 1.

TABLE I
Time performance classes for ITs

Time performance class	Accuracy (µs)	Reference	
T3	± 25	P1	
T4	± 4	P2	M1
T5	± 1	P3	M2/3

According to the IEEE 1588v2 standard, there are three possible points to perform the measurement of sync messages timestamps, as shown in Fig. 8. Implementations performed [6] point out that the accuracy achieved by timestamp measurement at *point A* is better than 10ns; at *point B,* it is between 10ns ~ 10µs; and at *point C,* it is worse than 10us. Therefore, a microcontroller with internal IEEE1588 hardware located at *point B* will be used, which should be sufficient to at least meet the *T3 class* requirements.

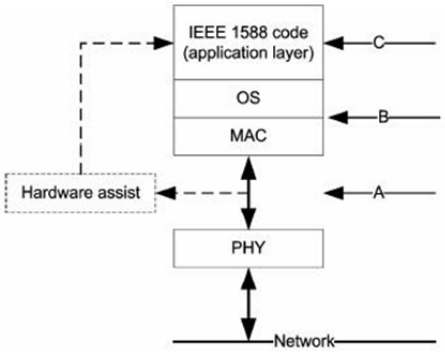

Fig. 8. Timestamp measuring points according to IEEE 1588v2

Since the sampling process of the high voltage signal begins at the instant the sample-and-holder circuits (inside the *signal processing unit*) perform their samples, and these samples are triggered synchronously by a high precision oscillator, it is necessary to synchronize the entire process according to the time base defined. Because the high precision oscillator allows resynchronization via an external 1pps pulse, and the microcontroller internally has an IEEE1588 hardware with dedicated 1pps output, the 1pps pulse will be used to resynchronize the high precision oscillator. The initial sampling rate proposed is 256 samples/cycle. Based on (1) and (2), it can be concluded that the precision oscillator must be set at the same frequency as the sampling, therefore, 12800Hz (for a 50Hz power system frequency).

IV. Initial Results

Papers [4] [5] developed initial prototypes of an *electro-optical unit* and *signal processing unit*. Fig. 9 presents a prototype image of the *interferometer regenerator* used in the *electro-optical unit* block.

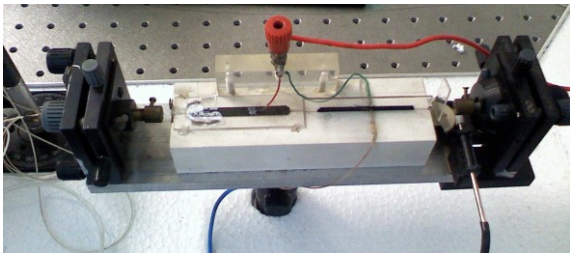

Fig. 9. Interferometer regenerator prototype

Using *Matlab*, some mathematical simulations were performed, in order to estimate the error introduced during the calculation of the samples of the high voltage applied. According to (2), each sample is calculated by analyzing a set of valley (V_{V1} and V_{V2}) and peak (V_P) values. Ideally, each sample would be generated without error in a situation in which the high voltage measured did not change in the time interval between two valleys. For an oscillation frequency of 12800Hz, the time interval is about 78.1μs. In practice, for a high voltage signal of 50Hz frequency, this does not occur, which causes an error. To compensate it, two hypotheses were formulated. From the application of a high voltage reference signal for IT calibration:

a) The sample value calculated is assumed not to have any magnitude error, but it was sampled at a given time with an error of ±Δt, if compared with the correct time instant; therefore, it is possible to correct this sample by adjusting its sampling time;
b) The sample value is assumed to have been sampled at a given time, without any timing error, but it has magnitude error; therefore, it is possible to correct this sample by adjusting a gain *G*.

For the simulations, (b) was adopted to prioritize a better time control of samples, taking into consideration the high timing requirements shown in Tab. 1. The sampling time adopted was $T_2/2$, according to Fig. 5. Signal *Vd(t)* adopted agrees with the example in Fig. 5. The results show that each sample error is not constant, and the distribution of errors depends on the gain value. In order to better adjust the gain, which minimizes the magnitude errors of samples, the Least Squares Method was used. The sum of quadratic errors, accumulated by 256 samples generated from a 50 Hz period of high voltage signal, may be expressed as:

$$S = \sum_{i=1}^{256} \left(y_i - G\, x_i \right)^2 \qquad (3)$$

where *S* is the sum of errors, y_i is the high voltage signal measured, x_i is the signal sampled by (2) and *G* is the adjusted gain. For several *G* values, the following *S* values were obtained, as shown in Fig. 10.

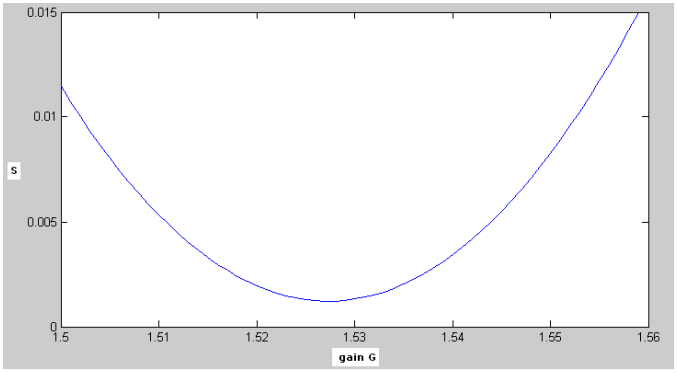

Fig. 10. Accumulated errors according to gain G adjusted

The better gain adjust occurs when:

$$\frac{dS}{dG} = \sum_{i=1}^{256} 2 \left(y_i - G\, x_i \right) \left(- x_i \right) = 0 \qquad (4)$$

which resulted in a *G* value of 1.528, approximately.

According to the IEC 61869-9 standard, which is in its final stage of elaboration, the amplitude and phase displacement errors are represented by a phasor $\varepsilon_{(s)}$ [7]. This phasor is calculated using a full cycle Discrete Fourier Transform on the difference between its samples and those of a reference instrument transformer, divided by the RMS value of the reference signal, as shown in (5).

$$\vec{\varepsilon}_{(s)} = \frac{\frac{\sqrt{2}}{N} \sum_{n=0}^{N-1} \left(i_{X(s-n)} - i_{R(s-n)} \right) e^{2\pi \sqrt{-1}\, k (s-n)/N}}{\sqrt{\frac{1}{N} \sum_{n=0}^{N-1} \left[\left(i_{R(s-n)} \right)^2 \right]}} \cdot 100\% \qquad (5)$$

For gain *G* calculated, both errors were close to zero.

V. Conclusions

This article presented a prototype of a digital optical IT for high voltage metering with IEC 61850-9-2 interface. The Pockels sensors, based on LWI, applied for measuring high voltage from power system showed to be promising. Initial prototypes of an *electro-optical unit* block and a *signal processing unit* block have been developed and presented satisfactory results. The calculation process used to obtain the samples values was improved using the Least Squares Method, reducing errors due to the measurement of high voltage sinusoidal signals. Future studies will be conducted in order to implement redundancy of communication channel and signature of *SV Messages* sent via process bus.

VI. References

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VII. BIOGRAPHIES

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