

# A Fast-Switching Current-Pulse Driver for LED Dimming Control Circuits

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**Abstract**— In this paper, a fast-switching current-pulse driver for dimming controllers of light-emitting diode (LED) backlight applications is proposed. A pair of current switches, which is used for driving the LED string, employs an adaptive bias circuit for low-power dissipation. A differential pre-amp drives the large-size current switches to achieve fast current switching. The proposed current-pulse driver was fabricated in TSMC 0.25- $\mu\text{m}$  1P4M BCD high-voltage process. The measured rising time and falling time of the LED current are 120 ns and 12 ns, respectively, when the load is a 10-LED string.

## I. INTRODUCTION

Nowadays, more and more kinds of flat-panel displays, such as liquid crystal displays (LCDs) and organic light-emitting diodes (OLEDs), have been utilized in information and communication technology (ICT). Besides, light-emitting diodes (LEDs) are widely used for LCD backlighting since they have longer lifetime, lower power consumption, wider brightness range, and better dimming capability. Fig. 1 shows the architecture of an LED backlight driver, consisting of a DC-DC converter and a current-mode dimming control circuit. The DC-DC converter provides a DC voltage  $V_{CC}$  to the parallel LED strings to ensure that every LED can be turned on. The current-mode dimming control circuit controls the current flow through each LED string to adjust the LED light brightness. Analog type and pulse width modulation (PWM) type are two common ways of dimming control for LED backlights [1]. Because of the color shift issue in the analog dimming control, the PWM control mode is generally used in LED backlight design. In order to achieve accurate brightness, a fast-switching current-pulse driver is required in the current-mode dimming control circuit [2-3].

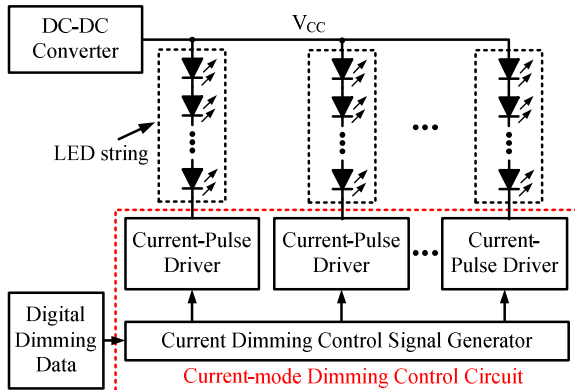


Fig. 1. LED backlight driver with the proposed current-pulse driver.

## II. PROPOSED ARCHITECTURE

Fig. 2 shows the architecture of the proposed fast-switching current-pulse driver, which consists of an adaptive bias circuit, a pre-amp, and a pair of current switches (M1-M2). M2 is a 40-V HV-NMOS device. In the adaptive bias circuit, M4 is a data-control current source, and M5 is a constant current source. When the data D is "0", switch 1 is turned off, and switch 2 is on.  $V_{DD}$  is applied to the inverting input of the open-loop op-amp, and the output of op-amp is reduced to a low level. This makes the current source transistor M4 off. Only a dc current of 5  $\mu\text{A}$  is applied to the differential pair. The digital signal D is also applied to the non-inverting terminal of the pre-amp. For digital signal D of "0", the pre-amp turns off M2, and it switches the constant current of 5  $\mu\text{A}$  to M1. The LEDs do not emit any light. The current switches consume only 5  $\mu\text{A}$  when the LEDs are not luminous. When the digital signal D changes to "1", the non-inverting input of the op-amp is isolated from  $V_{DD}$ , and the op-amp forms a closed loop as a unity-gain buffer. M3 and M4 form a current mirror. By setting the size ratio between M4 and M3 to be 1000, M4 supplies a current of 60 mA to the differential pair of the current switches. Simultaneously, the tail current of 60.005 mA is switched to the LED string by the pre-amp. The outputs of the pre-amp, which is constructed by a differential pair and two diode-connected transistors, are limited to several hundred millivolts to achieve high-speed current switching.

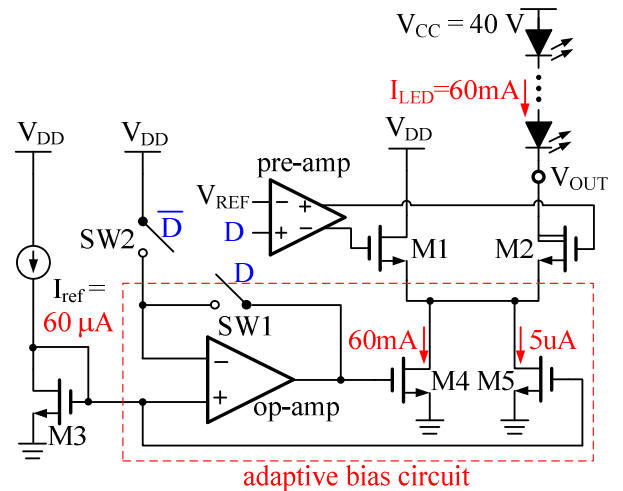


Fig. 2. Architecture of the proposed fast-switching current-pulse driver.

Because of the large aspect ratio of M4, a large parasitic capacitance exists at the gate of M4. However, the unity-gain buffer is used to drive M4 to achieve high-speed switching. Fig. 3 shows the schematic of the op-amp. When the data D is "0",  $V_{DD}$  is applied to the inverting input of the open-loop op-amp, M18 discharges the output, and the output voltage level is reduced. As the output voltage reduces below the NMOS threshold voltage, M19 turns off and it stops the output voltage reducing further. This voltage is low enough to turn off M4. Therefore, the current switches consume only 5  $\mu$ A when the digital signal is "0". When the signal D changes to "1", the op-amp forms a unity-gain buffer, and its output voltage increases from the NMOS threshold voltage to the gate-to-source voltage of M3. Only a small voltage increment is required at the gate of M4, and hence, a small time period is required for supplying the current of 60 mA. This also enhances the current switching.

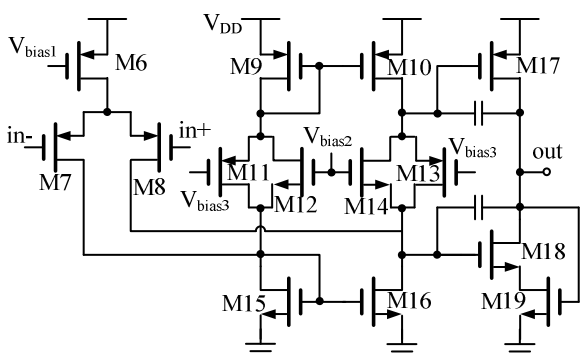


Fig. 3. Schematic of the op-amp.

### III. EXPERIMENTAL RESULTS

A 7-channel prototype was manufactured by using TSMC 0.25- $\mu$ m 1P4M BCD 2.5V/40V process to validate the performance of the proposed current-pulse driver for LED backlight applications. Fig. 4 shows the chip photograph of the 7-channel current-pulse driver with the chip size of  $0.69 \times 1.9$  mm<sup>2</sup>. Fig. 5 shows the measured input PWM signal with 50KHz and 50% duty cycle and output current waveform of a 10-LED string. The rising time and falling time are 120 ns and 12 ns, respectively, when the amplitude of LED current is 60mA. Table I shows the performance summary.

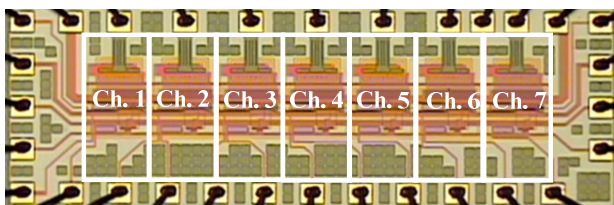


Fig. 4. Chip photograph of a 7-channel fast-switching current-pulse driver.

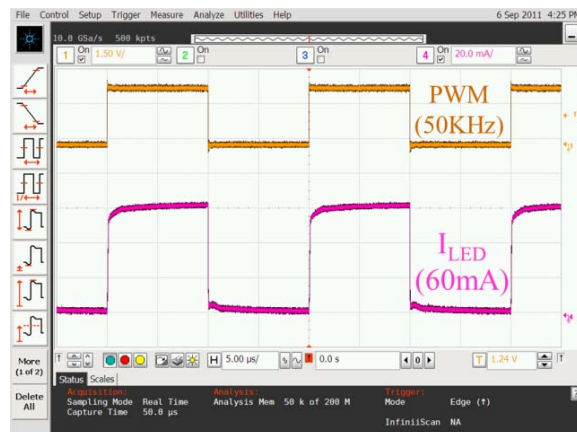


Fig. 5. Measured input PWM signal with 50% duty cycle and current waveform of an LED string.

### IV. CONCLUSION

This work presents a prototype of a 7-channel fast-switching current-pulse driver. The measured rising time and falling time of the LED current are only 120 ns and 12 ns. The measured results verify that the proposed current-pulse driver is suitable for LED backlight applications.

TABLE I  
PERFORMANCE SUMMARY

	This work	[2]
Process	2.5V/40V 0.25 $\mu$ m BCD Process	5V/40V 0.5 $\mu$ m BCD Process
$V_{DD}$	2.5 V	5 V
$V_{CC}$	40 V	40 V
$V_{OUT}$	3~40 V	2~40 V
$I_{LED}$	60 mA	80 mA
Channels (#)	7	8
Rising time	120 ns	360 ns*
Falling time	12 ns	5 ns*
DC current consumption	168 $\mu$ A/channel	1020 $\mu$ A/channel
Chip area	0.69 x 1.9 mm <sup>2</sup>	1.9 x 3.2 mm <sup>2</sup>

\*Simulation results.

### ACKNOWLEDGMENT

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### REFERENCES

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