An Energy Harvester Circuit with Clock Booster for Piezoelectric Energy Harvesting

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Abstract—**This paper presents an energy harvester circuit in a 0.18-μm CMOS process. The clock booster is employed to increase the amplitudes of the pulses and easily turn on the buck-boost converter. The proposed technique provides a stable power supply without using a low dropout regulator. The simulation results show the output voltage about 841 mV with the input frequency of 100 kHz, the peak-to-peak voltage of 1.6 V, a load capacitance of 10 nF, and a load resistance of 10 GΩ, respectively. Fully powered by a vibration piezoelectric energy harvester (PEH), the proposed circuit consumes an average power of 114 μW.**

Keywords—Energy harvester circuit; clock booster.

I. INTRODUCTION

In recent years, energy harvesting has become a popular technique because of the environmental awareness. For applications in the severe environments, such as the island, the mountaintop, the wildness or even in the human body, which is difficult to replace the batteries. Compared with conventional battery-powered systems, we tend to use the self-powered system in the devices. As a result, some portable electronics or wearable and implantable devices has added the energy harvesting circuits inside.

Instead of other energy harvesting components, piezoelectric energy harvesters (PEHs) are common used owing to its high power density, high scalability, and high output voltage generation [1]. The power management module is fabricated using a full bridge rectifier, a relaxation oscillator, a non-overlapping clock, a clock booster and a buck-boost converter.

This paper is organized as follows. The circuit descriptions is presented in Section II. The experimental results are presented in Section III, and Section IV concludes the paper.

II. CIRCUIT DESCRIPTION

Fig. 1 shows the block diagram of the proposed piezoelectric energy harvester (PEH) power conditioning circuit. The power conditioning circuit consists of a rectifier, a relaxation oscillator, a non-overlapping clock, a clock booster and a buck-boost converter [2], [3]. The rectifier converts the incoming AC signal, and the relaxation oscillator outputs a clock signal to the clock boosting circuit to make sure the timing signals can drive the buck-boost converter. Fig. 2 shows the schematic of the energy harvester circuit.

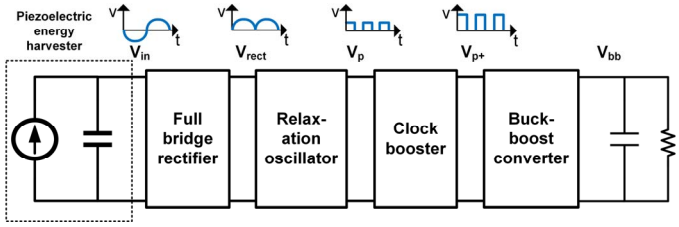

Fig. 1. Block diagram of the piezoelectric energy harvester.

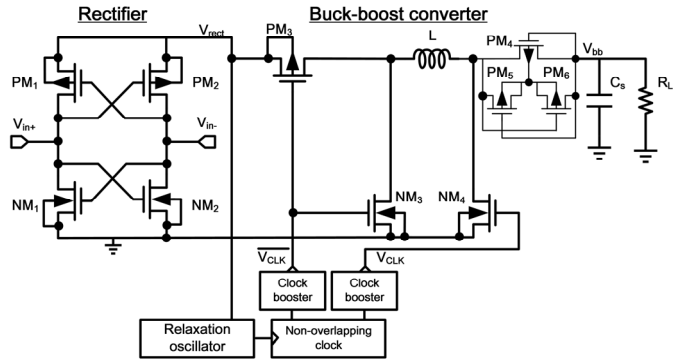

Fig. 2. The energy harvester circuits.

A. Full Bridge Rectifiers

The rectifier reduces the forward voltage drop to $2V_{ds}$ with a cross-coupled switching transistor architecture. PM_1 and NM_2 turn on during the positive half cycle. In the opposite, PM_2 and NM_1 turn on during the negative half cycle. The output V_{rect} is connected to the next stage for further processing.

B. The Relaxation Oscillator and Non-overlapping Clock

Fig. 3 shows the circuit of a relaxation oscillator. It is improved by a conventional relaxation oscillator [3] and is composed of a start-up circuit, a current source, buffers, and a divide-by-2 divider. The capacitor C_S is charged by current I_S. While C_S has charged over half of the V_{REC}, V_1 goes low. Then, V_{PUL} becomes high after six buffers' delay time, which is equal to $6\tau_D$. Then, M_{S1} is turned on to discharge C_S, and V_{SAW} becomes low. After $6\tau_D$, V_{PUL} turns low again. M_{S1} is turned off and the I_S current charged to C_S, repeatedly. The pulse is divided by 2 in order to get 50% duty cycle clock signal and the clock frequency f_{CLK} is given as

$$f_{CLK} \approx \frac{0.5}{\frac{0.5V_{REC} \cdot C_S}{I_S} + 12\tau_D} \quad (1)$$

where I_S is the source current. The improved version can get the same achievement with lower power consumption. A non-overlapping clock generates the control signals to drive the power MOSFET switching without shoot-through current. The simulation results are shown in Fig. 4. The I_S and C_S are chosen as 138 nA and 1.4 pF, respectively, to realize f_{CLK} of 122 kHz, when V_{REC} = 0.8 V.

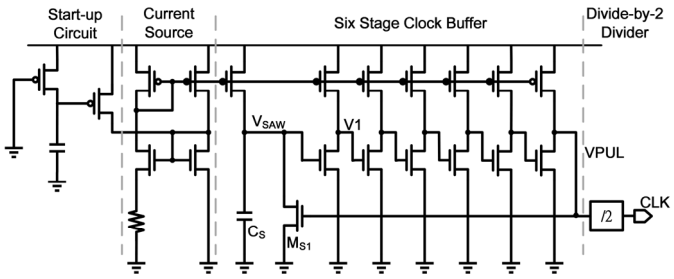

Fig. 3. Relaxation oscillator.

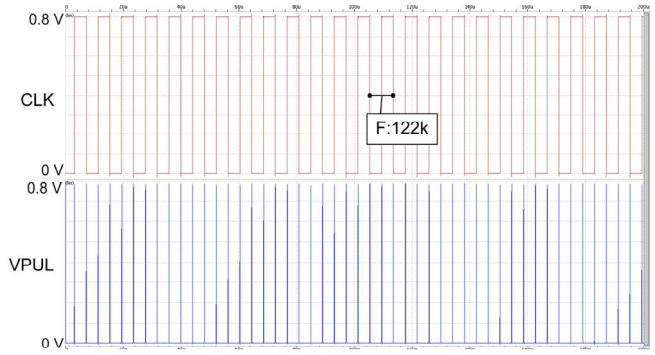

Fig. 4. The simulation results of relaxation oscillator.

C. *Clock Boosting Circuit and Buck-boost Converter*

A clock boosting circuit is shown in Fig. 5. When P_1 goes low, MB_1 will be turned on because of V_1 becomes low. Then, V_3 goes high and MB_2 will be turned off. At the same time, the capacitor C_B is charged to V_{REC} through MB_1, and V_2 becomes to V_{REC} finally. While P_1 goes high, V_1 will become V_{REC}, and therefore MB_1 will be turned off. Meanwhile, V_2 is boosted to $2V_{REC}$, and MB_2 is turned on due to V_3 goes low. As a result, the output P_{1+} has the amplitude of $2V_{REC}$. Two p-type dynamic body bias (PDBB) circuits are used to bias the body voltages for MB_1 and MB_2, in order to avoid the body leakage current. Fig. 6 shows the simulation waveforms. The output voltage P_{1+} is boosted to 1.2V, when V_{REC} = 0.8 V. The output voltage is smaller than $2V_{REC}$ may be caused by the loss during the switching of MB_1 and MB_2.

The buck-boost converter is controlled by the clock signal of clock boosting circuit. A discontinuous conduction mode (DCM) buck-boost converter is composed of only three MOS switches, rather than four MOS switches [4]. For the purpose of blocking the reverse current during DCM operation, a passive diode connected with the MOS device is added.

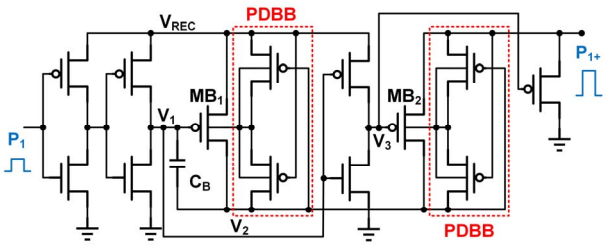

Fig. 5. Clock boosting circuit.

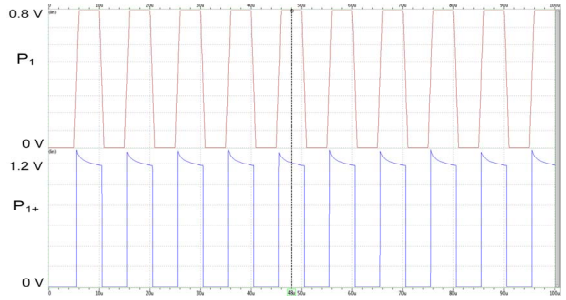

Fig. 6. Simulation results of clock boosting circuit.

III. EXPERIMENTAL RESULTS

The energy harvester circuit with clock booster was fabricated in 0.18-μm CMOS technology. Fig. 7 shows the simulation results of an energy harvester circuit. The simulation results have the output voltage about 841 mV with the input frequency of 100 kHz, the peak-to-peak voltage of 1.6 V, a load capacitance of 10 nF and a load resistance of 10 GΩ, respectively.

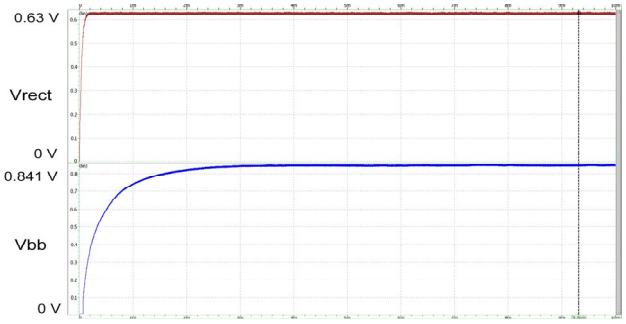

Fig. 7. Simulation results of the energy harvester circuit.

IV. REFERENCES

[1] Sanchez, D. A., et al., "A parallel-SSHI rectifier for piezoelectric energy harvesting of periodic and shock excitations," *IEEE J. Solid-State Circuits*, vol. 51, no. 12, pp. 2867-2879, Dec. 2016.

[2] Zhu, Y., et al., "An energy autonomous 400 MHz active wireless SAW temperature sensor powered by vibration energy harvesting," *IEEE Trans. Circuits and Systems I: Regular Papers*, vol. 62, no. 4, pp. 976-985, Apr. 2015.

[3] Luo, Y. S. and S. I. Liu, "A voltage multiplier with adaptive threshold voltage compensation," *IEEE J. Solid-State Circuits*, vol. 52, no. 8, pp. 2208-2214, Aug. 2017.

[4] B. Sahu and G. A. Rincon-Mora, "A low voltage, dynamic, noninverting, synchronous buck-boost converter for portable applications," *IEEE Trans. Power Electronics* vol. 19, no. 2, pp. 443-452, Feb. 2004.