# Over Temperature Protection Circuits for Integrated Power Converters

Deng Fong Lu and Chin Hsia
National Central University
*chinhsiancu2014@gmail.com*

***Abstract*—Integrated power converters suffer from overheating when they operate under extreme conditions. To prevent destructive breakdown an over-temperature protection (OTP) circuit is usually designed along with circuits, which restricts the chip temperature within a threshold level. From a design standpoint, OTP output should vary within a limit range throughout the whole process corners in order to support the chip's reliability. The paper presents an OTP circuit design to limit fluctuations in triggering and reset points by reducing the comparator errors. Simulated results revealed the designed OTP circuit can reach less than 10 % variation over 300 different corners.**

## I. INTRODUCTION

Over-temperature protection is an important function block in the integrated circuit, especially for power converters. Over-heating of a power converter may cause destructive breakdown when thermal instability of the device occurs. Moreover, over-heating reduces the product lifetime, due to the acceleration of failure mechanisms, and furthermore, over-heating is uncomfortable to the users [1,2].When the chip temperature exceeds a predetermined value, the comparator inside the OTP should be triggered to either power down or restart the circuit to avoid any possible damage [3-7]. In this paper, we present an improved version of protection circuit based on the reduction of comparator errors inside the OTP circuits. Two integrated temperature detectors was designed in comparisons and verify in full-corner simulations.

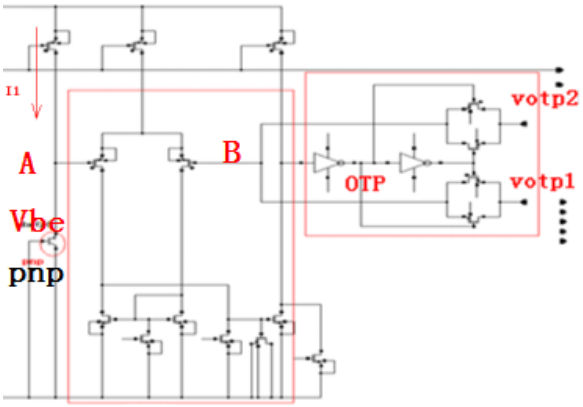


Fig. 1 A typical over temperature protection circuit schematic

The author would like to thank the Ministry of Science and Technology, Taiwan, R.O.C. for the project funding support under project number 106-2221-E-008 -061 -.

## II. OTP CIRCUIT DESIGN

To implement over-temperature protection requires a voltage measurement over temperature variations. A typical OTP circuit is shown in Fig. 1. A two-stage open-loop common-source amplifier, functioned as a comparator, was employed to drive two sets of transmission gates. By setting VA ≧ VB in the non-protection state, OTP is low, and VB is equal to Votp1. Vbe gradually decreases as the temperature rises. When VA ≤ VB, the OTP point is flipped to open the transmission gate such that VB is equal to Votp2. When the temperature drops from high to low, and hence the VA voltage below Votp2, the temperature protection is released. I1 can be generated from a band-gap reference and considered a relatively constant value. The PNP current, Ic, can be derived as follows,

$$Ic = I1 = Is*\exp (Vbe / (K0*T/q) \quad (1)$$

, where Is is the saturation current of bipolar transistors, and Vbe is the base-emitter junction voltage, K0 is the Boltzmann constant, and q is the charge of electrons. (1) can re-ordered to be equal to (2) as follows,

$$Vbe = (K0 * T / q) *\ln (I1 / Is). \quad (2)$$

and therefore, the designed OTP triggering and reset points, Ttriggering and Treset, are derived accordingly to be

$$Ttriggering = Vopt1/(K0/q*\ln(I1/Is)) \quad (3)$$

$$Treset = Vopt2/(K0/q*\ln(I1/Is)) \quad (4)$$

Figure 2 shows the simulated OTP triggering and reset points over 300 different corners. The dispersion over 60 degree Celsius was obtained due to the fact that the values of Vopt2 and Vopt1 fluctuate with corners. In addition, the overlapped points between triggering and reset points may cause OPT malfunctions in the circuits.

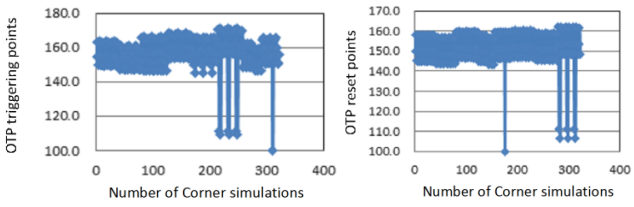


Fig. 2(a) Full-corner simulated OTP triggering points and (b) reset points (unit in Celsius)

## III. PROPOSED OTP CIRCUIT

Consider a modified OTP circuit as shown in Fig. 3. I1 and I2 are the bias current supplied by the band-gap references. When the temperature rises, Vbe of the PNP transistor

gradually decreases. When VA ≤ VB, the comparator is reversed, OTP is high, and Pmos1 is off. When the temperature drops from high to low, VA gradually increases, and while VA ≥ VB, OTP releases. These two temperature related turning points can be derived as in (5) and (6), respectively, from which, they are designed based on the current differences and no longer affected by the voltage fluctuations, as shown in (3) and (4).

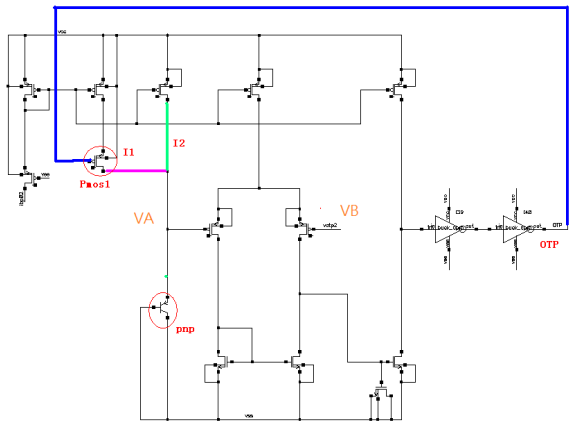


Fig. 3 The proposed modified over temperature protection circuit

$$Ttriggering = VB/(K0/q*\ln((I1+I2)/Is)) \quad (5)$$

$$Treset = VB/(K0/q*\ln(I2/Is)) \quad (6)$$

Figure 4 simulated the designed triggering and reset points of the OTP circuit in Fig. 3. The hysteresis band was set to 20 degree Celsius. Fig. 5 shows the full-corner simulation results, from which, the spreads of the turning points are within 10 degree Celsius, which shows a significant improvement over the previous circuits.

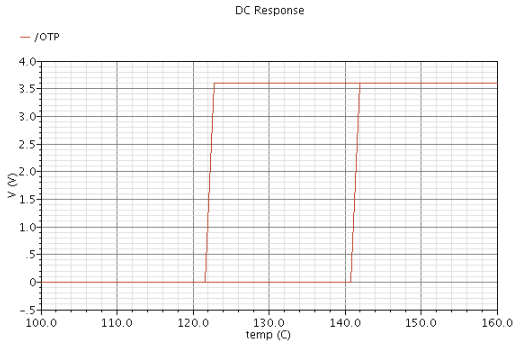


Fig. 4 Simulated hysteresis band of OTP points

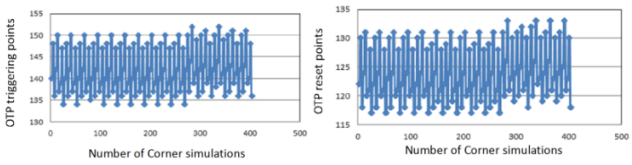


Fig. 5(a) Full-corner simulated OTP triggering points and (b) reset points (unit in Celsius) of the circuits shown in Fig. 3

## IV. Summary

Design of over temperature protection circuits is addressed in this paper. An improved architecture based on comparing current differences instead of two dispersed voltage levels were designed and verified with full-corner simulations. The simulated results show that the maximum variation is within 10 % across 300 different corners.

## Reference


[1] A-V. Bezooijen, F.-V. Straten, R-Mahmoudi, A.-m. Van Roermund, " Over-Temperature Protection by Adaptive Output Power Control", 2006 European Microwave Conference, 2006, pp. 1645 - 1647.

[2] B. Wang, Q. Feng, S. Zhuang, "A low voltage CMOS over-temperature protection circuit with MOSFETs working in the sub-threshold region", 2016 13th IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT), 2016, pp. 1372 - 1374.

[3] C-S Plesa, M. Neag, C. Boianceanu, A. Negoita, " Design methodology for over-temperature protection of an LDO voltage regulator by using electro-thermal simulations", 2016 22nd International Workshop on Thermal Investigations of ICs and Systems (THERMINIC), 2016, pp. 46 - 51.

[4] C. Tan, Z. Liu, Q.Yan, " A Bandgap Reference and Over Temperature Protection Circuit Designed for TCXO Chip", 2015 International Conference on Intelligent Transportation, Big Data and Smart City, 2015, pp. 8 - 11.

[5] L. Cartagena and S. Barbin, "Low power CMOS temperature protection sensor for smart cards", 2017 SBMO/IEEE MTT-S International Microwave and Optoelectronics Conference (IMOC), 2017, pp. 1 - 5.

[6] J. Zhao, J. A. Salcedo, and J.-J. Hajjar, "On-chip protection in precision integrated circuits operating at high voltage and high temperature", 2016 IEEE International Reliability Physics Symposium (IRPS), 2016, pp. EL-4.1-3.

[7] F. Qi and L. Xu, "Development of a High-Temperature Gate Drive and Protection Circuit Using Discrete Components", IEEE Transactions on Power Electronics, 2017, Volume: 32, Issue: 4, pp. 2957 - 2963.