Measurements of critical charge around rising edge of clock signal

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***Abstract*--This paper analyzed the critical charges of a master-slave D-FF when a soft error occurred around a rising edge of a clock signal. We measured the critical charge around a rising edge of clock signal, and then compared that when CLK is stable. This analysis showed that single events can bring about an upset even when the master latch is in a transparent state (i.e. CLK=0) around rising edge of clock signal while event do not incur an upset when the master latch is stably in a transparent state. Furthermore for CLK=0 there is a period in which the critical charge is lower than that for CLK=1. In our simulation, the period occurred 0.1ns prior to the clock edge.**

I. Introduction

The recent VLSI (Very Large Scale Integration) systems are getting smaller and smaller, and electronic circuits drive lower power. This development has made our lives wealthier. However, it makes the soft error issue more serious. Soft errors are transient errors caused by energetic particles hitting [1]-[2]. Hitting on the silicon bulk accumulates electrons and holes at a drain node. The collected electrons or holes lead to transient voltage and rewrite the holding value [3]. The shrinking voltage scaling leads to more frequent occurrence of soft errors on storage elements, such as latches.

Storage element has two states, the transparent and close states. Single event can incur an upset when a particle hits to a storage element in close state. In the transparent state, no upsets occur because correct value is supplied as the input signal and thus errors are immediately corrected by the input signal. However, if a soft error occur around a clock edge, in specific after the setup time and before the hold time, the value stored in storage elements is not stable and thus the elements may not operate as expected.

This paper is organized as follows: Section II introduces related knowledges and simulation environment as preliminaries. Section III presents the simulation and evaluation results. Finally, Section IV concludes the paper.

II. Preliminaries

A. Critical charge

Critical charge is the parameter which indicates the soft error tolerant capability of circuits. In digital circuits, binary values of 0 and 1 are identified with a threshold voltage as a boundary. If the amount of charge due to a soft error is small, the error magnitude of node voltages is also small, it does not affect the stored value and output. However, if the magnitude of voltage pulse is large (beyond an expected range), it leads to an upset. As a result the stored data is flipped incorrectly. The minimum charge amount of particles leading to an upset is called as critical charge. High critical charge means a robust soft error capability.

B. Latch

A latch is a storage element capable of holding a bit value. A latch has two state, the transparent state and close state. In transparent state, the latch does not keep the output value; the value is immediately output. In close state, the input value is not used, the latch keeps outputting the stored value. In this paper, we assumed clock synchronous latches, which is in the transparent (close) state during the clock signal CLK is 1 (0). In the transparent state, the correct output value is supplied as the input signal. So, even if a voltage pulse occurs, it is corrected soon. In the close state, the voltage pulse can flip the value stored in the latch.

III. Simulation

A. Simulation environment

Fig. 1 shows the construction of the D-FF used in our simulation. We can construct a master-slave D-FF by connecting two latches, master and slave latch, in series. In this D-FF, both master and slave latches store and output inverted input values. The inverted clock signal is supplied to the master latch.

Our simulation uses the 45nm Predictive Technology Model (PTM) library [4] and Synopsys HSPICE simulator. The power supply is 1.0 V. Rising and falling times for all input signals including the clock signals are 10ps. Simulation is performed at room temperature of 27℃.

To simulate a soft error we use a current source. Current pulses are injected to the node N, which is on the inverter loop of the master latch. The injection current was calculated using the equation (1) given in below [5], where τ_α and τ_b are the technology dependent constant. In this simulation, they are set to 0.164 and 0.05 respectively. Q is the injection charge. The maximal value of Q such that the output flipped is regarded as the critical charge [6].

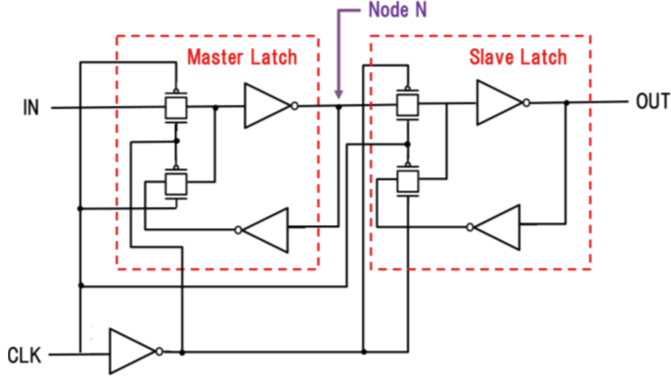

Fig. 1. The D-FF used in our simulation.

$$I_t = \frac{Q}{\tau_\alpha - \tau_\beta}\left(e^{\frac{-t}{\tau_\alpha}} - e^{\frac{-t}{\tau_\beta}}\right) \quad (1)$$

We evaluated the critical charges around a clock edge from 0.4ns before to 0.2ns after the edge. These simulations were performed in both input values IN=0 and IN=1.

B. Simulation Result

Fig. 2 shows the relation between the critical charge and the time when soft error occurs. In this simulation, the clock signal rises at 280ns. For CLK=1, the critical charge are 15fC about and 22fC for IN=1 and 0, respectively. For CLK=0, the FF can tolerate any charge at the master latch because the master latch is transparent state. For CLK=0, the closer the time when soft error occurs is to the clock edge, the lower the critical charge is. However, at 0.1ns before the clock edge, the downward slide stop. In this, the critical charges are 12fC and 19fC for IN=1 and 0, respectively. These are lower than those for the stable CLK of 1. The D-FF is in the most vulnerable condition. After this the critical charge increases slightly and goes to approach the critical charge for the stable CLK of 1.

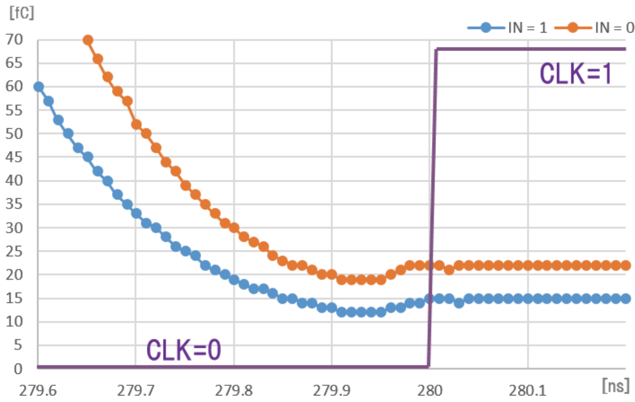

Fig. 1. The relation between the critical charge (y-axis) and the time (x-axis) when soft error occurs.

IV. CONCLUSION

This paper analyzed the critical charges of a master-slave D-FF when a soft error occurred around a rising edge of a clock signal. This analysis showed that soft errors at the master latch can flip the output value of the D-FF even when the master latch is in a transparent state if the error occurs around the rising edge of the clock signal. Critical charges decrease as the time soft error occurs approaches the rising edge. At 0.1ns before the edge, the minimal critical charge is the found. At this time, the D-FF is in the most vulnerable condition. After this the critical charge increases slightly and does to approach the critical charge for the stable CLK of 1.

ACKNOWLEDGMENT

This work was supported by VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with Synopsys, Inc.

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