Design of Floating High-Voltage Level-Shifters for Power Converter Applications

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***Abstract*—Design of fast floating high-voltage level-shifters based on cross-coupled latch pairs for high-side drivers in power converter applications is presented in this paper. A novel pre-charged circuit is proposed to reduce the voltage transition delay caused by parasitic components of the high-voltage DMOS transistors. Experimental results exhibit the designed level shifters with the capability of shifting input of 5V logic level to the maximum output voltage of 25 V and -25 V logic level using 0.25 μ m Bipolar-CMOS-DMOS(BCD) technology with the propagation delay of 6.4 nsec and 3.9 nsec, respectively, at cost of 26 pJ per transition.**

I. INTRODUCTION

Fast floating high-voltage level-shifters which translate a logic-level signal to either an elevated positive or negative voltage domain receives more and more attention in high-speed power converter applications [1-2]. Several fast level-shifters based on cross-coupled CMOS latch pairs have been reported in [2-5]. In [2], a capacitive-coupling level-shifting circuit can significantly reduce propagation delay but the voltage translation range is limited due to the voltage handling capability of on-chip capacitors. Another architecture employed two pairs of inverters in a cascode fashion was realized in [3-4]. The stacked transistors can tolerate higher voltage than the process limit but an extra voltage supply in the middle of VDD and ground is required. A fast floating high-voltage level-shifter based on a high-voltage cascode latching structure in which DMOS transistor was inserted to take the large voltage difference between two voltage domains was reported in [5-6]. Fig. 1(a) shows one of the architectures proposed in [5]. The circuit can successfully block the high-voltage switching operations from affecting low-voltage logics that would otherwise destroy low-voltage transistors, by employing high-voltage clamped DMOS transistors, and the translation speed, however, is limited by the parasitic elements of the high voltage DMOS devices. In addition, the size ratio between the active-clamped transistors and cross-coupled pairs as shown in Fig. 1(a) has to be carefully designed to avoid extra power and propagation delay. An improvement architecture was proposed in [6] to increase the translation speed of Fig. 1(a) but extra floating SR latches are required. This paper presents a modified architecture based on [5] together with a pre-charged bias circuit to reduce the voltage transition time during the level-shifting operation without costing of too much extra power. The rest content of the paper is organized as follows: In section II, the block diagram of the proposed pre-charged circuit based level-shifters is explained. Section III presents experimental results and section IV summarizes the results.

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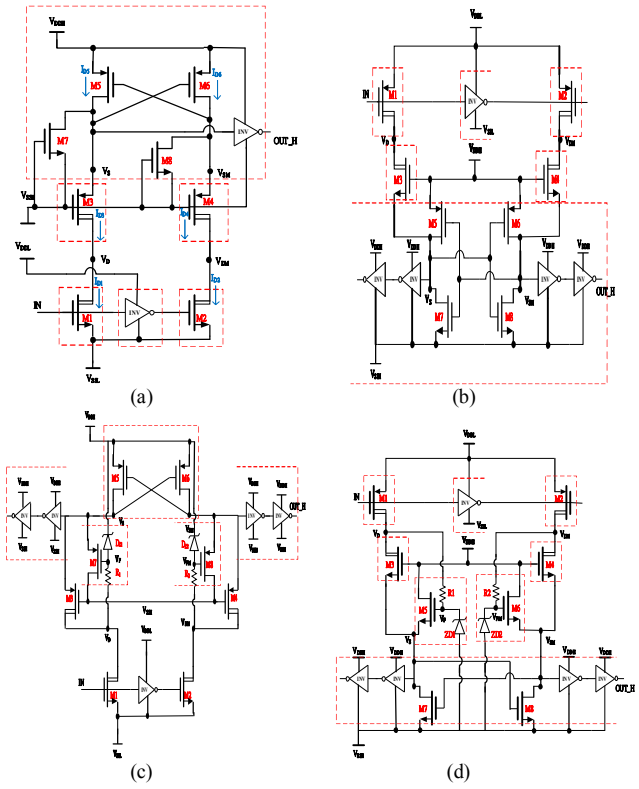


Fig. 1 Two different floating high-voltage level-shifters: (a) Level-shifting up active HV-MOS clamped circuit proposed in [5], (b) Level-shifting down active HV-MOS clamped circuit, (c) Level-shifting up active HV-MOS clamped with PMOS-assisted pre-charged circuit, and (d) Level-shifting down active HV-MOS clamped with NMOS-assisted pre-charged circuit.

II. PROPOSED CIRCUIT ARCHITECTURE

To lower the rising and falling time and hereafter propagation delay during the voltage transition period in Fig. 1(a) and (b) due to the parasitic elements of DMOS transistors, a pre-charged low-voltage PMOS/NMOS pairs were inserted between the high-side logic output and the gate of active-clamped DMOS transistors. Fig. 1(c) and (d) shows the proposed circuit schematic. For biasing two added PMOS/NMOS transistors, respectively, a pair of Zener diodes

in series with resistors were employed. The pre-charged circuit can help quickly pull up/down the drain voltage of DMOS devices during the voltage transition to reduce capactive influence by the DMOS transistors. In addition, the size ratio between low voltage cross-coupled latch pairs and DMOS transistors is no longer correlated. Since the parasitic capacitance of intrinsic PMOS/NMOS transistors is relatively small, the pull-up/down speed is less affected. In order to avoid device breakdown, these two pre-charged devices have to be inserted into a high-voltage buried layer (shown as dotted area in Fig. 1). All the components in the pre-charged cell can be designed with minimum size to reduce parasitic effects. The resistor value for biasing the PMOS/NMOS transistors can be designed relatively large in order to reduce extra static power dissipation.

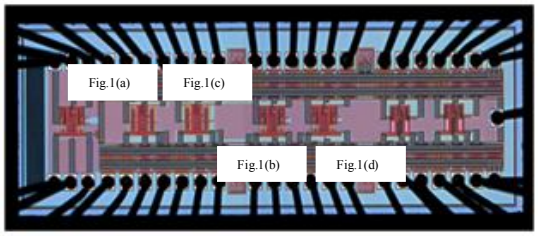
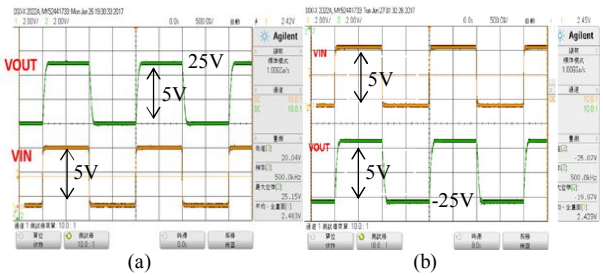
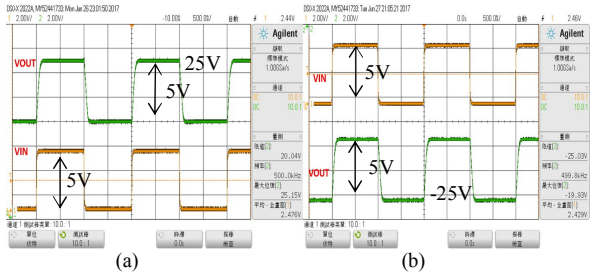


Fig. 3. Die photo of four level-shifter test key in Fig. 1(a), (b), (c), and (d), respectively



(a) (b)

Fig. 4. Experimental results of level shifting up (a) and down (b) of active HV MOS clamped without pre-charged circuit.



(a) (b)

Fig. 5. Experimental results of level shifting up (a) and down (b) of active HV MOS clamped with pre-charged circuit.

III. Experimental Results

The four level-shifters with the capability of elevating voltage up/down has been implemented in 0.25-µm 1P3M high-voltage BCD technology. Fig. 3 shows the chip photograph of the designed level-shifters with the total layout size of 2595.6 µm x 649.4 µm and size of each cell is around 150 µm x 130 µm, respectively. Fig. 4 shows the measured results of the designed level shifters with active HV-MOS clamped without pre-charged circuits. The measurement is carried out by setting input signal a square wave with 500 kHz frequency and output a 1-pF capacitance load. The propagation delay of the level-shifter is 8.8 nsec and 6.8 nsec, respectively, for up and down operations. The transition energy is estimated to be 64~65 pJ. Fig. 5 shows the measured waveform of the proposed level-shifters using the same test configuration as in Fig.4. The propagation delay is 6.4 nsec and 3.9 nsec, respectively at cost of 26~27 pJ per transition. Table I summarized the measured performance.

TABLE I
Summary of Performance

	Propagation delay (nsec)	Transition energy (pJ)	Static power dissipation (mW)	Dynamic power dissipation (mW)
Fig.1(a)	8.8	63.8	0.06	6.4
Fig.1(b)	6.4	65.4	0.04	6.1
Fig.1(c)	6.8	26.9	12.1	5.1
Fig.1(d)	3.9	26.1	7.3	2.7

IV. Summary

Design of fast floating high-voltage level-shifters for power converter applications is presented in this paper. The circuit employs a pair of pre-charged MOS transistors to improve propagation delay of the elevated voltage. Performance of high-voltage level-shifters was realized and compared using 0.25 µm BCD technology. Experimental results reveal that the proposed level-shifters can translate a 5 V logic level to 25 V and -25 V logic level with the propagation delay of 6.4 nsec and 3.9 nsec, respectively at cost of 26 pJ per transition. The total power consumption can be further reduced by lowering the static power dissipation compared to the conventional high-voltage level shifters.

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