NBL Layer Impacts on ESD Reliability for 60-V Power pLDMOS Transistors

Shen-Li Chen[1], Yi-Hao Chiu[1], Chih-Hung Yang[1], Chun-Ting Kuo[2], Yu-Lin Lin[1], Yi-Hao Chao[1], Jen-Hao Lo[2], Yu-Lin Jhou[1], Pei-Lin Wu[1]

[1]Department of Electronic Engineering, National United University, Taiwan
[2]Dept. of Integrated Circuits Design and Engineering, School of Software and Microelectronics, Peking University, China

***Abstract*--The traditional p-channel LDMOS is often used as a electrostatic discharge self-protection components in high-voltage circuit input/output pads. Nevertheless, it has one serious shortcoming that is the poor conductivity of pLDMOS leads to a very low electrostatic discharge (ESD) capacity per unit width. Therefore, a pLDMOS combined with the drain parasitic SCR to enhance its anti-ESD ability was discussed in some literatures. However, if there is an NBL isolation layer underneath the device, what happening about the ESD resistance of this pLDMOS-SCR? Eventually, we found that if there is an NBL layer under the pLDMOS-SCR, it will cause its I_{t2} anti-ESD ability > 7A. If the removal of this NBL layer, it will cause its I_{t2} anti-ESD ability in the drain region with the *npn* permutation will be much larger than the *pnp* permutation.**

I. INTRODUCTION

In recent years, under the promotion of 3C products, high-power integrated circuits rise and have a wide range of applications, such as for the rapid charging, wireless charging, automotive electronics, power management circuits, drive circuits and other markets. The planar structure of LDMOS (lateral double-diffused metal oxide field-effect transistor) is highly integrated, thus using for the main switching component or driving component in these ICs. However, the issue of electrostatic discharge (ESD) reliability in these applications is very important, but in general the ESD robustness of HV integrated components, especially for a pLDMOS is very poor. However, the LDMOS [1], silicon controlled rectifier (SCR) [2]-[3] or BJT transistor has been widely used as ESD protection devices in high voltage CMOS technologies. A traditional LDMOS acted as the ESD protection element mainly discharges the current through the underlying bipolar-junction transistor. Therefore, we will mainly focus on the anti-ESD reliability improvement of a p-channel LDMOS (pLDMOS) in this paper.

The test devices were fabricated by a TSMC 0.25-μm high voltage 60-V BCD process with non-butted source/body structure. In this work, all of pLDMOS tested devices were kept at the same geometry dimension. The length of each channel (L) is 2-μm, the unit channel width (W_f) is 100-μm, the total number of strips (M) is six, and the total width (W_{tot}) is 600-μm. A transmission-line-pulse (TLP) tester will be used to verify the snapback characteristics of these DUTs.

II. LAYOUT DESIGN OF PLDMOS DEVICES

Fig. 1 is the three-dimensional view structure of reference group of an HV pLDMOS. For studying the impact of NBL isolation layer on ESD immunity of pLDMOS devices, we divided the test samples into conventional pLDMOS, pLDMOS-SCR (*pnp*-arranged type) and (*npn*-arranged type), and which were with (or without) the N^+ buried layer (NBL) for both parasitic SCR devices. Then, pLDMOS-SCR (*pnp*-arranged type) and (*npn*-arranged type) which both with the NBL layer were shown in Figs. 2, and 3, respectively.

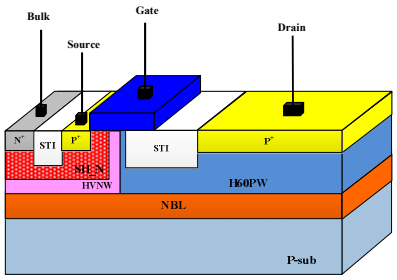

Fig. 1. 3-D structure diagram of a pLDMOS (Ref. DUT).

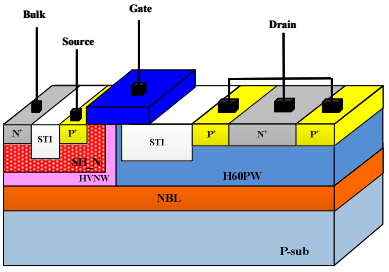

Fig. 2. 3-D structure diagram of a pLDMOS-SCR (drain side *pnp*-arranged type) with an NBL layer.

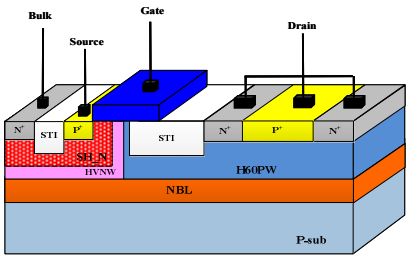

Fig. 3. 3-D structure diagram of a pLDMOS-SCR (drain side *npn*-arranged type) with an NBL layer.

III. TESTING RESULTS, DISCUSSION AND CONCLUSION

The snapback I-V curves and snapback parameters after TLP testing were shown in Fig. 4 and Table I. Based on these data, it can be found that a pLDMOS with the drain-side parasitic SCR structural will be result in reducing the component on-resistance (R_{on}) value, which leads to the decrease of the triggering voltage (V_{t1}) and the holding voltage (V_h) values, especially for the *npn*-arranged type. This is due to the location of its SCR in front of the LDMOS, so the SCR characteristics will be more obvious. Meanwhile, as the NBL layer was removed which led to a significant increase of the trigger voltage (V_{t1}) and the holding voltage (V_h) of the parasitic SCR_*pnp*-arranged type shown in Fig. 5. Therefore, the removal of the NBL structure by the parasitic SCR_*pnp*-arranged type has better in the latch-up (LU) immunity.

Fig. 6 shows the trend of secondary breakdown current (I_{t2}) of tested DUTs. It can be found that the I_{t2} value increased > 7 A by 664% upgrade as compared with the Ref. DUT except for the parasitic SCR with the *pnp*-arrangement excluding the NBL layer. Nevertheless, the I_{t2} value of pLDMOS-SCR_*pnp*-arrangement none with an NBL layer can also increase to 3.367 A by 267% upgrade. While the NBL layer adding in the pLDMOS-SCR_*pnp*-arrangement which has a better I_{t2} value than that of 3.367 A which removed the NBL layer. That is why? As for the pLDMOS-SCR_*pnp*-arranged type, owing to a large amount of current flows through the bottom NBL layer to the drain end, which can make the current flow path is relatively deep and more widely in the drain-side shown in Fig. 7(b) as compared with the Fig. 7(a) (none with the bottom NBL layer). Therefore, its anti-ESD ability will be effectively improved.

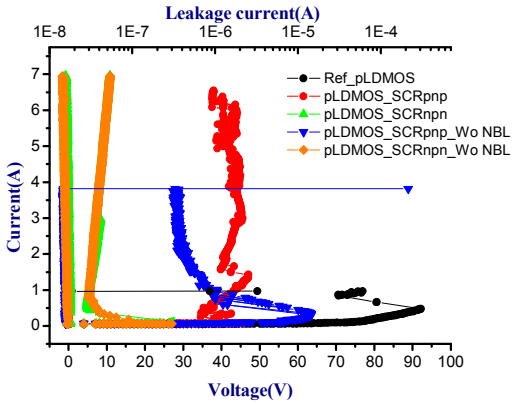

Fig. 4. Snapback I-V curves & leakage currents of tested samples.

Table I. SNAPBACK KEY PARAMETERS OF TESTED SAMPLES

Samples		V_{t1} (V)	V_h (V)	$I_{t2} \pm \sigma$ (A)
Ref_pLDMOS		76.886	76.886	0.916±0.157
Drain SCR	pnp	45.284	34.419	> 7
	npn	27.583	4.669	> 7
	pnp_wo_NBL	60.783	40.402	3.367±0.482
	npn_wo_NBL	27.024	5.408	> 7

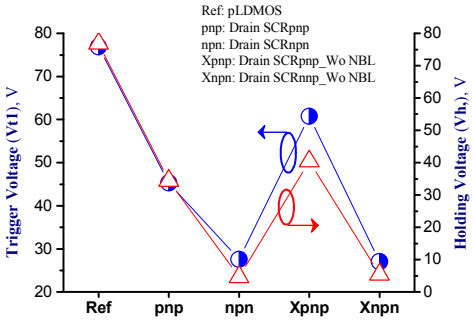

Fig. 5. V_{t1} & V_h diagrams of the tested samples.

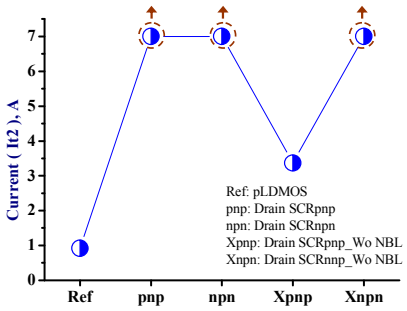

Fig. 6. The I_{t2} diagram of tested samples.

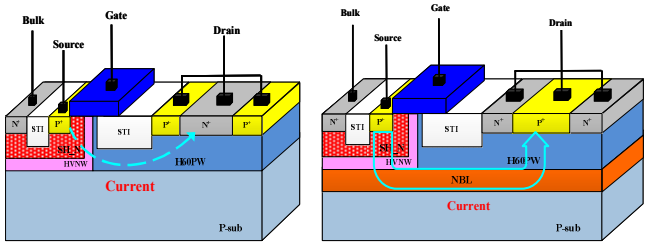

Fig. 7. ESD current path diagrams of pLDMOS-SCR drain side *pnp*-arranged type (a) without, and (b) with an NBL layer.

ACKNOWLEDGMENT

In this work, authors would like to thank the National Chip Implementation Center in Taiwan for providing the process information and fabrication platform. Moreover, authors would like to acknowledge the financial support of the Ministry of Science & Technology of Taiwan.

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