A Quarter-ROM DDS Using Phase Accumulator with Subtraction

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ABSTRACT

The conventional ROM-based direct digital frequency synthesizers (DDS) cannot output the high speed frequency due to a longer access time of the ROM table, therefore, a quarter wave symmetry technique that stores only one quarter of a sine wave is used to reduce the ROM table size. However, the sine wave produced by the DDS will have a poor symmetry if directly using the output of the phase accumulator to access a quarter ROM. In this paper, a phase accumulator with subtraction operation is proposed to improve the symmetry of the conventional quarter-ROM DDS, and this design does not require much hardware complexity.

I. INTRODUCTION

Direct digital frequency synthesizers (DDS) are important components in modern digital communication systems, and they are usually used in many applications such as digital radio and modems [1]. Using a ROM lookup table is the most commonly used method to convert the phase increments generated by a phase accumulator into the corresponding sine amplitude values. In the past, several improved methods were proposed to reduce a ROM table size. The one-quadrant ROM DDS [2] only needs a quarter-period ROM lookup table due to the symmetry and polarity of a sine wave. The initial guess/correction methods [3] provide an initial guess for the sine function, and then correct the errors between the prediction and the practical sine wave by a small correcting ROM table, such as the Parabolic-DDS [3] which uses a parabolic curve to approximate the sine wave initially. The other ROM-less DDSs employ mathematical algorithms to realize the sine function [4]. However, a large computation complexity is required for these DDSs by using approximation methods, and that will incur more power consumption. Based on a quarter-ROM DDS scheme, a phase accumulator providing a subtraction operation, without much hardware cost, is proposed to achieve a good symmetry of sine wave in this paper.

II. QUARTER-ROM DDS

Fig. 1 shows the basic structure of a quarter-ROM DDS scheme, where the amplitude values of a quarter period (0~π/2) of sine wave are stored into a quarter ROM table. The phase accumulator consists of an m-bit parallel adder and a latch rgister, and it can accumulate the frequency setting word (FSW; K) at each clock cycle to generate a periodical output of phase increments (x_j, j=0~m-1). Here, two most significant bits: POL and SYM are used to indicate the polarity and symmetry of one period of sine wave, respectively [2]. The rest n bits: x_i will pass through the inverter logical circuit controlled by SYM bit to form the address (y_i) of a quarter ROM, and then the ROM output data (d_k) delivers to the DAC which output polarity is decided by POL bit. After filtering of a low-pass filter, a complete sine wave will be generated as Table 1 described. Due to that the output frequency f_o of the conventional DDS [1] at a given K is:

$$f_O = \frac{K}{2^n} \times f_{CLK}, \tag{1}$$

where f_{CLK} is the input clock frequency, therefore, the real output frequency for a quarter-ROM DDS will be f_o/4. Actually, the ROM addresses at SYM=0 and at SYM=1 are asymmetric under some K values, which affects its symmetry of the generated sine wave.

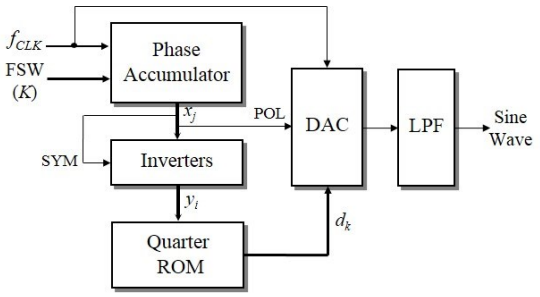


Fig. 1. Structure of a quarter-ROM DDS.

Table 1. Description of DDS Operation.

POL	SYM	ROM Address (y_i)	DAC Output
0	0	0~π/2: x_i	1st quarter sine wave (+)
0	1	π/2~π: $\overline{x_i}$	2nd quarter sine wave (+)
1	0	π~3/2π: x_i	3rd quarter sine wave (–)
1	1	3π/2~2π: $\overline{x_i}$	4th quarter sine wave (–)

III. DESIGN OF PROPOSED QUARTER-ROM DDS

For improving the symmetry of the conventional quarter-ROM DDS, the proposed DDS architecture shown in Fig. 2 will add a 2-bit counter. In this DDS scheme, the 2-bit counter is used to generate SYM and POL signals instead of 2 MSB bits from the output of the phase accumulator, and the states of SYM and POL will change when the overflow (OV) of the phase accumulator occurs, where the OV signal is connected to the clock input of the 2-bit counter. The position of the inverter logical circuit controlled by SYM is placed in front of the

parallel adder. This inverter logical circuit can be implemented by n-1 XOR gates, and their one of input pins is connected to the SYM signal to determine if invert the FSW (K) or not. Besides, the SYM signal also connects to the carry input of the parallel adder. Therefore, the phase accumulator in our proposed DDS can execute an addition or a subtraction operation depended on the state of SYM.

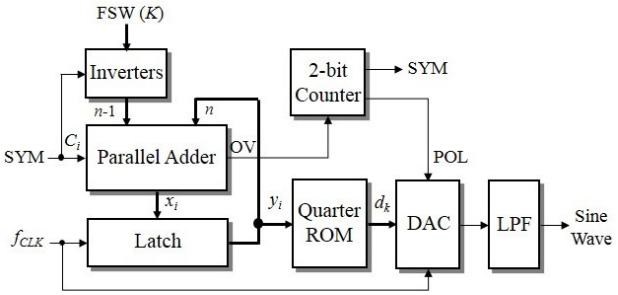


Fig. 2. Architecture of the proposed quarter-ROM DDS.

3.1 Operation Principle

To explain how the proposed quarter-ROM DDS works, the operating steps are described as follows:

(1) Initially, both POL and SYM are "0", the FSW directly passes through the inverter logical circuit. Therefore, the parallel adder accumulates the K value at each clock cycle and uses y_i to access the quarter ROM, and then the first quarter sine wave will be generated by the DAC and low-pass filter.

(2) During generating the second quarter sine wave, the FSW is inverted when POL is "0" and SYM is "1", and thus the output of the parallel adder: x_i becomes y_i + /K +1 to realize a subtraction operation. Hereby, the phase accumulator continually subtracts the K value at each clock cycle until the overflow occurs again, that means the address y_i to access the quarter ROM will decrease down in a reverse sequence, which is symmetrical to that of the first quarter sine wave.

(3) The generation of the third and fourth quarter sine waves are similar to above (1) and (2) operations, only the polarities of their amplitudes are negative due to that the DAC is set by POL=1.

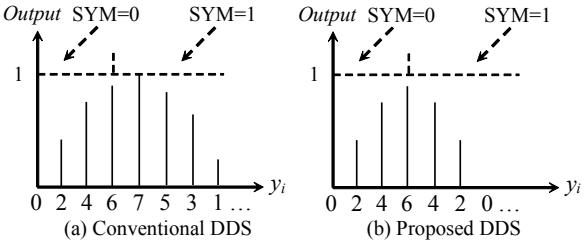


Fig. 3. Symmetry analysis for two quarter-ROM DDSs

3.2 Symmetry Analysis

Considering a 5-bit phase accumulator for the conventional quarter-ROM DDS, only 3 bits of the phase increments are used to access the quarter ROM, and thus the periodical sequence of 3-bit phase increments at K=2 is 0, 2, 4, 6. When SYM is "1", the symmetrical sequence after inverting phase increments is 7, 5, 3, 1. However, for the proposed DDS under the same conditions, the periodical sequence of phase increments including at SYM=0 and at SYM=1 is 0, 2, 4, 6, 4, 2, 0. From Fig. 3 shown, we find that these amplitudes on left side and right side of peak value are not the same in the conventional quarter-ROM DDS. However, the proposed DDS always can keep the same amplitudes on both sides of peak value in order to achieve a good symmetry.

IV. SIMULATION RESULTS

For verifying the proposed quarter-ROM DDS, a simulation platform is built by the personal computer and a USB D/A card. We try to create two quarter-ROM DDS schemes including the conventional DDS and the proposed DDS by C programming, where the memory size to store a quarter sine data is 256 words. By a conversion of the USB D/A card, a complete sine wave at K = 8 of the proposed DDS will be generated shown in Fig. 4. To further make a comparison of symmetry for two quarter-ROM DDSs, K is set to 35 for clear observation, the generated sine waves are shown in Fig. 5(a) and Fig. 5(b), respectively.

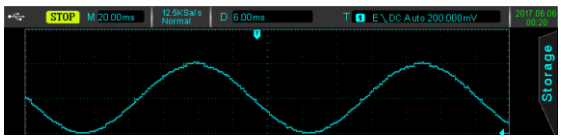
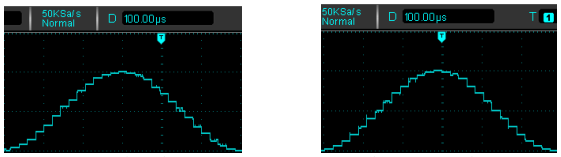


Fig. 4. Generated sine wave at f_o = 7.6 Hz.



(a) Conventional DDS (b) Proposed DDS

Fig. 5. Symmetry observation for two quarter-ROM DDSs

V. CONCLUSION

In this paper, a design of the phase accumulator with addition and subtraction is proposed to improve the symmetry of the conventional quarter-ROM DDS. Moreover, the proposed DDS scheme, without adding much hardware complexity, indeed can successfully generate a sine wave with a better symmetry through simulation and verification. The future work will focus on the practical circuit implementation and analysis.

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