Area-Efficient VLSI Architecture of High-Order Matched Filter Design Using Odd-and-Even Phase Processing for Image Recognition Applications

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***Abstract*—In this paper, we propose an area-efficient VLSI hardware architecture of matched filter design for image recognition applications, especially for larger number of taps. By using odd-phase and even-phase processing, it can extremely reduce the number of complex multipliers and complex adders utilized. As for a practical design implementation with TSMC 40-nm CMOS technology, a 64-tap matched filter circuit operates up to a clock frequency of 500MHz and only occupies a synthesis area of 0.059 mm^2. It totally saves the design area by a saving ratio of 70.29% compared to a typical transposed form circuit.**

Keywords—Area-Efficient, VLSI Architecture, Matched Filter, High Order, Image Recognition.

I. INTRODUCTION

Recently, the interests in the image recognition applications [1], [2] have become more and more popular in many fields, including video stream display, person or object identification, biomedical/ultrasound image-assisted diagnosis and under-water exploring worlds. Matched filters [3], [4] are one of the commonly-used tools to realize the specified task. Utilizing higher-order taps on transposed form matched filters [5] can make image recognition performance better in terms of identification accuracy. But, it causes lager design area occupation in hardware implementation. Thus, in order to overcome the difficulties, we propose an area-efficient VLSI architecture of matched filter, especially for high-order cases.

II. PROPOSED AREA-EFFICIENT VLSI ARCHITECTURE

The simplest hardware approach for directly realizing the core operation of matched filter is based on typical transposed form circuit [5], as an 8-tap example depicted in Fig. 1. The advantages are that the critical-path timing is always identical for any number of taps (N) and contributed by concatenating one complex multiplier and one complex adder. Unfortunately, the disadvantage is that it entirely requires N complex multipliers and (N-1) complex adders. As N increases, the components needed also get extremely increasing. Therefore, Fig. 2 demonstrates our proposed area-efficient matched filter design, which also provides the users to flexibly determine matched filter configuration. Instead of the fixed and inelastic weighting coefficients in other typical filter design circuits, our developed system has two processing stages, such as setup state and calculating state.

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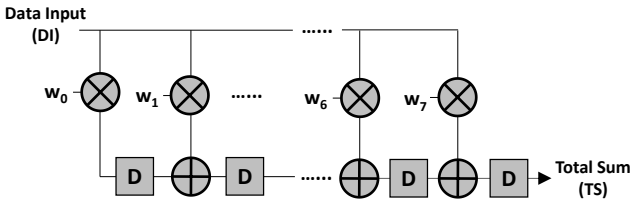

Fig. 1 Hardware design of 8-tap typical transposed form circuit.

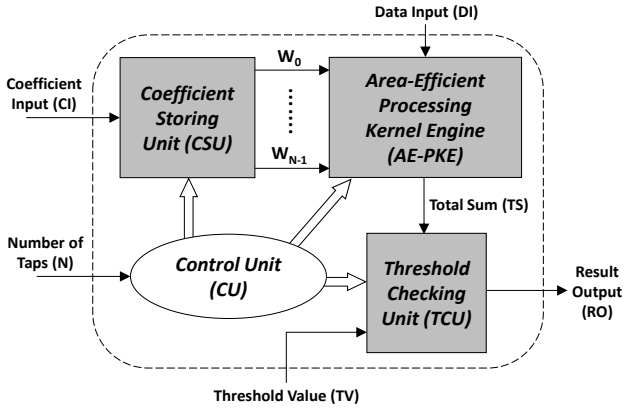

Fig. 2 Block diagram of proposed area-efficient matched filter design.

First, in setup state, the users can arbitrarily adjust the system parameters, including total number of taps (N) and each tap's weighting coefficient (W_0, …, W_{N-1}). All weighting coefficients required are determined via Coefficient Input (CI) port and stored in Coefficient Storing Unit (CSU). Secondly, in calculating state, Area-Efficient Processing Kernel Engine (AE-PKE) is used to calculate core operation of matched filter and pass the calculated value, Total Sum (TS), to Threshold Checking Unit (TCU). TCU is responsible for comparing TS with Threshold Value (TV), which is decided by the users. Finally, Result Output (RO) is single-bit, revealing the final checked result.

AE-PKE is the highlighted focus of our proposed system. By suitably utilizing hardware sharing idea, the main calculating hardware resource for N taps only consists of (N/2) complex multipliers and (N/2) complex adders, as expected to achieve an area-efficient property. As shown in Fig. 3, it is an 8-tap AE-PKE design example. We utilize double clock-rate

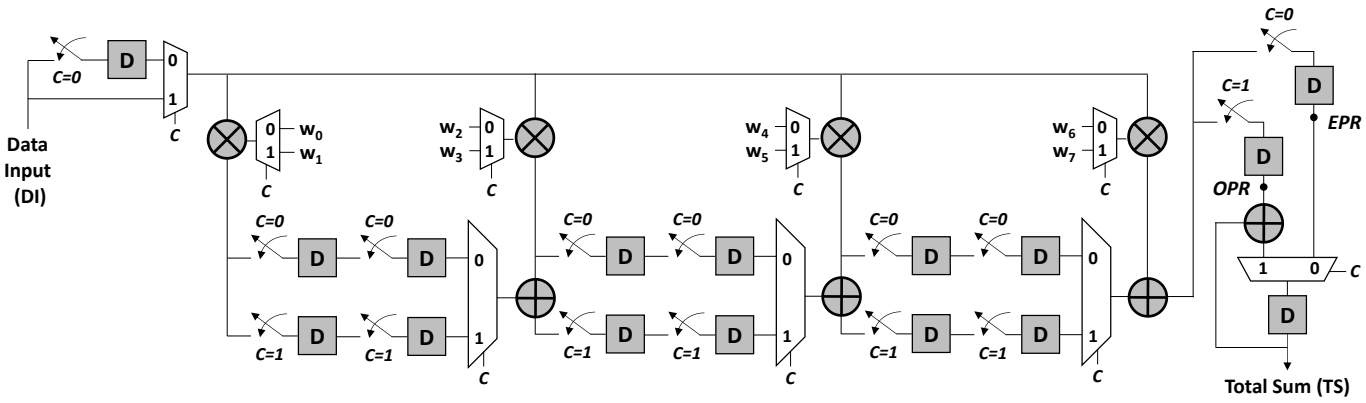

Fig. 3 Hardware design of proposed area-efficient processing kernel engine (AE-PKE): 8-tap design example.

TABLE I. AREA COMPARISON WITH DIFFERENT NUMBER OF TAPS USING TSMC 40-NM CMOS TECHNOLOGY.

Number of Taps (N)	Synthesis Area : Transposed Form Circuit (um^2)			Synthesis Area : Proposed Work (um^2)			Area Saved (um^2)	
	Combinational Circuit (X1)	Sequential Circuit (X2)	Total (X=X1+X2)	Combinational Circuit (Y1)	Sequential Circuit (Y2)	Total (Y=Y1+Y2)	Value (X-Y)	Saving Ratio
8	15344.0 (89.17%)	1864.3 (10.83%)	17208.3	4455.9 (65.82%)	2314.0 (34.18%)	6769.9	10438.4	60.66%
12	23125.7 (88.63%)	2966.5 (11.37%)	26092.2	5960.5 (61.14%)	3788.5 (38.86%)	9749.0	16343.2	62.64%
16	31154.2 (88.04%)	4232.1 (11.96%)	35386.3	7663.5 (60.32%)	5040.8 (39.68%)	12704.3	22682.0	64.10%
24	48055.5 (87.61%)	6794.1 (12.39%)	54849.6	10683.5 (56.92%)	8087.3 (43.08%)	18770.8	36078.8	65.78%
32	70940.4 (86.99%)	10614.0 (13.01%)	81554.4	14730.7 (56.30%)	11434.9 (43.70%)	26165.6	55388.8	67.92%
48	110118.8 (86.23%)	17581.9 (13.77%)	127700.7	21668.3 (55.09%)	17665.5 (44.91%)	39333.8	88366.9	69.20%
64	170031.9 (85.39%)	29090.6 (14.61%)	199122.5	29148.8 (49.27%)	30009.4 (50.73%)	59158.2	139964.3	70.29%

(2X) compared to the single clock-rate (X) in the typical transposed form circuit. A control signal (C) is regarded as a one-bit counter, toggled every clock cycle. All of clock cycles are divided into odd- and even-indexed phases for C=1 and C=0, respectively. If C=0, the system executes all of the multiplication-and-addition processing with even-indexed coefficient taps (W_0, W_2, …) and stores the summation value into data storage, even-phase result (EPR). On the other hand, the system executes all of the multiplication-and-addition processing with odd-indexed coefficient taps (W_1, W_3, …) and stores the summation value into data storage, odd-phase result (OPR), when C=1. Eventually, TS is the addition of EPR and OPR, producing the final result for next-step checking for every two clock cycles.

III. Design Implementation And Comparison

In a practical hardware implementation, we choose all weighting coefficients (W_i) and Data Input (DI) as 10 bits while setting Threshold Value (TV) as 20 bits. By using TSMC 40-nm CMOS technology, our proposed work with N=16 is synthesized with a maximum operating frequency of 500MHz, delivering a total design area of 12704.3 um^2. The combinational and sequential circuits occupy 60.32% (7663.5 um^2) and 39.68% (5040.8 um^2), respectively. By contrast, the typical transposed form circuit has a larger area occupation, such as 35386.3 um^2. Therefore, our work has an area saving ratio of 64.10%. In addition, TABLE I lists the detailed design comparison based on different number of taps. It is obvious that the area saving ratio becomes extremely increasing while N increases. For a 64-tap case, our work only has 59158.2 um^2 with an area saving ratio of 70.29%. It successfully brings the benefit of circuit area efficiency, especially for high-order demands.

IV. Conclusion

As for the matched filter design utilized in image recognition applications, we present an area-efficient VLSI hardware architecture, especially for a system requirement of high-order taps. By using odd-phase and even-phase calculating operations, it can save circuit components utilized, including complex multipliers and complex adders.

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