Area and Speed Optimization of a 5x5 Median Filter Design with 3-Direction Fast Searching Approach for Image Signal Processing Applications

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***Abstract*—In this paper, we propose 3-direction fast searching approach for a 5x5 median filter hardware architecture in the image signal processing applications. In algorithm, instead of typical serial compared schedule, this systematic approach utilizes grouping comparison in parallel to extremely shrink total comparison time. In hardware realization, it can provide an area-optimized and speed-optimized design architecture compared to other types of median-value searching methods. By using TSMC 40-nm CMOS technology, a design implementation of developed 5x5 median filter with a wordlength of 8 bits is synthesized, only occupying a design area of 0.0099 mm^2 and operating up to 250 MHz.**

Keywords—Fast Searching, Median Filter, Area-Optimized, Speed-Optimized, Image Signal Processing.

I. INTRODUCTION

Median filter [1] is usually utilized for signal-smoothing and noise-removing in digital image signal processing fields. Its benefits are to preserve the sharp edges and eliminate the noise effects, such as salt-and-pepper noises. Therefore, how to develop an area-optimized and speed-optimized hardware solution becomes our main mission and challenging task.

II. PROPOSED FAST SEARCHING ALGORITHM

Our proposed 3-direction fast searching approach is demonstrated in Fig. 1. The overall searching procedure is divided into 4 levels as follows.

Level 1: X-axis direction sorting

All of 25 signal candidates are located in a 2-dimensional XY-plane with 5x5 grids, marked as P(1, 1) ~ P(5, 5). Along X-axis direction, these 25 signals are separated into 5 groups, such as G1 ~ G5. G1 is composed of P(1, 1) ~ P(5, 1) whereas G5 consists of P(1, 5) ~ P(5, 5). In G1, we execute in-place descending sorting along X-axis direction. After sorting, the mathematical relationship of these 5 positions is P(1, 1) ≥ P(2, 1) ≥ P(3, 1) ≥ P(4, 1) ≥ P(5, 1). The other 4 groups also perform the similar actions. By the way, each group has the independent processing with respect to other groups, completing the descending sorting in parallel.

Level 2: Y-axis direction sorting

In this level, all of 25 signal candidates are again divided into 5 groups, but along Y-axis direction. Each group performs in-place descending sorting in parallel along Y-axis direction.

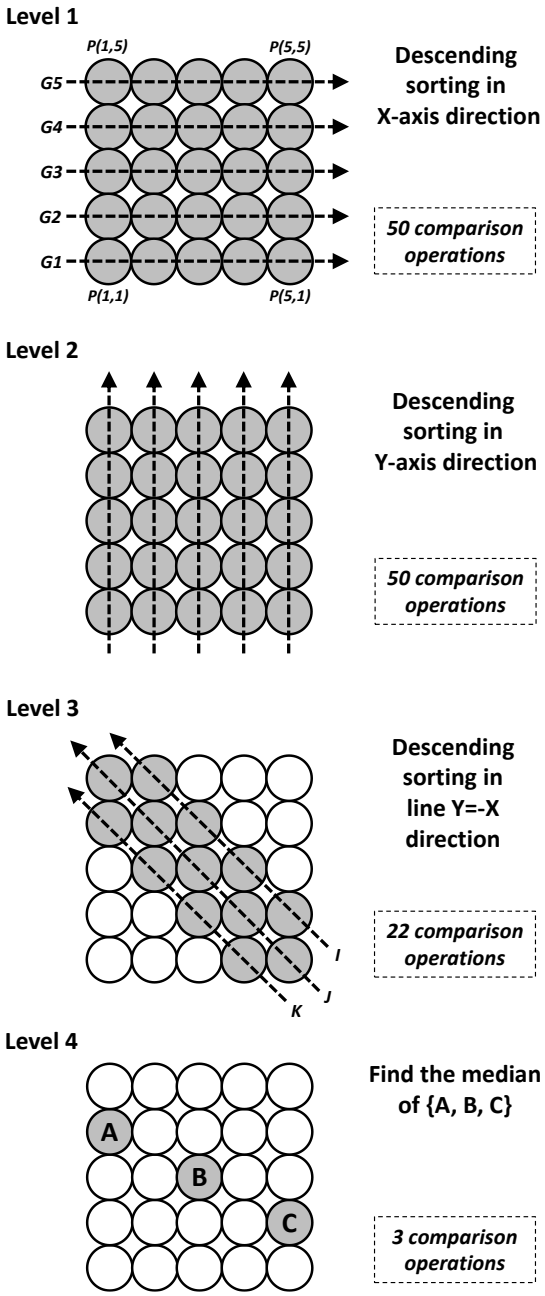

Fig. 1 Proposed 3-direction fast searching approach for a 5x5 median filter design.

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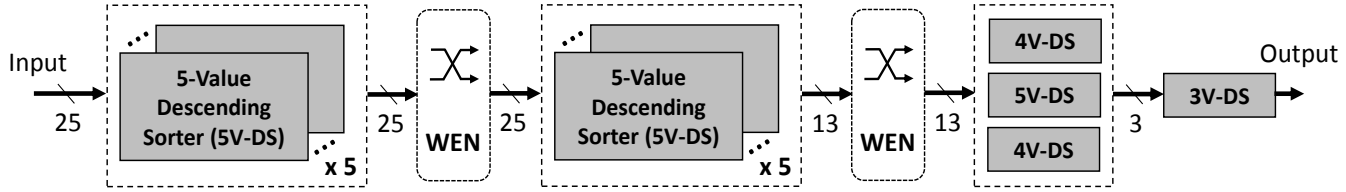

Fig. 2 Hardware architecture of proposed 5x5 median filter design.

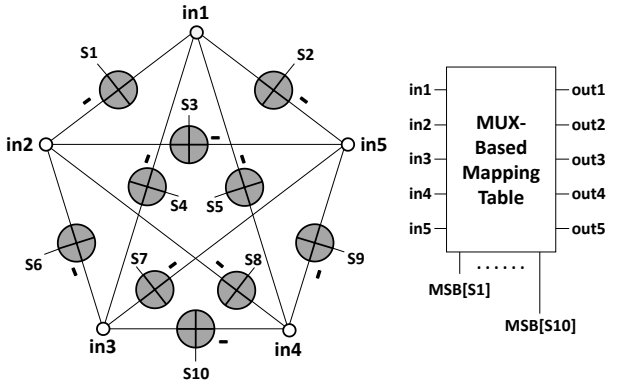

Fig. 3 Hardware design of 5-Value Descending Sorter (5V-DS).

Fig. 4 Design verification: (a) "cameraman" image with salt-and-pepper noises, (b) reconstruction result after a 5x5 median filter hardware.

TABLE I. COMPARISON OF DIFFERENT APPROACHES.

Approaches	Proposed 3-Direction Fast Searching	Bubble Sort [2]	Selection Sort [3]	Cocktail Sort [4]	Odd/Even Transposition Sort [5]
Total Number of Subtractors	125 (1^{st} rank)	234 * (2^{nd} rank)	234 *	300 **	300 ***
Computing Time (Levels)	4 (1^{st} rank)	234	234	300	25 (2^{nd} rank)

[Note] * : 234 = (24+12)*13/2, ** : 300 = (24+1)*24/2, *** : 300 = 12*25

Level 3: Line Y=-X direction sorting

After first 2 levels of sorting, there are only 13 signal candidates (as the gray-shaded circles), owning the chances to compete for the final median value. These 13 signal candidates are divided into 3 groups in line Y=-X direction. Group I, J, and K contain 4, 5, and 4 signal candidates, respectively. Each group performs in-place descending sorting in parallel along line Y=-X direction in an analogues manner.

Level 4: Final sorting of 3 candidates

Finally, the final median result is the median of 3 signal candidates, such as A, B, and C.

III. Proposed Hardware Architecture

Fig. 2 shows the hardware architecture based on our proposed algorithm. The critical design module is 5-Value Descending Sorter (5V-DS), as depicted in Fig. 3. It first employs 10 subtractors in parallel to calculate the relationship of 5 input values. All most significant bits (MSBs) of the subtraction results (S1 ~ S10) are considered as the select signals for the following mapping table, which consists of several MUXes. Eventually, 5 final outputs are remapped from the original 5 inputs. In addition, 4V-DS and 3V-DS are the reduced-forms of 5V-DS. WEN denotes the wire exchange network, passing the signals between two successive stages.

IV. Design Verification And Comparison

As illustrated in Fig. 4, our proposed design can be verified by a benchmark of "camera" image with salt-and-pepper noises. This image has 512x512 pixels and each pixel has an 8-bit gray-level value. After using our median filter hardware, the affected image is successfully reconstructed [see Fig. 4(b)].

In order to make a fair comparison, we assume that all of design approaches [2]-[5] applied on hardware have neither pipelining nor folding techniques, as listed in TABLE I. In the main circuit resource, we require less subtractors utilized, such as 125 (=10x5x2+10+6x2+3). In the aspect of main critical-path computing time, we also need less levels of subtractors in series, such as 4 levels, while just ignoring MUXes. Moreover, in the synthesis results with all 8-bit inputs and TSMC 40-nm CMOS technology, [2] requires 0.0137 mm^2 under 14 MHz (max) and [5] needs 0.0165 mm^2 under 125 MHz (max). By contrast, our design only occupies 0.0099 mm^2 and operates up to 250 MHz, outperforming all of these 4 approaches.

V. Conclusion

As for a 5x5 median filter design, we present an area-optimized and speed-optimized hardware solution compared to other median-value searching approaches.

References

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