

Design and Analysis of a Low Noise Amplifier for 5G Systems

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Abstract – This study designed a low noise amplifier (LNA) to achieve the 3.4 ~ 3.8GHz frequency band in the future 5G, and used advanced design system (ADS) for circuit design and simulation. LNA circuit using TSMC 0.18um RF CMOS process, the circuit simulation results at 3.6GHz operating frequency, the input has a good input impedance matching to 50Ω, the output has sufficient gain of 15.2dB and lower noise figure of 1.34dB, IP3 = -6dBm, P1dB = -13.5dBm, DC voltage of 1.8V and power consumption of 9.3mW.
Keyword–radio frequency (RF), Low Noise Amplifier (LNA), 5G, Noise Figure (NF)

I. INTRODUCTION

At present, the popularity of 4G network is worldwide, and the global coverage is about 70%. However, with the rapid growth of smart phones, the demand for bandwidth is keeping pace with the times, and the requirement for speed of wireless networks is also greater. As a result, a new generation of 5G (fifth generation wireless communication technology) [1] has been introduced. With the feature of a data transfer rate 10 times than 4G, low latency, 5G can meet the demand for future Mobile Health, Smart Home, and Internet of Vehicle; The release time point for 5G uncovered by Taiwan's NCC is about 2020 [2], and the 5G spectrum will be announced by various countries gradually. The 5G standard of advanced countries in Europe, the United States and Asia-Pacific will be the main references for Taiwan. Taiwan plan to release 3.4-3.8GHz and 4.4-4.9 GHz, 28GHz, 700MHz and several other frequency bands. In this study, low noise amplifier (LNA) is designed to achieve 3.4 ~ 3.8GHz band.

II. CIRCUIT DESIGN

The main function of the LNA is to provide sufficient gain and sensitivity of the RF signal from the antenna. A complete LNA consists of four parts, an input impedance matching circuit, an amplifier, bias circuit and output impedance matching circuit. The circuit architecture used in this study is inductive degeneration [3] to achieve the input impedance matching, shown in Figure 1.

Using small-signal analysis, the input impedance Z_{in} is derived as shown in equation (1). Inductance L_s is added at the source to make the input impedance extra real part. Dividing equation (1) into imaginary term and real part, we got equation (2). The real part of extra inductance L_s can match the value to 50Ω, and the imaginary part of the matching is 0, that can achieve the input impedance matching.

$$Z_{in} = sL_g + \frac{1}{sC_{gs}} + sL_s + \frac{g_m L_s}{C_{gs}} \quad (1)$$

$$\begin{cases} R_s = \frac{g_m L_s}{C_{gs}} \\ s(L_s + L_g) + \frac{1}{sC_{gs}} = 0 \end{cases} \quad (2)$$

The LNA circuit shown on Figure 2 is applied in this study [4]–[6], cascaded with a common source (CS) and common gate (CG). The main cascade amplifier M_1 is also cascaded to M_2 amplifier. This connection method uses the same DC current to reduce the current consumption. L_3 is a matching of stages inductance that counteracts parasitic common-source Output capacitance and common-gate input capacitance effect, the transistor M_1 , M_2 can get better power transmission, increase voltage gain and reduce noise; L_1 , L_2 , C_2 do input impedance matching; R_3 , L_4 , C_3 , C_4 for the output impedance matching; R_1 , R_2 , M_3 for the bias circuit, providing M_1 a stable voltage.

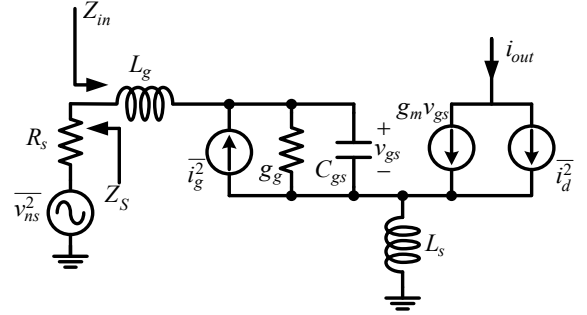


Figure 1. Inductive degeneration small-signal model

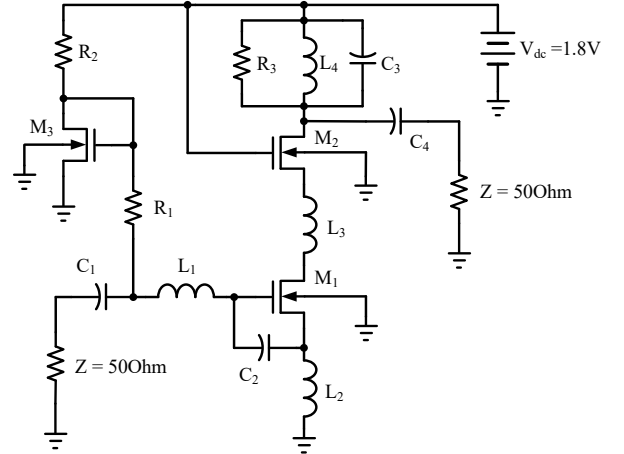


Figure 2. Low noise amplifier circuit

III. SIMULATION RESULTS

The center frequency of 3.6GHz simulation results are as follows, Figure 3 shows the input return loss at the input S11 = -39.6 dB, Figure 4 shows the output gain S21 = 15.3 dB, and Figure 5 shows the output return loss at the output S22 = -26.4 dB and Figure 6 shows the Noise Figure NF = 1.34 to 1.477dB. Figure 7 shows the gain compression point P1dB = -13.5dBm.

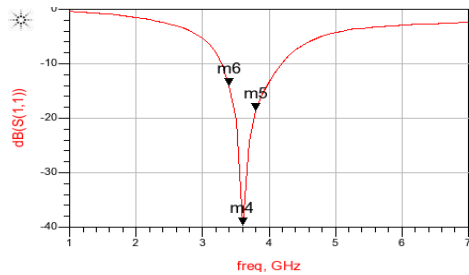


Figure 3. Input Return Loss-S11

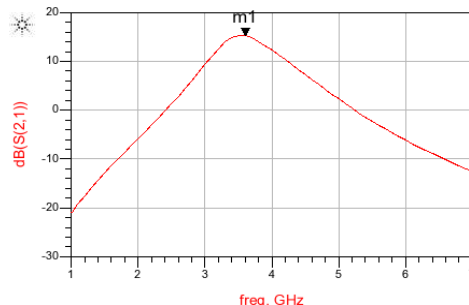


Figure 4. Input Gain S21

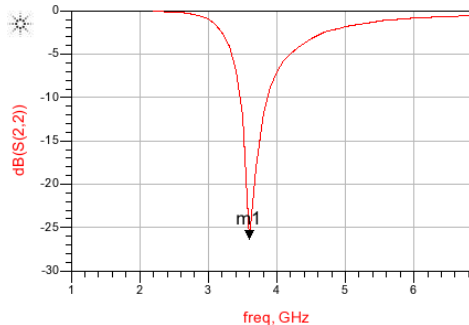


Figure 5. Output Return Loss-S22

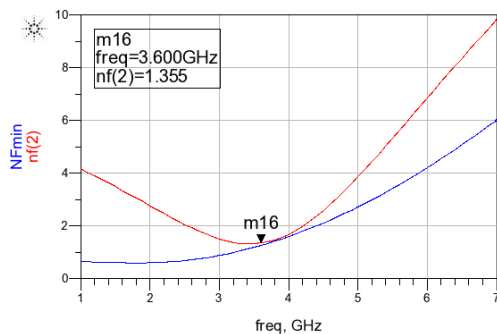


Figure 6. Noise Figure-NF

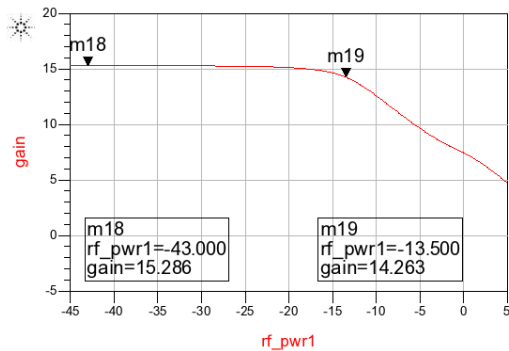


Figure 7. 1-dB Compression Point-P1dB

Third-Order Intercept Point, when there are two or more signals on the input side, and added to the amplifier circuit, there will be many additional frequency signals in the output signal to make the output signal distorted. Figure 8 shows the third-order intercept point (IP3) of -6dBm. Table 1 shows the performance of the proposed cascade LNA.

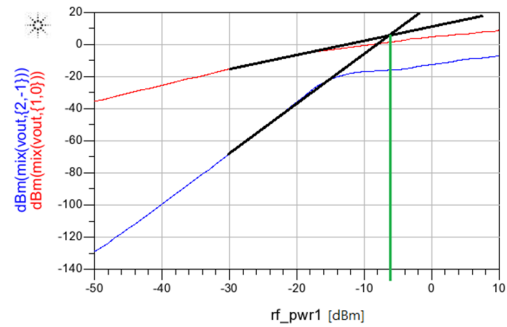


Figure 8. Third-Order Intercept Point-IP3

TABLE 1. Simulation Results of LNA

Performance	This work
Operating frequency	3.4~3.8 GHz
S11[dB]	-39.6
S21[dB]	15.3
P1db[dBm]	-13.5
IP3[dBm]	-6
Supply voltage[V]	1.8
Power[mW]	9.3

IV. CONCLUSION

This study designed a low complexity LNA, in the future 5G system in Taiwan 3.4 ~ 3.8GHz band. Use ADS to make the circuit simulation as shown in Table 1, the direct-flow voltage is 1.8V The power consumption is 9.3mW; The working frequency is 3.6GHz, S11 is -39.6dB, S21 is 15.3dB, NF is 1.34dB; P1dB = -13.5dBm, IP3 = -6dBm.

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